TWL1101
VOICE-BAND AUDIO PROCESSOR (VBAP™)

SLWS074A – MAY 1998 REVISED MARCH 1999

- 3-V Operation
- Two Differential Microphone Inputs, One Differential Earphone Output, and One Single-Ended Earphone Output
- Programmable Gain Amplifiers for Transmit, Receive, Sidetone, and Volume Control
- Earphone Mute and Microphone Mute
- On-chip I²C-Bus, Which Provides a Simple, Standard, Two-Wire Serial Interface with Digital ICs
- Programmable for 13-Bit Linear Data or 8-Bit Companded (μ-Law) Data
- Available in a 48-Pin TQFP Package, a 64-Pin μ*BGA Package, and a
- Designed for Analog and Digital Wireless Handsets and Telecommunications Applications
- TX Channel AGC Function Available Through PCM Interface or I²C Bus

description

The voice-band audio processor (VBAP) is designed to perform the transmit encoding analog/digital (A/D) conversion and receive decoding digital/analog (D/A) conversion, together with transmit and receive filtering for voice-band communications systems.

The device operates in either the 13-bit linear or 8-bit companded μ-law mode, which is selectable through the I²C interface.

From a 2.048-MHz master clock input, the VBAP generates its own internal clocks.

The TWL1101 device is characterized for operation from –40°C to 85°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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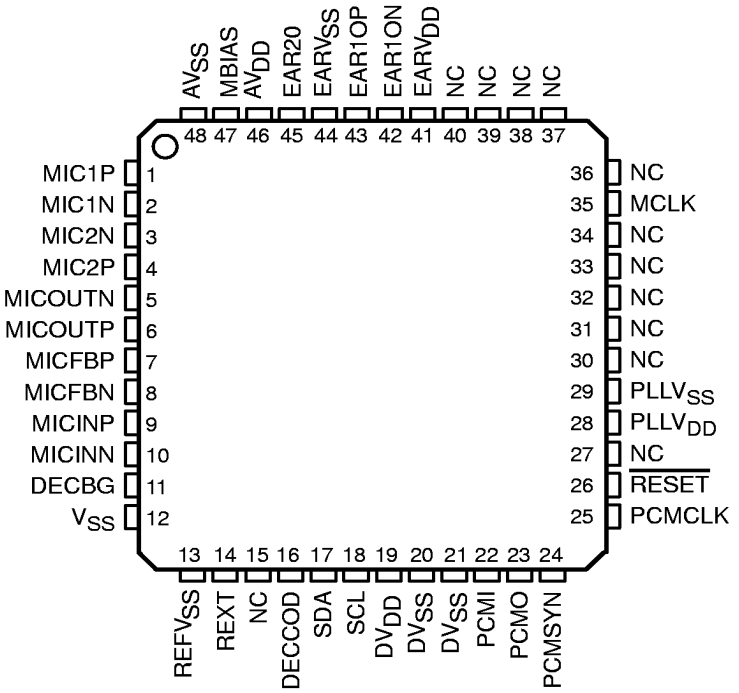
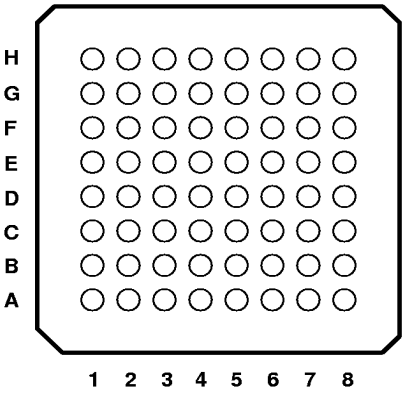
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PFB PACKAGE
(TOP VIEW)

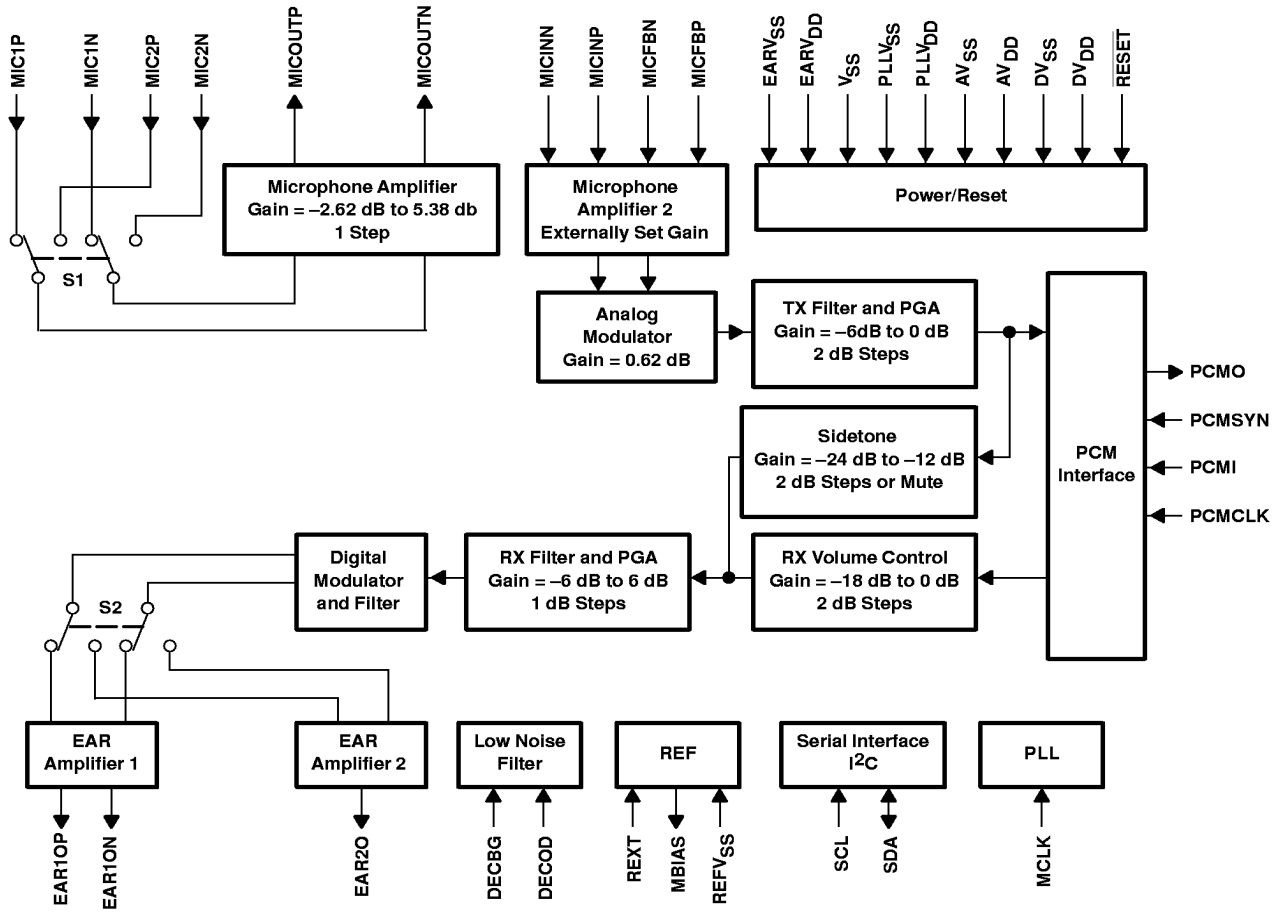


NC – No internal connection

GGV PACKAGE
(BOTTOM VIEW)



functional block diagram



functional description

power-on/reset

The power for the various digital and analog circuits is separated to improve the noise performance of the device. When digital power (DV_{DD}) is first applied, power-on reset circuitry initializes the device and puts it into the power-down state. An external reset must be applied to the active low $\overline{\text{RESET}}$ pin to guarantee reset upon power on. After the initial power-on sequence the TWL1101 can be functionally powered up and down by writing to the Power Control register through the I^2C interface.

reference

A precision band gap reference voltage is generated internally and supplies all required references to operate the transmit and receive channels. The reference system also supplies bias current for use with an electret microphone at pin MBIAS. An external precision resistor is required for reference current setting at pin REXT. A separate reference system ground is also provided at pin $REFV_{SS}$.

low noise filter

The VBAP requires external decoupling capacitors at pins DECBG and DECOD.

I^2C serial interface

The I^2C bus is a simple two-wire bidirectional serial interface. It controls the VBAP by writing data to the following five control registers: 1) power control, 2) mode control, 3) transmit PGA and sidetone control, 4) receive volume control, 5) receive PGA gain control.

phase-locked loop

The internal digital filters and modulators require a 10.24-MHz clock that is generated by phase locking to the 2.048-MHz master clock input.

PCM interface

The PCM interface transmits and receives data at the PCMO and PCMI pins respectively. The data is transmitted or received at the PCMCLK speed once every PCMSYN cycle. The PCMCLK may be tied directly to the 2.048-MHz master clock (MCLK).

microphone amplifiers

The microphone input is a switchable interface for two differential microphone inputs. The first stage is a low noise differential amplifier that provides a selectable gain of –2.62 dB or 5.38 dB, which is routed to output pins MICOUTP and MICOUTN. The second stage amplifier gain is set externally. The first and second stages may be tied directly together with a specified gain or an external filter may be added to enhance the transmit channel performance.

analog modulator

The transmit channel modulator is a third-order sigma-delta design.

transmit filter and PGA

The transmit filter is a digital filter designed to meet CCITT G.714 requirements. The device operates in either the 13-bit linear or 8-bit companded μ-law mode that is selectable through the I^2C interface. The transmit PGA defaults to 0 dB.

sidetone

A portion of the transmitted audio is attenuated and fed back to the receive channel through the sidetone path. The sidetone path defaults to –12 dB. The sidetone path can be muted by writing to the Power Control register.

receive volume control

The receive volume control block acts as an attenuator with a range of –18 dB to 0 dB in two dB steps for control of the receive channel volume. The receive volume control gain defaults to 0 dB.

receive filter and PGA

The receive filter is a digital filter that meets CCITT G.714 requirements with a high-pass filter that is selectable through the I^2C interface. The device operates in either the 13-bit linear or 8-bit μ-law companded mode, which is selectable through the I^2C interface. The gain defaults to –6 dB.

digital modulator and filter

The second-order digital modulator and filter convert the received digital PCM data to the analog output required by the earphone interface.

earphone amplifiers

The analog signal can be routed to either one of two earphone amplifiers, one with differential output (EAR1ON and EAR1OP) and one with single-ended output (EAR2O). Clicks and pops are suppressed for EAR1 differential output only.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PFB	GGV		
AV_{DD}	46	C3	I	Analog positive power supply
AV_{SS}	48	B2	I	Analog negative power supply
DECBG	11	F2	I/O	Bypass capacitor decoupling pin – bypass with 0.1 μF capacitor
DECCOD	16	G3	I/O	Bypass capacitor decoupling pin – bypass with 0.1 μF capacitor
DV_{DD}	19	G4	I	Digital positive power supply
DV_{SS}	20,21	G5, H5	I	Digital negative power supply
EAR1ON	42	B5	O	Earphone 1 amplifier output (–)
EAR1OP	43	A4	O	Earphone 1 amplifier output (+)
EAR2O	45	B3	O	Earphone 2 amplifier output
$EARV_{DD}$	41	A5	I	Analog positive power supply for the earphone amplifiers
$EARV_{SS}$	44	A3	I	Analog negative power supply for the earphone amplifiers
MBIAS	47	A2	O	Microphone bias supply output, no decoupling capacitors
MCLK	35	C8	I	Master system clock input (2.048 MHz) (digital)
MIC1N	2	B1	I	MIC1 input (–)
MIC1P	1	A1	I	MIC1 input (+)
MIC2N	3	C2	I	MIC2 input (–)
MIC2P	4	C1	I	MIC input (+)
MICOUTN	5	D3	O	Microphone differential output to external TX high-pass filter
MICOUTP	6	D1	O	Microphone differential output to external TX high-pass filter
MICINN	10	F1	I	Microphone differential input from external TX high-pass filter
MICINP	9	E1	I	Microphone differential input from external TX high-pass filter
MICFBN	8	E2	I	Microphone differential amp feedback from external TX high-pass filter
MICFBP	7	D2	I	Microphone differential amp feedback from external TX high-pass filter
PCMI	22	H6	I	Receive PCM input
PCMO	23	G6	O	Transmit PCM output
PCMSYN	24	H7	I	PCM frame sync
PCMCLK	25	F7	I	PCM data clock
$PLLV_{SS}$	29	E7	I	PLL negative power supply
$PLLV_{DD}$	28	E8	I	PLL digital power supply
$REFV_{SS}$	13	H1	I	Analog negative power supply for the reference system
$\overline{RESET}$	26	F8	I	Active low reset
REXT	14	H2	I/O	Internal 10-μA reference current setting pin – use precision 100-kΩ resistor and no filtering capacitors
SCL	18	H4	I	I^2C-bus serial clock – this input is used to synchronize the data transfer from and to the CODEC
SDA	17	H3	I/O	I^2C-bus serial address/data input/output – this is a bidirectional pin used to transfer register control addresses and data into and out of the codec. It is an open-drain terminal and therefore requires a pull-up resistor to V_{DD} (typical 10 kΩ for 100 kHz)
V_{SS}	12	G1	I	Ground return for all internal circuits. To minimize noise sources, ground connections to each device must meet as close as possible to the V_{SS} pin.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range . . . . . –0.3 V to 7.5 V
Output voltage range at DOUT,VO . . . . . –0.3 V to 7.5 V
Input voltage range at DIN, VI . . . . . –0.3 V to 7.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature range (industrial temp) . . . . . –40°C to 85°C
Storage temperature range, testing . . . . . –65°C to 150°C
Lead temperature 1,6 mm from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
GGV	809 mW	9 mW/°C	270 mW
PFB	916 mW	6.1 mW/°C	552 mW

recommended operating conditions (see Notes 1 and 2)

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, DV_{DD}, $PLLV_{DD}$, $EARV_{DD}$	2.7		3.5	V
High-level input voltage (V_{IH})	0.7 x V_{DD}			V
Low-level input voltage (V_{IL})			0.3 x V_{DD}	V
Load impedance between EAR1OP and EAR1ON-R_L (similar for EAR20)		32		Ω
Operating free-air temperature, T_A (Industrial temp)	–40		85	°C

NOTES: 1. To avoid possible damage and resulting reliability problems to these CMOS devices, the power-up sequence detailed in the system reliability features paragraph should be followed.
2. Voltages at analog inputs, outputs and V_{DD} are with respect to V_{SS}.

electrical characteristics over recommended ranges of supply voltage and free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(dd)}$	Supply current from V_{DD}	Operating, EAR1 selected			11	mA
$I_{(dd)}$	Supply current from V_{DD}	Operating, EAR2 selected			9	mA
$I_{(dd)}$	Supply current from V_{DD}	Power down			30	µA
$t_{(pu)}$	Power-up time from power down				60	ms

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage PCMO	I_{OH} = –3.2 mA V_{DD} = 3 V	DV_{DD} –0.2			V
V_{OL}	Low-level output voltage PCMO	I_{OL} = 3.2 mA V_{DD} = 3 V			0.2	V
I_{IH}	High-level input current, any digital input	V_I = 2.2V to V_{DD}			10	µA
I_{IL}	Low-level input current, any digital input	V_I = 0 to .8 V			10	µA
$C_{(i)}$	Input capacitance				10	pF
$C_{(o)}$	Output capacitance				20	pF

microphone interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage at MIC1N, MIC2N	V_I = 0 V to 3 V	–5		5	mV
I_{IB}	Input bias current at MIC1N, MIC2N		–200		200	nA
$C_{(i)}$	Input capacitance at MIC1N, MIC2N			5		pF
V_n	Microphone input referred noise, C-message weighted	Differential, external 18-dB gain setting, microphone amplifier gain = 5.38 dB			10	μV_{rms}
I_O(max)	Output source current – MBIAS		1			mA
$V_{(m)bias}$	Microphone bias supply voltage		1.88	2	2.12	V
	MICMUTE		–80			dB
	Input impedence	Fully differential	50	72	94	kΩ

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Earphone AMP1 output power	V_{DD} = 3 V, fully differential, 32-Ω load, 3-dBm0 output			35	mW
	Earphone AMP2 output power	V_{DD} = 3 V, single ended, 32-Ω load, 3-dBm0 output			10	mW
$V_{OO(1)}$	Output offset voltage at EAR1	Fully differential	–50		50	mV
$V_{OO(2)}$	Output offset voltage at EAR2	Single ended	–30		30	mV
I_O(max)	Maximum output current for EAR1(rms)	3-dBm0 input			33	mA
I_O(max)	Maximum output current for EAR2 (rms)	3-dBm0 input			17.7	mA
THD	Total harmonic distortion	V_{DD} = 3 V, 35-mW output, 32-Ω load			5%	
	EARMUTE		–80			dB

transmit gain and dynamic range, companded mode (μ-law) or linear mode selected, transmit slope filter bypassed (see Notes 3 and 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit reference-signal level (0dB)	Differential			62	mV_{rms}
Overload-signal level (3 dBm0)	Differential			248	mV_{pp}
Overload-signal level (3 dBm0) at the analog modulator input (MICFBN, MICFBP)	Differential			3.66	V_{pp}
Absolute gain error	0 dBm0 input signal, V_{DD} ±10%, T_A = –40°C to 85°C	–1		1	dB
Gain error with input level relative to gain at –10 dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at 3 dBm0 to –30 dBm0	–0.5		0.5	dB
Gain error with input level relative to gain at –10 dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at –31 dBm0 to –45 dBm0	–1		1	dB
Gain error with input level relative to gain at –10 dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at –46 dBm0 to –55 dBm0	–1.2		1.2	dB

NOTES: 3. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.

4. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 88-mV_{rms}. The transmit channel gain is 24 dB (External gain is 18 dB, the default setting for the TXPGA is 0 dB and microphone amplifier is set to 6 dB).

transmit gain and dynamic range, companded mode (μ-law) or linear mode selected, transmit slope filter enabled (see Notes 3 and 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit reference-signal level (0 dB)	Differential			62	mV_{rms}
Overload-signal level (3 dBm0)	Differential			248	mV_{pp}
Absolute gain error	0 dBm0 input signal, V_{DD} ±10%, T_A = –40°C to 85°C	–1		1	dB
Gain error with input level relative to gain at –10 dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at 3 dBm0 to –30 dBm0	–0.5		0.5	dB
Gain error with input level relative to gain at –10 dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at –31 dBm0 to –45 dBm0	–1		1	dB
Gain error with input level relative to gain at –10 dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at –46 dBm0 to –55 dBm0	–1.2		1.2	dB

NOTES: 3. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.

4. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 88 mV_{rms}. The transmit channel gain is 24 dB (External gain is 18 dB, the default setting for the TXPGA is 0 dB and microphone amplifier is set to 6 dB).

transmit filter transfer, companded mode (μ-law) or linear mode selected, transmit slope filter bypassed, external high pass filter bypassed (MCLK = 2.048 MHz)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz, internal high-pass filter disabled.	f_{MIC1} or f_{MIC2} <100 Hz	–0.5		0.5	dB
	f_{MIC1} or f_{MIC2} = 200 Hz	–0.5		0.5	dB
	f_{MIC1} or f_{MIC2} = 300 Hz to 3 kHz	–0.5		0.5	dB
	f_{MIC1} or f_{MIC2} = 3.4 kHz	–1.5		0	dB
	f_{MIC1} or f_{MIC2} = 4 kHz			–14	dB
	f_{MIC1} or f_{MIC2} = 4.6 kHz			–35	dB
	f_{MIC1} or f_{MIC2} = 8 k Hz			–47	dB
Gain relative to input signal gain at 1.02 kHz, internal high-pass filter enabled.	f_{MIC1} or f_{MIC2} <100 Hz			–15	dB
	f_{MIC1} or f_{MIC2} = 200 Hz			–5	dB

transmit filter transfer, companded mode (μ-law) or linear mode selected, transmit slope filter selected (MCLK = 2.048 MHz)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz, with slope filter selected, external high-pass filter disabled.	f_{MIC1} or f_{MIC2} =100 Hz			–27	dB
	f_{MIC1} or f_{MIC2} = 200 Hz			–8	dB
	f_{MIC1} or f_{MIC2} = 250 Hz			–4	dB
	f_{MIC1} or f_{MIC2} = 300 Hz		–1.80		dB
	f_{MIC1} or f_{MIC2} = 400 Hz		–1.50		dB
	f_{MIC1} or f_{MIC2} = 500 Hz		–1.30		dB
	f_{MIC1} or f_{MIC2} = 600 Hz		–1.1		dB
	f_{MIC1} or f_{MIC2} = 700 Hz		–0.8		dB
	f_{MIC1} or f_{MIC2} = 800 Hz		–0.57		dB
	f_{MIC1} or f_{MIC2} = 900 Hz		–0.25		dB
	f_{MIC1} or f_{MIC2} = 1000 Hz		0		dB
	f_{MIC1} or f_{MIC2} = 1000 Hz		1.8		dB
	f_{MIC1} or f_{MIC2} = 2000 Hz		4.0		dB
	f_{MIC1} or f_{MIC2} = 2500 Hz		6.5		dB
	f_{MIC1} or f_{MIC2} = 3000 Hz		7.6		dB
	f_{MIC1} or f_{MIC2} = 3100 Hz		7.7		dB
	f_{MIC1} or f_{MIC2} = 3300 Hz		8.0		dB
	f_{MIC1} or f_{MIC2} = 3500 Hz		6.48		dB
	f_{MIC1} or f_{MIC2} = 4000 Hz			–13	dB
	f_{MIC1} or f_{MIC2} = 4500 Hz			–35	dB
	f_{MIC1} or f_{MIC2} = 5000 Hz			–45	dB
	f_{MIC1} or f_{MIC2} = 8000 Hz			–50	dB

NOTE 5: The pass-band tolerance is ± 0.25 dB from 300 Hz to 3500 Hz.

transmit idle channel noise and distortion, companded mode (μ-law) selected, slope filter bypassed

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit noise, C-message weighted	TXPGA gain= 0 dB, external gain = 18 dB, microphone amplifier gain = 5.38 dB			10	μVrms
Transmit signal-to-distortion ratio with 1020-Hz sine-wave input	MIC1N, MIC1P to PCMO at 3 dBm0	25			dBm0
	MIC1N, MIC1P to PCMO at 0 dBm0	33			dBm0
	MIC1N, MIC1P to PCMO at –5 dBm0	33			dBm0
	MIC1N, MIC1P to PCMO at –10 dBm0	36			dBm0
	MIC1N, MIC1P to PCMO at –20 dBm0	35			dBm0
	MIC1N, MIC1P to PCMO at –30 dBm0	30			dBm0
	MIC1N, MIC1P to PCMO at –40 dBm0	28			dBm0
	MIC1N, MIC1P to PCMO at –45 dBm0	23			dBm0
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.1), R2	49			dB
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.2), R2	51			dB

transmit idle channel noise and distortion, companded mode (μ-law) selected, slope filter enabled

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit noise, C-message weighted	TXPGA gain = 0 dB, external gain = 18 dB, microphone amplifier gain = 5.38 dB			10	μVrms
Transmit signal-to-distortion ratio with 1020-Hz sine-wave input	MIC1N, MIC1P to PCMO at 3 dBm0	25			dBm0
	MIC1N, MIC1P to PCMO at 0 dBm0	33			dBm0
	MIC1N, MIC1P to PCMO at –5 dBm0	33			dBm0
	MIC1N, MIC1P to PCMO at –10 dBm0	36			dBm0
	MIC1N, MIC1P to PCMO at –20 dBm0	35			dBm0
	MIC1N, MIC1P to PCMO at –30 dBm0	30			dBm0
	MIC1N, MIC1P to PCMO at –40 dBm0	28			dBm0
	MIC1N, MIC1P to PCMO at –45 dBm0	23			dBm0
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.1), R2	49			dB
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.2), R2	51			dB

transmit idle channel noise and distortion, linear mode selected, slope filter bypassed

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit noise, C-message weighted	TXPGA gain = 0 dB, external gain = 18 dB, microphone amplifier gain = 5.38 dB			10	μVrms
Transmit signal-to-distortion ratio with 1020-Hz sine-wave input	MIC1N, MIC1P to PCMO at 3 dBm0	26			dB
	MIC1N, MIC1P to PCMO at 0 dBm0	50			dB
	MIC1N, MIC1P to PCMO at –5 dBm0	50			dB
	MIC1N, MIC1P to PCMO at –10 dBm0	46			dB
	MIC1N, MIC1P to PCMO at –20 dBm0	45			dB
	MIC1N, MIC1P to PCMO at –30 dBm0	40			dB
	MIC1N, MIC1P to PCMO at –40 dBm0	30			dB
	MIC1N, MIC1P to PCMO at –45 dBm0	25			dB

transmit idle channel noise and distortion, linear mode selected, slope filter enabled

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit noise, C-message weighted	TXPGA gain = 0 dB, external gain = 18 dB, microphone amplifier gain = 5.38 dB			10	μVrms
Transmit signal-to-distortion ratio with 1020-Hz sine-wave input	MIC1N, MIC1P to PCMO at +3 dBm0	26			dB
	MIC1N, MIC1P to PCMO at 0 dBm0	50			dB
	MIC1N, MIC1P to PCMO at –5 dBm0	50			dB
	MIC1N, MIC1P to PCMO at –10 dBm0	46			dB
	MIC1N, MIC1P to PCMO at –20 dBm0	45			dB
	MIC1N, MIC1P to PCMO at –30 dBm0	40			dB
	MIC1N, MIC1P to PCMO at –40 dBm0	30			dB
	MIC1N, MIC1P to PCMO at –45 dBm0	25			dB

receive gain and dynamic range, EAR1 selected, linear or companded (μ-law) mode selected (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive reference-signal level (0dB)	0dBm0 output signal			750	mV_{rms}
Overload-signal level (3 dB)				3	V_{pp}
Absolute gain error	0 dBm0 input signal, V_{DD} ±10%, T_A = –40°C to 85°C	–1		1	dB
Gain error with output level relative to gain at –10 dBm0	PCMIN to EAR1ON, EAR1OP at 3 dBm0 to –40 dBm0	–0.5		0.5	dB
Gain error with output level relative to gain at –10 dBm0	PCMIN to EAR1ON, EAR1OP at –41 dBm0 to –50 dBm0	–1		1	dB
Gain error with output level relative to gain at –10 dBm0	PCMIN to EAR1ON, EAR1OP at –51 dBm0 to –55 dBm0	–1.2		1.2	dB

NOTE 6: RXPGA = 0 dB, RXVOL = 0 dB, 1020 Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP

receive gain and dynamic range, EAR2 selected, linear or companded (μ-law) mode selected (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive reference-signal level (0 dB)	0 dBm0 output signal			400	mV_{rms}
Overload-signal level (3 dB)				1.6	V_{pp}
Absolute gain error	0 dBm0 input signal, V_{DD} ±10%, T_A = –40°C to 85°C	–1		1	dB
Gain error with output level relative to gain at –10 dBm0	PCMIN to EAR2O at 3 dBm0 to –40 dBm0	–0.5		0.5	dB
Gain error with output level relative to gain at –10 dBm0	PCMIN to EAR2O at –41 dBm0 to –50 dBm0	–1		1	dB
Gain error with output level relative to gain at –10 dBm0	PCMIN to EAR2O at –51 dBm0 to –55 dBm0	–1.2		1.2	dB

NOTE 7: RXPGA = 0 dB, RXVOL = 0 dB

receive filter transfer, companded mode (μ-law) or linear mode selected (MCLK = 2.048 MHz) (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1.02 kHz, internal high-pass filter disabled.	f_{EAR1} or f_{EAR2} <100 Hz	–0.5		0.5	dB
	f_{EAR1} or f_{EAR2} = 200 Hz	–0.5		0.5	dB
	f_{EAR1} or f_{EAR2} = 300 Hz to 3 kHz	–0.5		0.5	dB
	f_{EAR1} or f_{EAR2} = 3.4 kHz	–1.5		0	dB
	f_{EAR1} or f_{EAR2} = 4 kHz			–14	dB
	f_{EAR1} or f_{EAR2} = 4.6 kHz			–35	dB
	f_{EAR1} or f_{EAR2} = 8 kHz			–47	dB
Gain relative to input signal gain at 1.02 kHz, internal high-pass filter enabled.	f_{EAR1} or f_{EAR2} <100 Hz			–15	dB
	f_{EAR1} or f_{EAR2} = 200 Hz			–5	dB

NOTE 7: RXPGA = 0 dB, RXVOL = 0 dB

receive idle channel noise and distortion, EAR1 selected, companded mode (μ-law) selected (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, C-message weighted	PCMIN = 11111111 (μ–law)			102	μV_{rms}
Receive signal-to-distortion ratio with 1020-Hz sine-wave input	PCMIN to EAR1ON, EAR1OP at 3 dBm0	23			dB
	PCMIN to EAR1ON, EAR1OP at 0 dBm0	34			dB
	PCMIN to EAR1ON, EAR1OP at –5 dBm0	35			dB
	PCMIN to EAR1ON, EAR1OP at –10 dBm0	36			dB
	PCMIN to EAR1ON, EAR1OP at –20 dBm0	35			dB
	PCMIN to EAR1ON, EAR1OP at –30 dBm0	32			dB
	PCMIN to EAR1ON, EAR1OP at –40 dBm0	26			dB
	PCMIN to EAR1ON, EAR1OP at –45 dBm0	24			dB

NOTE 6: RXPGA = 0 dB, RXVOL = 0 dB, 1020-Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP

receive idle channel noise and distortion, EAR1 selected, linear mode selected (see Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, C–message weighted	PCMIN = 0000000000000			150	μV_{rms}
Receive signal-to-distortion ratio with 1020 Hz sine-wave input	PCMIN to EAR1ON, EAR1OP at 3 dBm0	26			dB
	PCMIN to EAR1ON, EAR1OP at 0 dBm0	50			dB
	PCMIN to EAR1ON, EAR1OP at –5 dBm0	47			dB
	PCMIN to EAR1ON, EAR1OP at –10 dBm0	46			dB
	PCMIN to EAR1ON, EAR1OP at –20 dBm0	42			dB
	PCMIN to EAR1ON, EAR1OP at –30 dBm0	33			dB
	PCMIN to EAR1ON, EAR1OP at –40 dBm0	24			dB
	PCMIN to EAR1ON, EAR1OP at –45 dBm0	18			dB
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.1), R2	50			dB
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.2), R2	54			dB

NOTE 6: RXPGA = 0dB, RXVOL = 0dB, 1020-Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP

receive idle channel noise and distortion, EAR2 selected, companded mode (μ-law) selected (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, C-message weighted	PCMIN = 11111111 (μ–law)			72	μV_{rms}
Receive signal-to-distortion ratio with 1020-Hz sine-wave input	PCMIN to EAR2O at 3 dBm0	20			dB
	PCMIN to EAR2O at 0 dBm0	33			dB
	PCMIN to EAR2O at –5 dBm0	34			dB
	PCMIN to EAR2O at –10 dBm0	34			dB
	PCMIN to EAR2O at –20 dBm0	33			dB
	PCMIN to EAR2O at –30 dBm0	32			dB
	PCMIN to EAR2O at –40 dBm0	21			dB
	PCMIN to EAR2O at –45 dBm0	17			dB

NOTE 7: RXPGA = 0dB, RXVOL = 0dB

receive idle channel noise and distortion, EAR2 selected, linear mode selected (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, C-message weighted	PCMIN = 0000000000000			106	μV_{rms}
Receive signal-to-distortion ratio with 1020-Hz sine-wave input	PCMIN to EAR2O at 3 dBm0	24			dB
	PCMIN to EAR2O at 0 dBm0	45			dB
	PCMIN to EAR2O at –5 dBm0	44			dB
	PCMIN to EAR2O at –10 dBm0	42			dB
	PCMIN to EAR2O at –20 dBm0	39			dB
	PCMIN to EAR2O at –30 dBm0	32			dB
	PCMIN to EAR2O at –40 dBm0	20			dB
	PCMIN to EAR2O at –45 dBm0	16			dB
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.1), R2	50			dB
Intermodulation distortion, 2-tone CCITT method, composite power level, –13 dBm0	CCITT G.712 (7.2), R2	54			dB

NOTE 7: RXPGA = 0 dB, RXVOL = 0 dB

power supply rejection and crosstalk attenuation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage rejection, transmit channel	MIC1N, MIC1P =0 V, V_{DD} = 3 V_{dc} + 100 mV_{rms}, f = 0 –30 KHz	–45	–50		dB
Supply voltage rejection, receive channel	PCM code = positive zero, V_{DD} = 3 V_{dc} + 100 mV_{rms}, f = 0 –30 KHz	–45	–50		dB
Crosstalk attentuation, transmit-to-receive (differential)	MIC1N, MIC1P = 0 dB, f = 300 – 3400 Hz measured differentially between EAR1ON and EAR1OP	70			dB
Crosstalk attenuation, receive-to-transmit	PCMIN = 0 dBm0, f = 300 – 3400 Hz measured at PCMO, EAR1 amplifier unloaded	70			dB

clock timing requirements

PARAMETER		MIN	NOM	MAX	UNIT
t_t	Transition time, MCLK			10	ns
f_{mclk}	MCLK frequency		2.048	2.5	MHz
	MCLK jitter			37	%
	Number of MCLK clock cycles per PCMSYN frame	256		256	
$t_{c(PCMCLK)}$	PCMCLK clock period	156	488	512	ns
	Duty cycle, PCMCLK	45	50	68%	

transmit timing requirements (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{su(PCMSYN)}$	Setup time, PCMSYN high before falling edge of PCMCLK	20	$t_{c(PCMCLK)}$–20	ns
$t_{h(PCMSYN)}$	Hold time, PCMSYN high after falling edge of PCMCLK	20	$t_{c(PCMCLK)}$–20	ns

receive timing requirements (see Figure 7)

PARAMETER		MIN	MAX	UNIT
$t_{su(PCSYN)}$	Setup time, PCMSYN high before falling edge of PCMCLK	20	$t_{c(PCMCLK)}$–20	ns
$t_{h(PCSYN)}$	Hold time, PCMSYN high after falling edge of PCMCLK	20	$t_{c(PCMCLK)}$–20	ns
$t_{su(PCMI)}$	Setup time, PCMI high or low before falling edge of PCMCLK	20		ns
$t_{h(PCMI)}$	Hold time, PCMI high or low after falling edge of PCMCLK	20		ns

switching characteristics

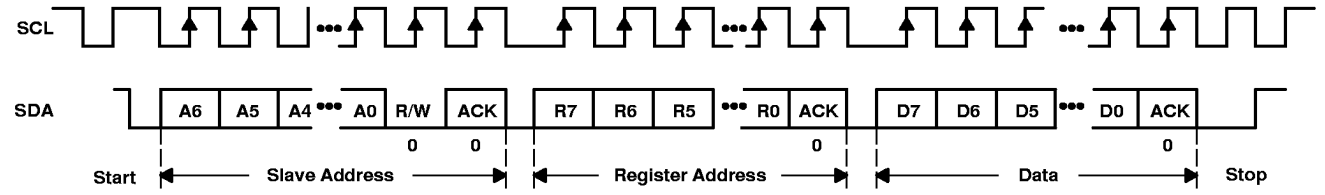
propagation delay times, C_{Lmax} = 10 pF (see Figure 6)

PARAMETER		MIN	MAX	UNIT
t_{pd1}	From PCMCLK bit 1 high to PCMO bit 1 valid		35	ns
t_{pd2}	From PCMCLK high to PCMO valid, bits 2 to n		35	ns
t_{pd3}	From PCMCLK bit n low to PCMO bit n Hi-Z	30		ns

I^2C bus timing requirements (see Figure 8)

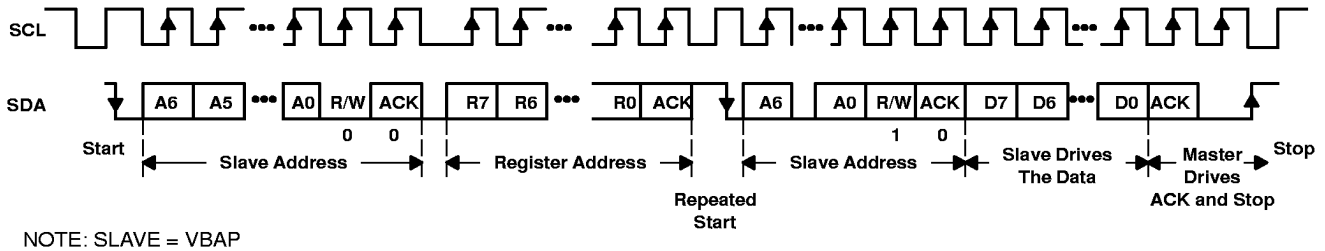
PARAMETER		MIN	MAX	UNIT
SCL	Clock frequency		400	kHz
t_{HIGH}	Clock high time	4000		ns
t_{LOW}	Clock low time	4700		ns
t_R	SDA and SCL rise time		1000	ns
t_F	SDA and SCL fall time		300	ns
$t_{HD:STA}$	Start condition setup time	4000		ns
$t_{SU:STA}$	Start condition setup time	4700		ns
$t_{HD:DAT}$	Data input hold time	0		ns
$t_{SU:DAT}$	Data input setup time	250		ns
$t_{SU:STO}$	Stop condition setup time	4000		ns
t_{BUF}	Bus free time	4700		ns

PARAMETER MEASUREMENT INFORMATION



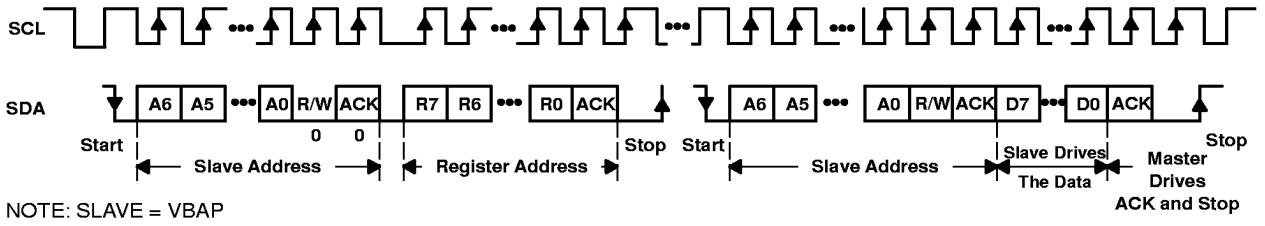
NOTE: SLAVE = VBAP

Figure 1. I²C-Bus Write to VBAP



NOTE: SLAVE = VBAP

Figure 2. I²C Read From VBAP: Protocol A



NOTE: SLAVE = VBAP

Figure 3. I²C Read From VBAP: Protocol B

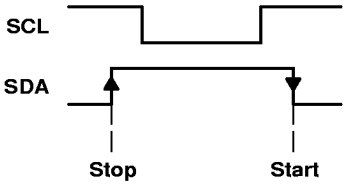


Figure 4. I²C Stop – Start Clock Timing

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PRINCIPLES OF OPERATION

power-on initialization

When digital power (DV_{DD}) is first applied, power-on reset circuitry initializes the device and puts it into the power-down state. An external reset with a minimum pulse width of 500 ns must be applied to the active low $\overline{\text{RESET}}$ pin to guarantee reset upon power on. Bit 0 of the power control register defaults to logic 0 upon reset (codec, reference system, and phase-locked loop (PLL) in power-down state). Gain control registers for the programmable gain amplifiers are initialized as indicated in the corresponding registers. The TWL1101 can be powered up by writing a logic 1 to bit 0 of the power control register through the I^2C interface. The earphone and microphone amplifiers can be selected during the same I^2C write sequence.

The desired selection for all programmable functions can be initialized prior to a power-up command using the I^2C-bus interface.

Table 1. Power-Up and Power-Down Procedures (V_{DD} = 3 V, Earphone Amplifier Unloaded)

DEVICE STATUS	PROCEDURE	MAXIMUM POWER CONSUMPTION
Power-up	Set bit zero = 1 in power control register, EAR1 enabled	33 mW
Power-up	Set bit zero = 1 in power control register, EAR2 enabled	27 mW
Power-down	Set bit zero = 0 in power control register	90 μW

In addition to resetting the power-down bit in the power control register, loss of MCLK (no transition detected) automatically enters the device into power-down state with PCMO in the high impedance state. If during a pulse code modulation (PCM) data transmit cycle an asynchronous power down occurs, the PCM interface remains powered up until the PCM data is completely transferred.

conversion laws

The device can be programmed either for 13-bit linear or 8-bit μ-law companding mode. The μ-law companding operation approximates the CCITT G.711 recommendation. The linear mode operation uses a 13-bit twos complement format.

transmit operation

microphone input

The microphone input stage is a low noise differential amplifier that provides a selectable preamplifier gain of 5.38 dB or –2.62 dB. A microphone can be capacitively connected to the MIC1N and MIC1P inputs, while the MIC2N and MIC2P inputs can be used to capacitively connect a second microphone or an auxiliary audio circuit.

PARAMETER MEASUREMENT INFORMATION

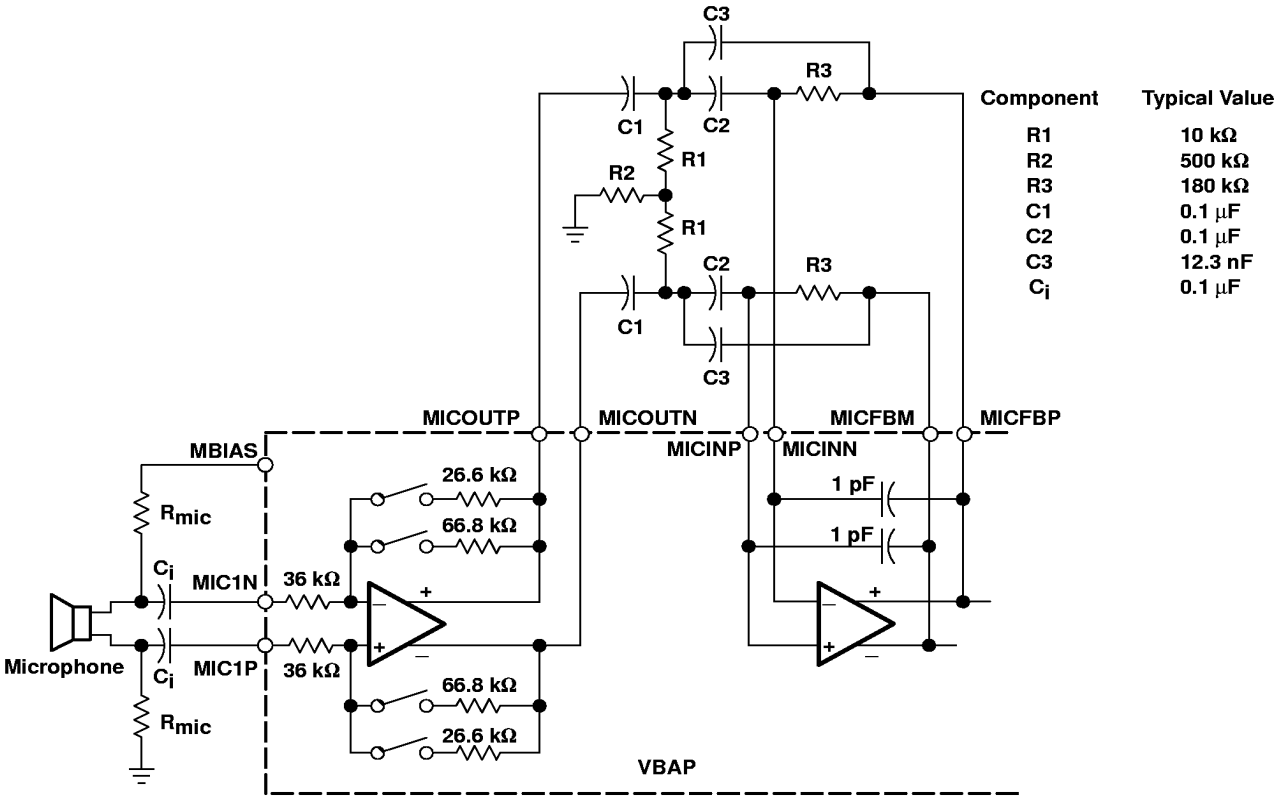


Figure 5. Typical Microphone Interface

microphone mute function

Transmit channel muting provides 80-dB attenuation of input microphone signal. The micmute function can be selected by setting bit 6 of the power control register through the serial control interface.

transmit channel gain control

The MIC AMP gain is changed along with the TX PGA block gain to perform the loud talker AGC function. The total TX channel gain can vary from 24 dB to 10 dB assuming an externally set gain of 18 dB at MIC AMP2. The AGC function can be controlled through the PCM interface or the I^2C bus. The default total TX channel gain is 24 dB.

PARAMETER MEASUREMENT INFORMATION

Table 2. Transmit Gain Control

BIT NAME			MIC AMP	MIC AMP2	TX PGA	AMOD	TOTAL TX GAIN			
TP2	TP1	TP0	GAIN	GAIN	GAIN	GAIN	MIN	TYP	MAX	UNIT
0	0	0	5.38	18	0	0.62	23.8	24	24.2	dB
0	0	1	5.38	18	–2	0.62	21.8	22	22.2	dB
0	1	0	5.38	18	–4	0.62	19.8	20	20.2	dB
0	1	1	5.38	18	–6	0.62	17.8	18	18.2	dB
1	0	0	–2.62	18	0	0.62	15.8	16	16.2	dB
1	0	1	–2.62	18	–2	0.62	14.8	14	14.2	dB
1	1	0	–2.62	18	–4	0.62	12.8	12	12.2	dB
1	1	1	–2.62	18	–6	0.62	9.8	10	10.2	dB

receive operation

receive channel gain control

The values in the receive PGA control registers control the gain in the receive path. PGA gain is set from –6 dB to 6 dB in 1-dB steps through the I^2C interface. The default receive channel gain is –6 dB.

Table 3. Receive PGA Gain Control

BIT NAME				RELATIVE GAIN			
RP3	RP2	RP1	RP0	MIN	TYP	MAX	UNIT
0	0	0	0	5.8	6	6.2	dB
0	0	0	1	4.8	5	5.2	dB
0	0	1	0	3.8	4	4.2	dB
0	0	1	1	2.8	3	3.2	dB
0	1	0	0	1.8	2	2.2	dB
0	1	0	1	0.8	1	1.2	dB
0	1	1	0	–0.2	0	0.2	dB
0	1	1	1	–1.2	–1	–0.8	dB
1	0	0	0	–2.2	–2	–1.8	dB
1	0	0	1	–3.2	–3	–2.8	dB
1	0	1	0	–4.2	–4	–3.8	dB
1	0	1	1	–5.2	–5	–4.8	dB
1	1	0	0	–6.2	–6	–5.8	dB

PARAMETER MEASUREMENT INFORMATION

sidetone gain control

The values in the sidetone PGA control registers control the sidetone gain. Sidetone gain is set from –12 dB to –24 dB in 2-dB steps through the I^2C interface. Sidetone can be muted by setting bit 7 of the power control register. The default sidetone gain is –12 dB.

Table 4. Sidetone Gain Control

BIT NAME			RELATIVE GAIN			
ST2	ST1	ST0	MIN	TYP	MAX	UNIT
0	0	0	–12.2	–12	–11.8	dB
0	0	1	–14.2	–14	–13.8	dB
0	1	0	–16.2	–16	–15.8	dB
0	1	1	–18.2	–18	–17.8	dB
1	0	0	–20.2	–20	–19.8	dB
1	0	1	–22.2	–22	–21.8	dB
1	1	0	–24.2	–24	–23.8	dB

receive volume control

The values in the volume control PGA control registers provide volume control into the earphone. Volume control gain is set from 0 dB to –18 dB in 2-dB steps through the I^2C interface. The default RX volume control gain is 0 dB.

Table 5. rx Volume Control

BIT NAME				RELATIVE GAIN			
RV3	RV2	RV1	RV0	MIN	TYP	MAX	UNIT
0	0	0	0	–0.2	0	0.2	dB
0	0	0	1	–2.2	–2	–1.8	dB
0	0	1	0	–4.2	–4	–3.8	dB
0	0	1	1	–6.2	–6	–5.8	dB
0	1	0	0	–8.2	–8	–7.8	dB
0	1	0	1	–10.2	–10	–9.8	dB
0	1	1	0	–12.2	–12	–11.8	dB
0	1	1	1	–14.2	–14	–13.8	dB
1	0	0	0	–16.2	–16	–15.8	dB
1	0	0	1	–18.2	–18	–17.8	dB

earphone amplifier

The analog signal can be routed to one of two earphone amplifiers: one with differential output (EAR1ON and EAR1OP), or one with single-ended output (EAR2O) .

PARAMETER MEASUREMENT INFORMATION

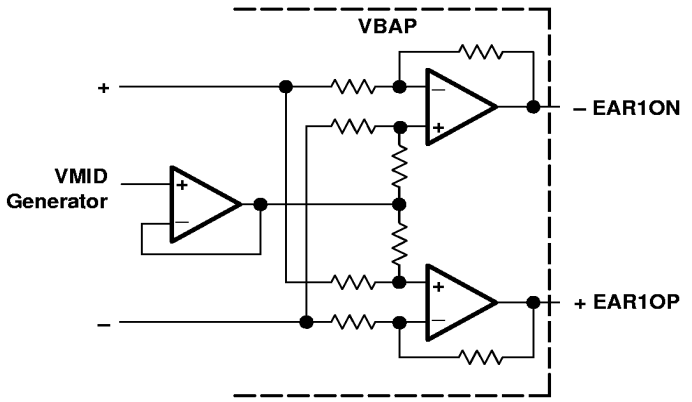


Figure 6. Differential Earphone Amplifier Configuration

earphone mute function

Muting can be selected by setting bit 3 of the power control register through the serial control interface.

receive PCM data format

1. Companded mode:
   a. Transmit channel gain control through I^2C: 8 bits are received, the most significant (MSB) first.
   b. Transmit channel gain control through PCM interface: 11 bits are received, first eight bits are companded data, next three bits are transmit channel gain control bits.
2. Linear mode:
   a. Transmit channel gain control through I^2C: 13 bits are received, MSB first.
   b. Transmit channel gain control through PCM interface: 16 bits are received, first 13 bits are linear data, next three bits are transmit channel gain control bits.

PARAMETER MEASUREMENT INFORMATION

Table 6. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	COMPANDED MODE WITH TX GAIN CONTROL	LINEAR MODE	LINEAR MODE WITH TX GAIN CONTROL
1	CD7	CD7	LD12	LD12
2	CD6	CD6	LD11	LD11
3	CD5	CD5	LD10	LD10
4	CD4	CD4	LD9	LD9
5	CD3	CD3	LD8	LD8
6	CD2	CD2	LD7	LD7
7	CD1	CD1	LD6	LD6
8	CD0	CD0	LD5	LD5
9	–	TP2	LD4	LD4
10	–	TP1	LD3	LD3
11	–	TP0	LD2	LD2
12	–	–	LD1	LD1
13	–	–	LD0	LD0
14	–	–	–	TP2
15	–	–	—	TP1
16	–	–	—	TP0

Transmit channel gain control bits always follow the PCM data in time:

CD7–CD0 = Data word in companded mode

LD12–LD0 = Data word in linear mode

TP2, TP1, TP0 : TXPGA gain control (see Table 2)

support section

The clock generator and control circuit use the MCLK input to generate internal clocks that drive internal counters, filters, and converters. Register control information is written into and read back from the VBAP registers through the I^2C–bus serial control interface.

PARAMETER MEASUREMENT INFORMATION

I²C–bus protocol

The VBAP serial interface is designed to be I²C-bus compatible. This interface consists of the following terminals:

SCL: I²C-bus serial clock – This input synchronizes the data transfer from and to the codec.

SDA: I²C-bus serial address/data input/output – This is a bidirectional pin that transfers register control addresses and data into and out of the codec. It is an open drain terminal and therefore requires a pullup resistor to V_{CC} (typical 10 kΩ for 100 KHz).

TWL1101 has a fixed device select address of {E2}HEX for write mode and {E3}HEX for read mode.

For normal data transfer, SDA is allowed to change only when SCL is low. Changes when SCL is high are reserved for indicating the start and stop conditions.

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is at high. Changes in the data line while the clock line is at high are interpreted as a start or stop condition.

Table 7. I²C-Bus Conditions

CONDITION	STATUS	DESCRIPTION
A	Bus not busy	Both data and clock lines remain at high
B	Start data transfer	A high to low transition of the SDA line while the clock (SCL) is high determines a start condition. All commands must proceed from a start condition.
C	Stop data transfer	A low to high transition of the SDA line while the clock (SCL) is high determines a stop condition. All operations must end with a stop condition.
D	Data valid	The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit data.

Each data transfer is initiated with a start condition and terminated with a stop condition. No consecutive stop and start conditions are allowed in a single clock high period (see Figure 4). The number of data bytes transferred between the start and stop conditions is determined by the master device.

When addressed, the VBAP generates an acknowledge after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with this acknowledge bit.

The VBAP must pull down the SDA line during the acknowledge clock pulse so that the SDA line is at stable low state during the high period of the acknowledge related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave (VBAP) must leave the data line high to enable the master to generate the stop condition.

current reference

An external current setting resistance of 100 kΩ ±1% must be connected from REXT to ground. No capacitance should be connected to this pin, and stray capacitance should be minimized.

clock frequencies and sample rates

A fixed PCMSYN rate of 8 KHz determines the sampling rate.

PARAMETER MEASUREMENT INFORMATION

register map

Table 8. Power Control Register: Address {00} HEX

BIT NUMBER								DEFINITIONS
7	6	5	4	3	2	1	0	
1	1	0	0	1	0	0	0	Default setting
X	X	X	X	X	X	X	0	Codec, reference system, PLL power down
X	X	X	X	X	X	X	1	Codec, reference system, PLL power up
X	X	X	X	X	0	0	X	EAR AMPS 1 and 2 power down
X	X	X	X	X	0	1	X	EAR AMP1 selected, EAR AMP2 power down
X	X	X	X	X	1	0	X	EAR AMP2 selected, EAR AMP1 power down
X	X	X	X	0	X	X	X	Receive channel enabled
X	X	X	X	1	X	X	X	Receive channel muted
X	X	0	0	X	X	X	X	MIC AMP, microphone bias amp power down
X	X	0	1	X	X	X	X	MIC1 selected
X	X	1	0	X	X	X	X	MIC2 selected
X	0	X	X	X	X	X	X	Transmit channel enabled
X	1	X	X	X	X	X	X	Transmit channel muted
0	X	X	X	X	X	X	X	Sidetone enabled
1	X	X	X	X	X	X	X	Sidetone muted

Table 9. Mode Control Register: Address {01} HEX

BIT NUMBER								DEFINITIONS
7	6	5	4	3	2	1	0	
0	1	0	0	0	0	1	0	Default setting
X	X	X	X	X	X	0	0	TX channel high-pass filter enabled and slope filter enabled
X	X	X	X	X	X	0	1	TX channel high-pass filter enabled and slope filter disabled
X	X	X	X	X	X	1	0	TX channel high-pass filter disabled and slope filter enabled
X	X	X	X	X	X	1	1	TX channel high-pass filter disabled and slope filter disabled
X	X	X	X	X	0	X	X	RX channel high-pass filter disabled (low pass only)
X	X	X	X	X	1	X	X	RX channel high-pass filter enabled
X	X	X	X	0	X	X	X	TX channel gain control through I^2C
X	X	X	X	1	X	X	X	TX channel gain control through PCMIN
X	X	X	0	X	X	X	X	Linear mode selected
X	X	X	1	X	X	X	X	μ–law companding mode selected
X	X	0	X	X	X	X	X	TX and RX channels normal mode
X	X	1	X	X	X	X	X	PCM loopback mode (TX gain control through I^2C)
X	0	X	X	X	X	X	X	TX channel gain control enabled,
X	1	X	X	X	X	X	X	TX channel gain control disabled (MIC AMP gain = 6 dB and TXPGA gain = 0 dB)

PARAMETER MEASUREMENT INFORMATION

Transmit PGA and sidetone control register: Address {02}HEX

Bit definitions :

7	6	5	4	3	2	1	0
X	X	TP2	TP1	TP0	ST2	ST1	ST0

Receive volume control register: Address {03}HEX

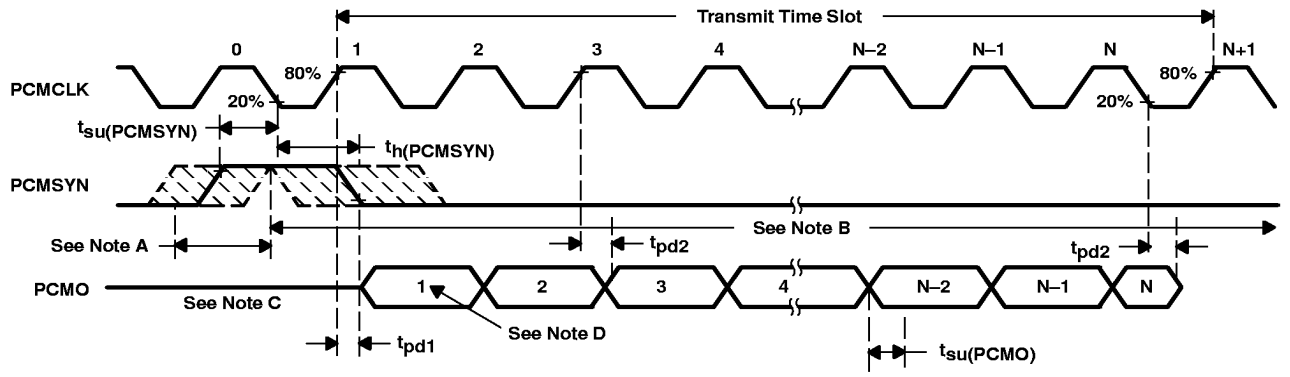
Bit definitions :

7	6	5	4	3	2	1	0
X	X	X	X	RV3	RV2	RV1	RV0

Receive PGA gain control register: Address {04}HEX

Bit definitions :

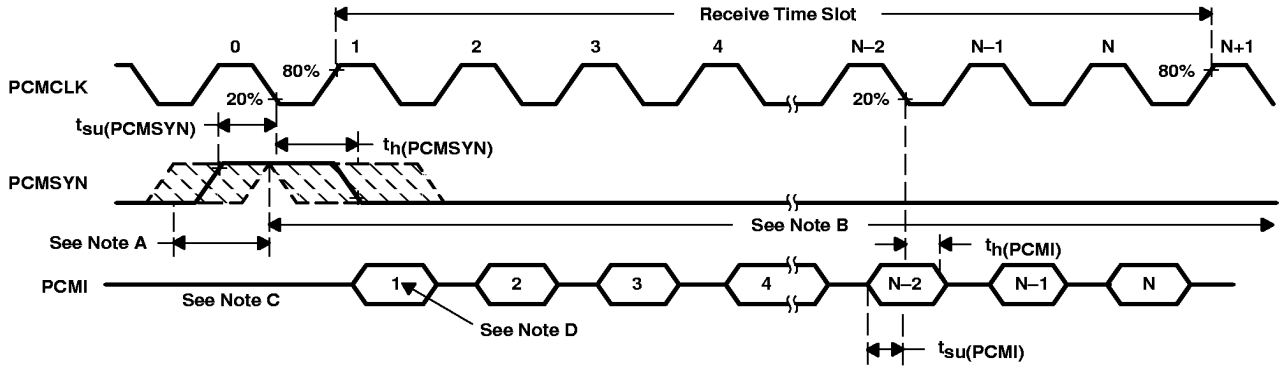
7	6	5	4	3	2	1	0
X	X	X	X	RP3	RP2	RP1	RP0



NOTES: A. This window is allowed for PCMSYN high.
B. This window is allowed for PCMSYN low ($t_{h(PCMSYN)}$max determined by data collision considerations).
C. Transitions are measured at 50%.
D. Bit 1 = MSB, Bit N = LSB

Figure 7. Transmit Timing Diagram

PARAMETER MEASUREMENT INFORMATION



A. This window is allowed for PCMSYN high.
B. This window is allowed for PCMSYN low.
C. Transitions are measured at 50%.
D. Bit 1 = MSB, Bit N = LSB

Figure 8. Receive Timing Diagram

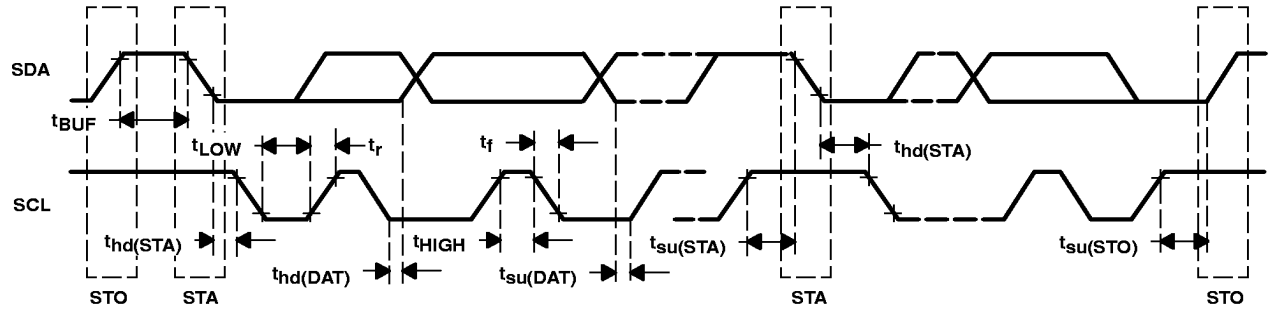


Figure 9. I²C-Bus Timing Diagram

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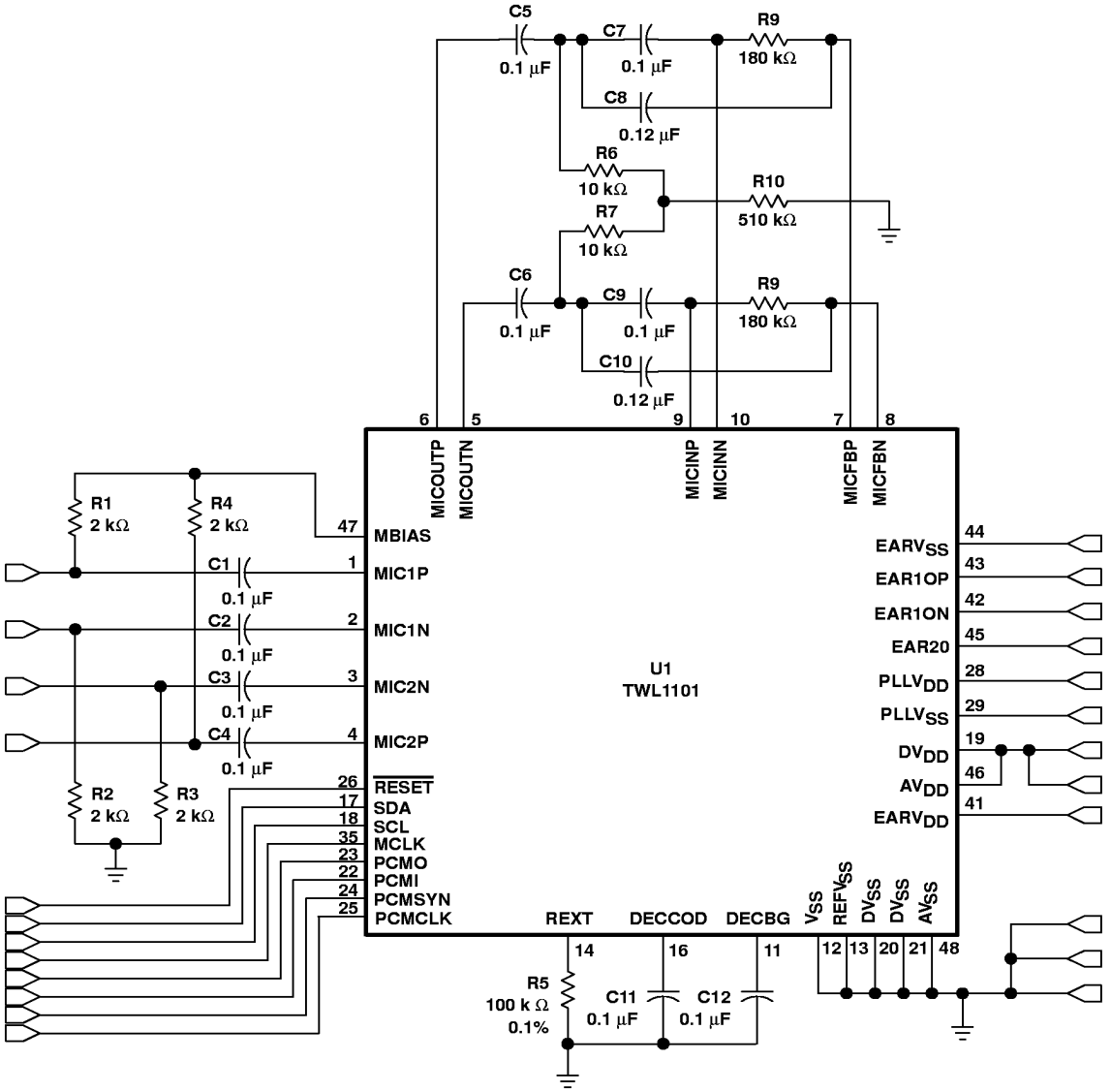
APPLICATION INFORMATION



NOTE: Pin numbers represent the 48-pin QFP package.

Figure 10. TWL1101 EVM Schematic with Filter and Mic Interface Components

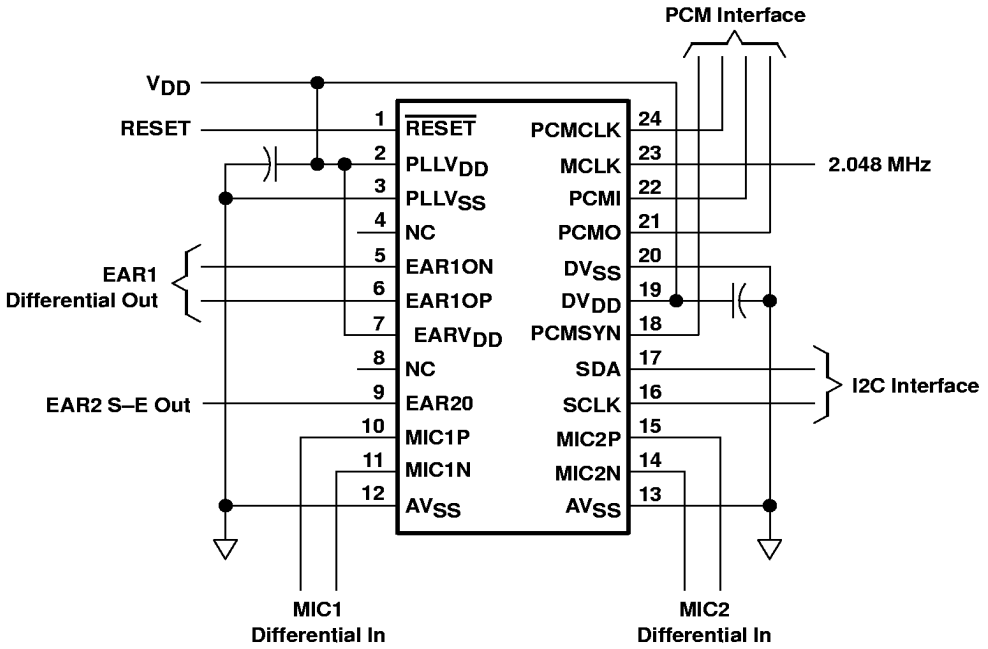
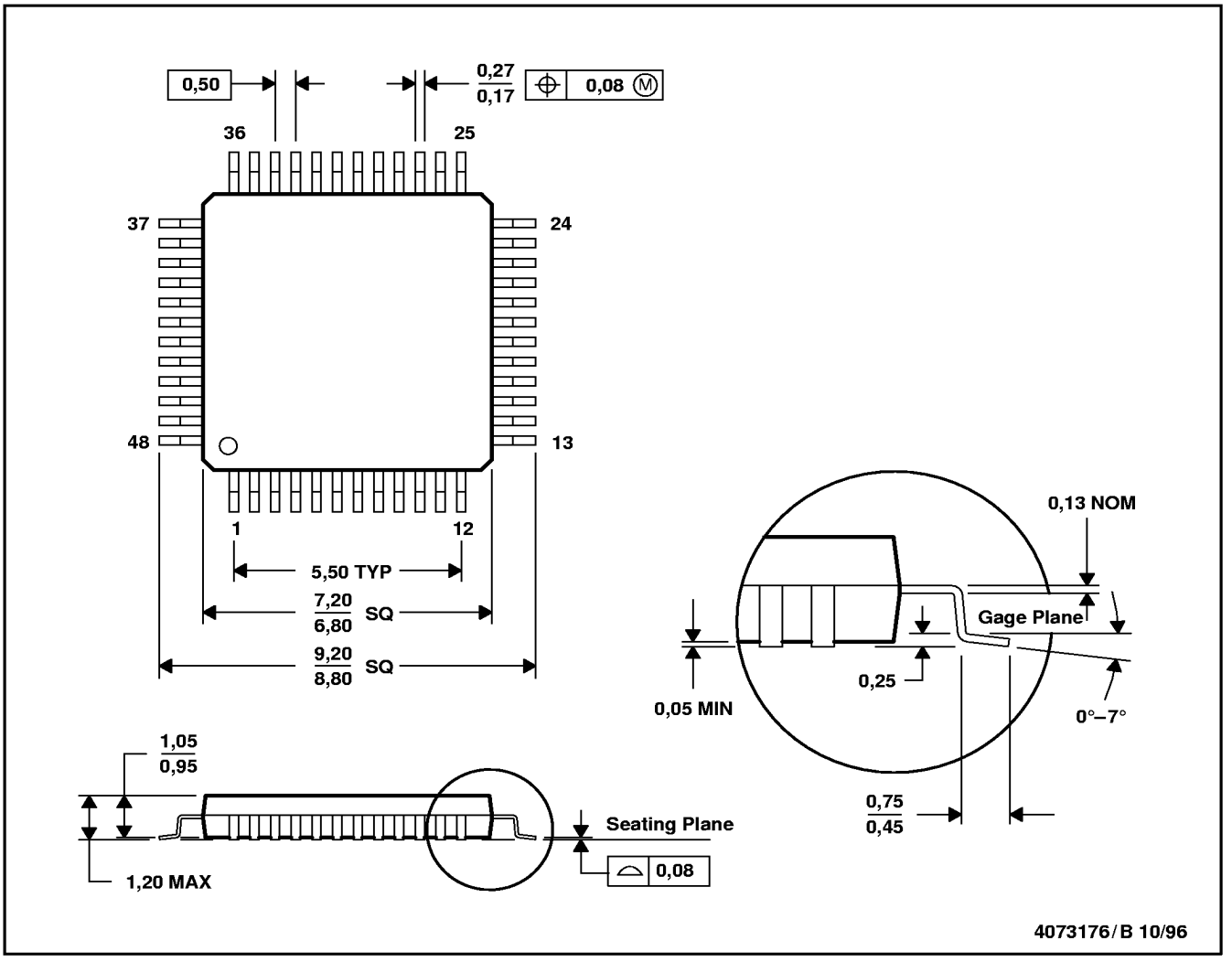


Figure 11. Typical EVM Interface to Support Circuitry

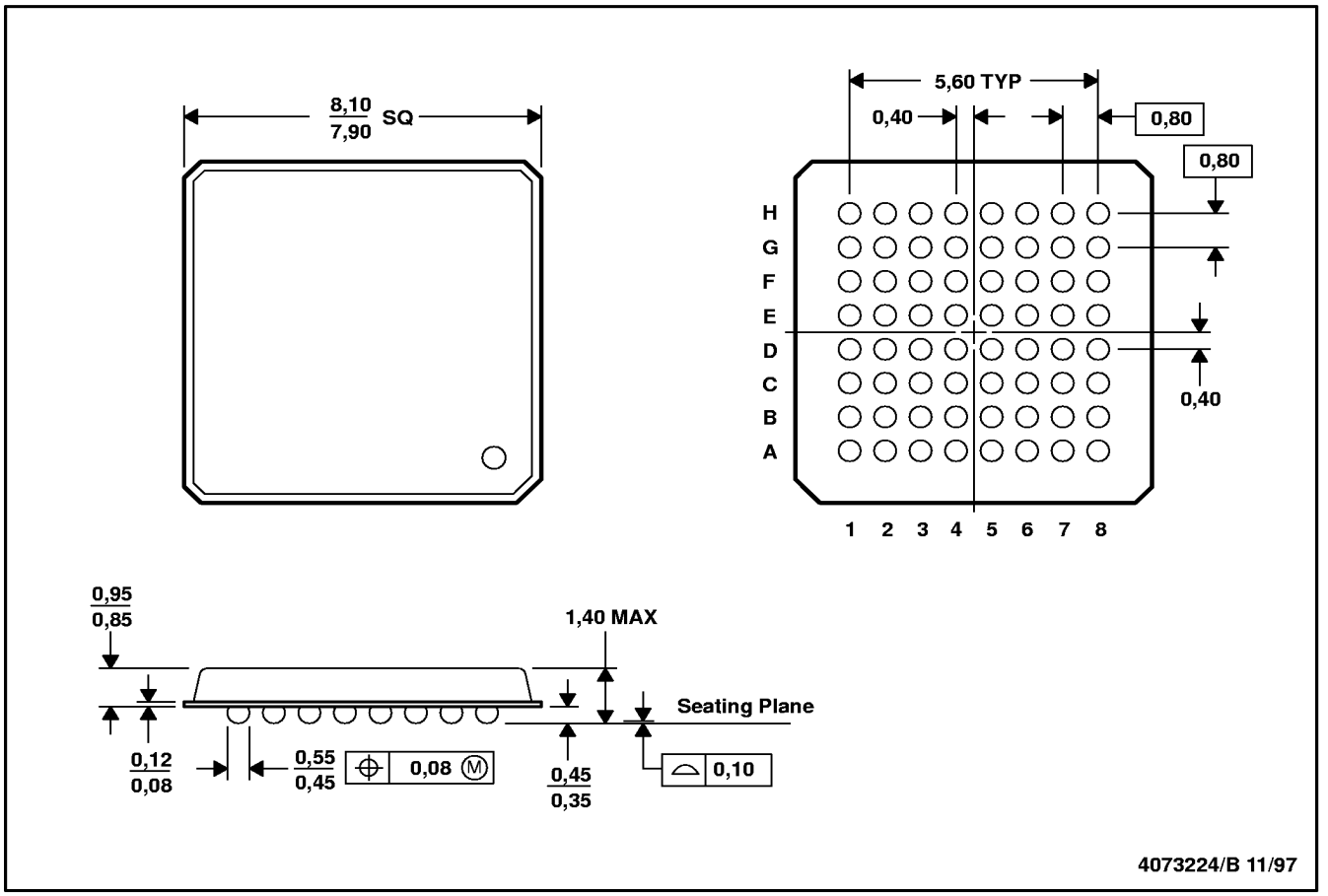
MECHANICAL DATA

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–026

GGV (S-PBGA-N64) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar™ BGA configuration

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