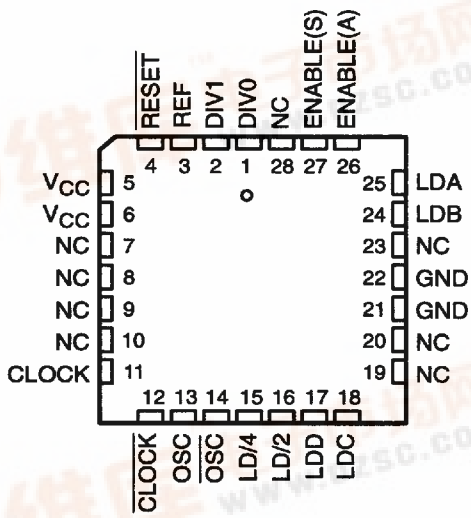
TVP2002
CLOCK DRIVER

SLAS083 – JANUARY 1994

- 135-MHz Operation
- Differential ECL Clock Generation
- Divide by 3, 4, 5, or 8 of the Clock
- Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the TLC34058
- 1.235-V Voltage Reference Output
- 5-V Single Power-Supply Operation
- 28-Pin PLCC (FN) Package
- Low Power Consumption . . . 400 mW Max
- Designed to Be Interchangeable With Brooktree Bt438

FN PACKAGE
(TOP VIEW)



NC – No internal connection

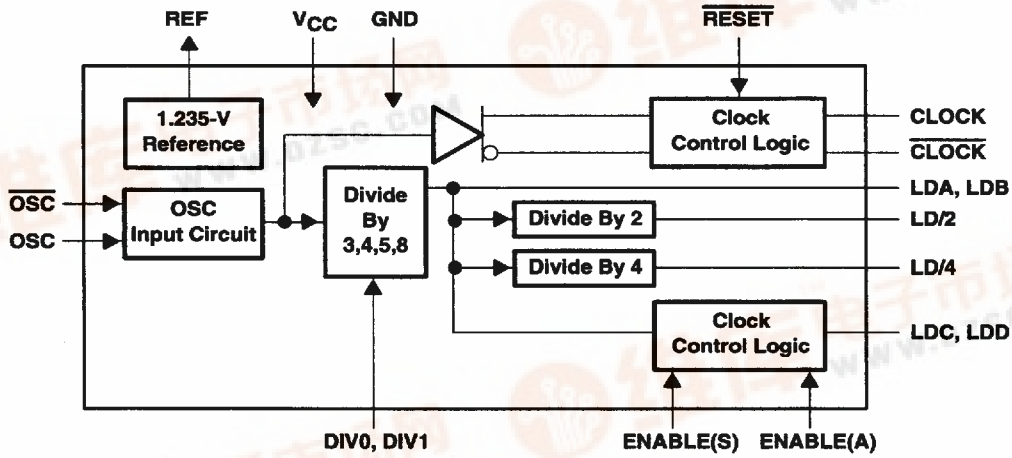
description

The TVP2002 is a clock driver for the Texas Instruments TLC34058 and functionally equivalent color palettes. It interfaces a 10KH-ECL oscillator operating from a single 5-V supply to the TLC34058, generating the necessary clock and control signals.

The clock output may be divided by 3, 4, 5, or 8 to generate the load signal. The load signal is also divided by 2 and 4 for clocking video timing logic, etc. A second load signal may be synchronously or asynchronously controlled to enable starting and stopping of the VRAM clock.

The TVP2002 also optionally configures the pipeline delay of the TLC34058 to a fixed pipeline delay. An on-chip 1.235-V reference is provided and may be used to provide the reference voltage for the color palette.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLOCK, $\overline{\text{CLOCK}}$	11, 12	O	These differential clock outputs connect directly to the CLOCK and $\overline{\text{CLOCK}}$ inputs of the TLC34058. The clock rate is equal to the OSC and $\overline{\text{OSC}}$ rate, and these terminals are capable of driving the TLC34058 directly. The output levels are equivalent to 10KH-ECL logic operating from a single 5-V supply.
DIV0, DIV1	1, 2	I (TTL compatible)	The divide control inputs specify the division factor (3, 4, 5, or 8) for the generation of the LDA and LDB signals as specified in Table 1.
ENABLE(A)	26	I (TTL compatible)	The asynchronous load-enable control input is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE(A) is low, the LDC and LDD outputs remain in the state they are in when ENABLE(A) goes to a low level. While both ENABLE(A) and ENABLE(S) are low, LDC and LDD are free-running and in phase with the LDA and LDB outputs. Care should be taken to avoid glitches on this asynchronous input.
ENABLE(S)	27	I (TTL compatible)	The synchronous load-enable control input is internally synchronized to LDA and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE(S) is low, LDC and LDD are low. While both ENABLE(A) and ENABLE(S) are high, LDC and LDD are free-running and in phase with the LDA and LDB outputs.
GND	21, 22		Device ground. GND terminals must be connected.
LDA, LDB	25, 24	O (TTL compatible)	Load outputs LDA and LDB are generated by dividing CLOCK by 3, 4, 5, or 8 as determined by the DIV0 and DIV1 inputs.
LDC, LDD	18, 17	O (TTL compatible)	Load outputs. When both ENABLE inputs are high, these outputs have the same timing as the LDA and LDB outputs.
LD/2	16	O (TTL compatible)	Load output. LD/2 is generated by dividing LDA by two.
LD/4	15	O	Load output. LD/4 is generated by dividing LDA by four.
OSC, $\overline{\text{OSC}}$	13, 14	I	Differential-ECL oscillator inputs. OSC and $\overline{\text{OSC}}$ are designed to interface to a 10KH-ECL crystal oscillator operating from a single 5-V supply.
REF	3	O	Voltage reference output. REF provides a 1.235-V (typical) reference and may be used to drive the REF input of the TLC34058.
$\overline{\text{RESET}}$	4	I (TTL compatible)	Reset control input. Following the first rising edge of LD/4 after the rising edge of $\overline{\text{RESET}}$, CLOCK and $\overline{\text{CLOCK}}$ are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and $\overline{\text{CLOCK}}$ outputs are set to be free running. Care must be taken to avoid glitches on this edge-triggered input.
V_{CC}	5, 6		Device power. V_{CC} terminals must be connected.

Table 1. Selection of Division Factor

DIV1	DIV0	DIVISION FACTOR	CLOCK CYCLES	
			LDx LOW	LDx HIGH
L	L	3	1	2
L	H	4	2	2
H	L	5	2	3
H	H	8	4	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TTL	2			
Low-level input voltage, V_{IL}	TTL			0.8	
High-level input voltage, V_{IH}	PECL‡	$V_{CC}-1.1$		$V_{CC}-0.8$	
Low-level input voltage, V_{IL}	PECL‡			$V_{CC}-1.5$	
High-level output current, I_{OH}	TTL			−2	mA
Low-level output current, I_{OL}	TTL			12	
Output current, I_O	PECL			30	
Input frequency, f_{OSC}		0		135	MHz
Pulse duration, $\overline{RESET}$ low, $t_{w(RL)}$	See Figure 1	15			ns
Setup time, $\overline{RESET}\uparrow$ before LD/4↑, $t_{su(R)}$	See Figure 1	10			
Setup time, ENABLE(S) before LDA↑, $t_{su(ES)}$	See Figure 1	10			
Hold time, ENABLE(S) after LDA↑, $t_{h(ES)}$	See Figure 1	0			
Setup time, ENABLE(A) before LDA↑, $t_{su(EA)}$	See Figure 1	10			
Hold time, ENABLE(A) after LDA↑, $t_{h(EA)}$	See Figure 1	0			
Input duty ratio		40%	50%	60%	
Operating free-air temperature, T_A		0		70	°C

‡ Pseudo-ECL

electrical characteristics V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	TTL	V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	TTL	V_{CC} = 5 V ±5%,	I_{OH} = −2 mA	2.4			
V_{OL}	Low-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OL} = 12 mA		0.3	0.5	
V_{OH}	High-level output voltage	PECL	Connected V_{CC}−2 V through 50 Ω		$V_{CC}-1$		$V_{CC}-0.8$	
V_{OL}	Low-level output voltage	PECL	Connected V_{CC}−2 V through 50 Ω		$V_{CC}-2$		$V_{CC}-1.6$	
I_I	Input current	TTL	V_{CC} = 5.25 V,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current	TTL	V_{CC} = 5.25 V,	$V_{I(TTL)}$ = 2.7 V			20	µA
I_{IL}	Low-level input current	TTL	V_{CC} = 5.25 V,	$V_{I(TTL)}$ = 0.4 V			−0.2	mA
I_{IH}	High-level input current	PECL	$V_{I(PECL)}$ = 4 V				15	µA
I_{IL}	Low-level input current	PECL	$V_{I(PECL)}$ = 0.4 V				15	µA
I_{OS}	Short-circuit output current	TTL	V_{CC} = 5.25 V,	V_O = 0 V	−40	−65	−100	mA
V_{ref}	Reference voltage		I_{ref} = −100 µA		1.2	1.235	1.26	V
I_{CC}	Supply current (see Note 1)					60	80	mA

NOTE 1: Does not include output part

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock(max)}$	Maximum clock frequency		135			MHz
$t_{pd(OH-LDALH)}$	Propagation delay time, OSC high to LDA↑	See Figure 1		9	15	ns
t_{sk}	Skew time	LDA to LDB	−2	0	2	ns
		LDA to LDC	−1	1.5	4	
		LDA to LD/2	0	1.5	5	
		LDA to LD/4	0	2	6	
		LDC to LDD	−2	0	2	

PARAMETER MEASUREMENT INFORMATION

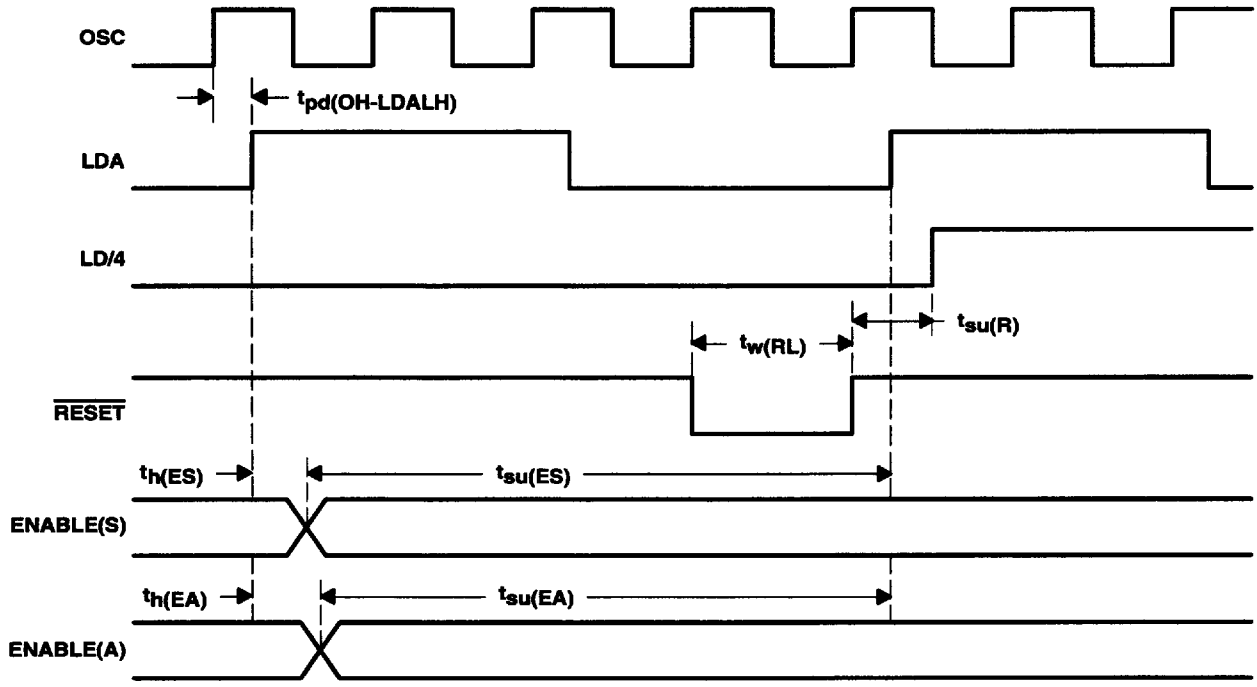
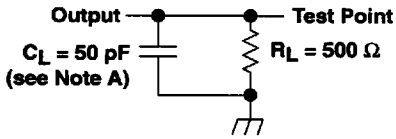


Figure 1. Timing Diagram

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 2. TTL Output Load Circuit

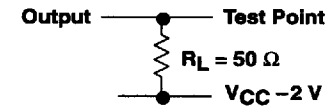


Figure 3. PECL Output Load Circuit

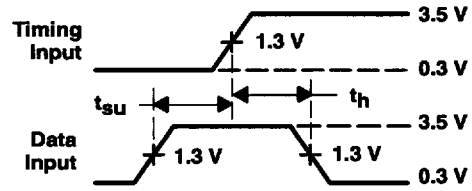


Figure 4. Setup Time and Hold Time

PRINCIPLES OF OPERATION

The TVP2002 is designed to interface to a 10KH-ECL crystal oscillator and generate the clock signals required by the TLC34058 . The OSC and $\overline{\text{OSC}}$ inputs are designed to interface to a 10KH-ECL oscillator operating from a single 5-V power supply.

The CLOCK and $\overline{\text{CLOCK}}$ outputs are designed to interface directly to the CLOCK and $\overline{\text{CLOCK}}$ inputs of the TLC34058. The output levels are compatible with 10KH-ECL logic operating from a single 5-V power supply. DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by 3, 4, 5, or 8 to generate the LDA and LDB signals. LDA is also divided by 2 and 4 to generate the LD/2 and LD/4 signals, respectively.

ENABLE(S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. When ENABLE(S) is low, LDC and LDD are low. ENABLE(A) is used to asynchronously start and stop the LDC and LDD outputs. When ENABLE(A) is low, the LDC and LDD outputs remain in the state they are when the ENABLE(A) input goes low.

Both ENABLE(A) and ENABLE(S) should not be low simultaneously. If this occurs, synchronous control of LDC and LDD, via ENABLE(S), is not ensured.

When both ENABLE(S) and ENABLE(A) are high, LDC and LDD are free running and in phase with LDA and LDB. This architecture allows the shift registers of the VRAMs to be optionally nonclocked during the retrace intervals. Figure 5 illustrates the ENABLE implementation with the TVP2002, while Figure 6 shows the load output timing.

$\overline{\text{RESET}}$ is designed to enable the TVP2002 to set the pipeline delay of the TLC34058 to a specified number of clock cycles (the exact number is dependent on the TLC34058). Following the first rising edge of LD/4 after the rising edge of $\overline{\text{RESET}}$, the CLOCK and $\overline{\text{CLOCK}}$ outputs are stopped in the high and low states, respectively. At the next rising edge of LD4, the CLOCK and $\overline{\text{CLOCK}}$ outputs are restarted. Figure 7 shows the operation of the $\overline{\text{RESET}}$ input. The TVP2002 also generates a 1.235-V (typical) reference that may be used to drive the REF input of the TLC34058.

PRINCIPLES OF OPERATION

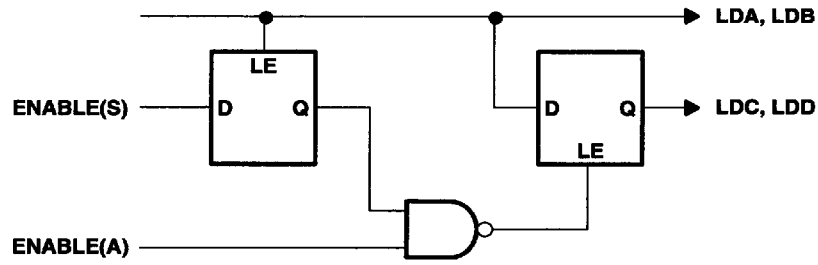


Figure 5. ENABLE Control

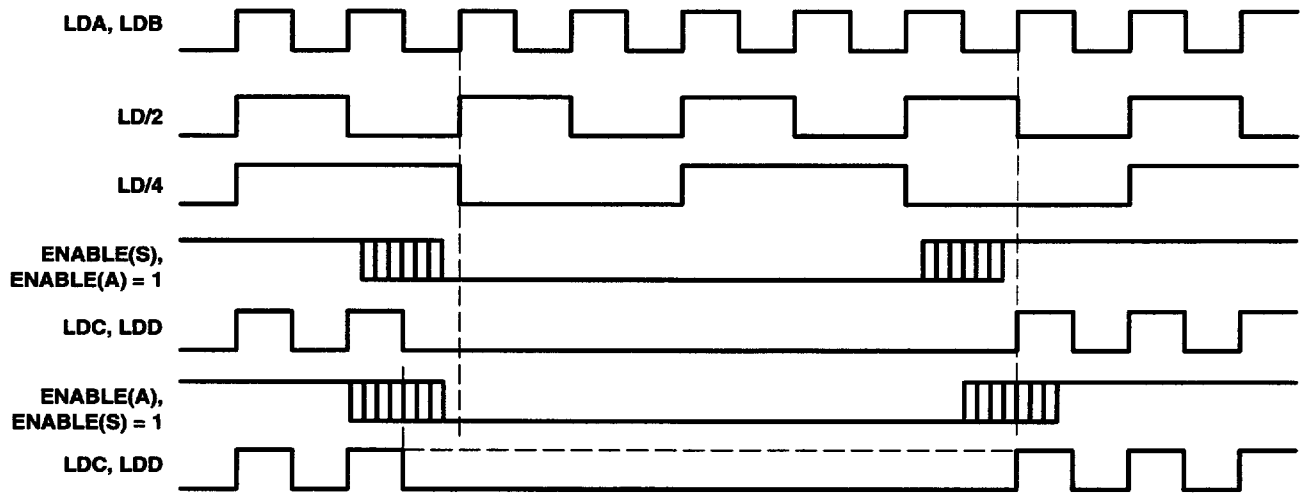


Figure 6. Load Output Timing

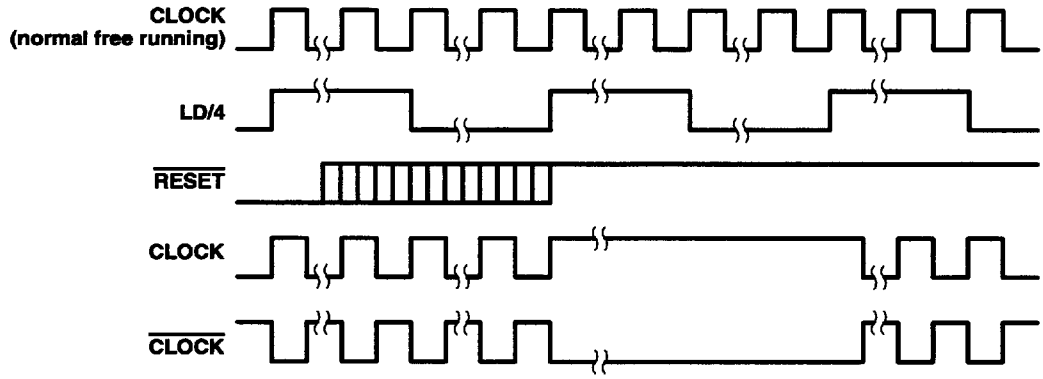


Figure 7. $\overline{\text{RESET}}$ Timing

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PRINCIPLES OF OPERATION

interfacing to the TLC34058 color palette

Figure 8 illustrates interfacing the TVP2002 to the TLC34058 when using a PECL oscillator. The TVP2002 should be located as close as possible to the TLC34058. The termination resistors for the CLOCK and $\overline{\text{CLOCK}}$ lines should be located as close as possible to the TLC34058.

The TVP2002 may drive the CLOCK and $\overline{\text{CLOCK}}$ inputs of the TLC34058 if they are located as close as possible to each other. Due to the inability to ensure proper synchronization between TVP2002s, multiple devices should not be used in applications where multiple color palettes drive the same monitor.

A 1-kΩ (typical) resistor must be used to isolate the REF output of the TVP2002 from the REF input of the TLC34058. This prevents noise from the TVP2002 voltage reference from being coupled onto the TLC34058 REF terminal. The REF input of the color palette must still have a decoupling capacitor connected to V_{CC} as specified in the TLC34058 data sheet.

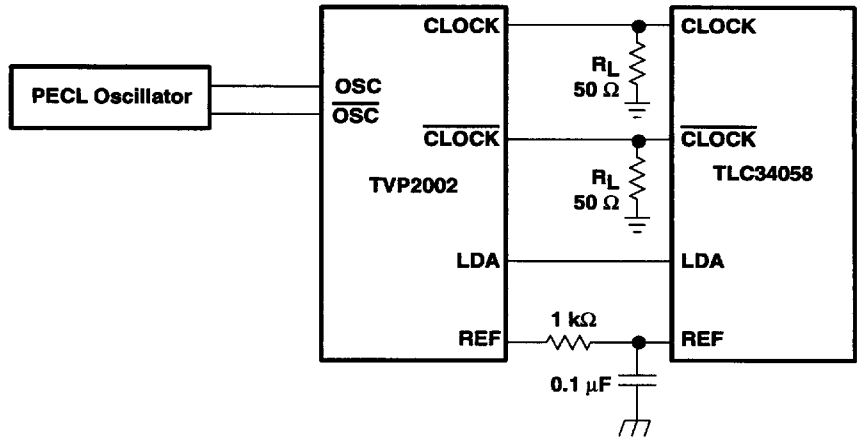


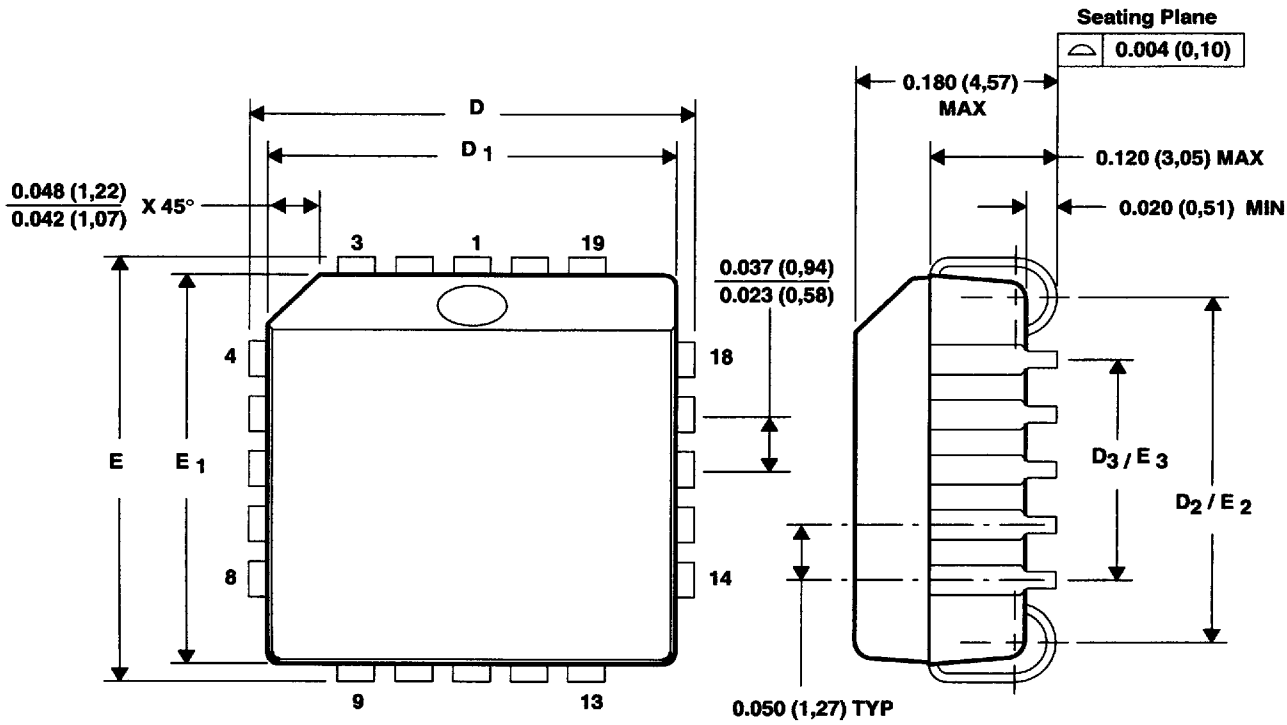
Figure 8. Interfacing the TVP2002 to a PECL Oscillator

MECHANICAL DATA

FN/S-PQCC-J**

PLASTIC J-LEADED CHIP CARRIER

20-PIN SHOWN



JEDEC OUTLINE	NO. OF PINS**	D / E		D1 / E1		D2 / E2		D3 / E3
		MIN	MAX	MIN	MAX	MIN	MAX	TYP
MO-047AA	20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.290 (7,34)	0.330 (8,38)	0.200 (5,08)
MO-047AB	28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.390 (9,91)	0.430 (10,92)	0.300 (7,62)
MO-047AC	44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.590 (14,99)	0.630 (16,00)	0.500 (12,70)
MO-047AD	52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.690 (17,53)	0.730 (18,54)	0.600 (15,24)
MO-047AE	68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.890 (22,61)	0.930 (23,62)	0.800 (20,32)
MO-047AF	84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	1.090 (27,69)	1.130 (28,70)	1.000 (25,40)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-047.