TVGA8900D DATA SHEET

Trident

TVGA8900D SUPER VGA CONTROLLER

Overview

- Single-chip solution for IBM PC/AT and compatible, PS/2 and compatible
- Built-in data bus transceiver and feature connector support
- Only one 32Kb EPROM required to achieve 16-bit BIOS operation speed
- Fully hardware compatible with VGA, EGA, CGA, MDA, and Hercules at the register level
- Programmable DRAM timing
- Supports 256Kx4, 256Kx8, 256Kx16, 512Kx4 and 512Kx8 DRAM chips
- Requires only two 256Kx4 DRAM chips for VGA solution
- Supports up to 1 MB of DRAM
- Supports 640x400, 640x480, 800x600, 1024x768 (interlaced or non-interlaced) in 256 colors
- Supports 800x600, 1024x768, and 768x1024 (interlaced or non-interlaced) in 16 colors
- Supports 640x400, 640x480, and 800x600 in 32K/64K colors (Trident's TKD8001 or other 15/16-bit DAC required)
- Supports 640x480 16M color mode (Trident's TKD8001 or other 24-bit DAC required)
- Supports 1024x768x256 72Hz non-interlaced
- Supports 70Hz refresh at 800x600 and 1024x768
- Supports Edsun CEG™ DAC
- Zero-wait state ISA bus performance
- Supports linear addressing
- Supports 80/132-column text in 25, 30, 43, or 60 rows
- High-resolution drivers available
- 0.8 µm low power CMOS technology
- 160 pin PFP package

General Description

The TVGA8900D is the successor to the popular TVGA8900CL and TVGA8900C. The TVGA8900D is a highly integrated and cost effective solution for high performance VGA (Video Graphics Array) systems. The built-in data bus transceiver and feature connector support mean a minimum motherboard solution can be achieved with only three support chips: the TKD8001 Truecolor DAC/clock chip, and two pieces 256Kx4 DRAM. Programmable DRAM timing allows the designer to choose either slower speed DRAM for a cost saving solution or faster speed DRAM for high speed performance. Display support for Super VGA, VGA, EGA, CGA, and MDA monitors assures TVGA8900D solutions can be matched up with virtually any monitor on the market.

The TVGA8900D also provides improved speed over the TVGA8900CL and TVGA8900C. This is achieved by zero-wait state direct memory write ISA bus performance, faster base DRAM clock (48MHz), and 1 MB linear addressing. The linear addressing eliminates memory bank switching and increases the speed for software that accesses more than 256K of memory.

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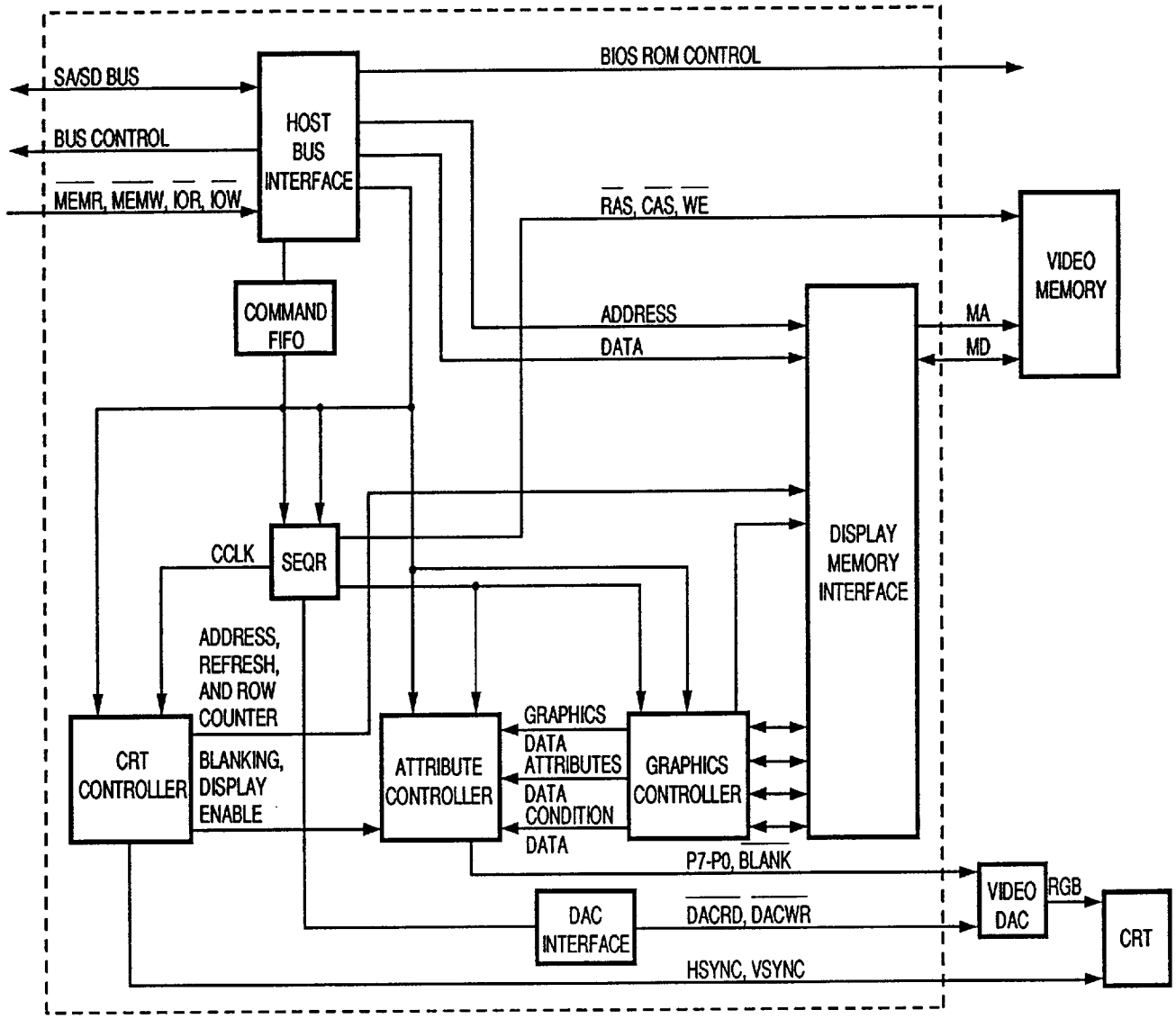

Figure 1. TVGA8900D Functional Block Diagram

Compatibility

The TVGA8900D is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes, and allows:

- Use of application software that uses any of the above modes
- Emulation of EGA, CGA, MDA, and Hercules modes on a VGA monitor

Extended Graphics and Text Modes

Extended graphics modes supported include:

- 640x400, 640x480, and 800x600 in 32K or 64K colors
- 640x480 in 16M colors
- 640x400, 640x480, 800x600, and1024x768 (interlaced or non-interlaced) in 256 colors from a palette of 256K colors (with 6-bit DAC) or 16M colors (with 8-bit DAC)
- 800x600, 768x1024, and 1024x768 (interlaced or non-interlaced) and 1280x1024 (interlaced) in 16 colors out of 256K/16M
- 1024x768 in 4 colors out of 256K/16M
- Extended text modes offer 80-column text with 30, 43 , and 60 rows; and 132-column text with 25, 30, 43, and 60 rows

Hardware Features

The TVGA8900D supports PC/AT bus and PS/2 Micro Channel bus and offers speed improvement and flexible memory type selections over the TVGA8900CL.

The support of pseudo 16-bit ROM operation in TVGA8900D means high performance can be achieved using a single ROM chip. A single ROM solution helps minimize the number of chips required for VGA implemention.
The chip allows programmable DRAM timing and supports 256Kx4, 256Kx8, 256Kx16, 512Kx4 and 512Kx8 DRAM. Table 1 outlines the amount and speed of Fast Page Mode 256Kx4 DRAM required to implement the 16-, 256-, 32K-, and 16M-color modes. For other types of DRAM, typically 80ns speed is required.

Table 1. 16, 256, 32K, and 16M-Color DRAM Requirements

	Colors				DRAM Count			Speed ns	
Resolution	16	256	32K[1]	16M	2	4	8	100	80
Standard VGA	•				•				•
640x480		•				•			•
640x480			•			•		•	
640x480				•					•
800x600	•				•				•
800x600		•					•	•	
800x600			•				•		•
1024x768 (Interlaced)	•					•		•	
1024x768 (Non-interlaced)	•					•			•
1024x768 (Interlaced)		•					•	•	
1024x768 (Non-interlaced)		•					•		•
1280x1024 (Interlaced)	•						•		•

[1]Same DRAM requirement for 64K color

A CPU command FIFO allows zero-wait state performance on the PC/AT and MCA bus. On the display side, base DRAM clock speed has improved and linear addressing eliminates bank switching overhead for all display resolutions.

Software Drivers Supported

The TVGA8900D is compatible with all drivers currently available for the TVGA8900CL. The following applications are supported:

- AutoCAD
- Autoshade
- CADKEY
- Framework
- GEM
- Lotus
- MS Windows
- MS Word
- P-CAD
- Symphony
- Ventura
- VersaCAD
- WordPerfect
- Wordstar
- OS/2
- SCO X-Windows (contact SCO)
- Edsun CEG™ (Windows, Lotus, ACAD)

Contact Trident for the latest high-resolution driver releases.

TVGA8900D Applications

The TVGA8900D works with your hardware allowing you to develop a high-end or low-end system. You can use Trident's DAC/clock chip, the TKD8001, to select up to 16 different clock frequencies. Such frequency selection ability allows you to implement specific applications such as support for high-resolution analog VGA monitors, fixed-frequency VGA monitors, and EGA, CGA, MDA, and Hercules monitors. The TVGA8900D allows you to divide clock input frequencies by one and one half, two, or four. Four chips signals (SC1, SC2, SC3, and SC4) can be programmed to select specific clock inputs for the TVGA8900D.

A minimum configuration requires a TVGA8900D, TKD8001 DAC/clock chip, two 256Kx4 DRAM chips, 32KB EPROM, 15-pin connector, 14.318MHz crystal, jumpers, and miscellaneous ferrite beads, capacitors, resistors.

TVGA8900D Components

The TVGA8900D consists of eight major components: Sequencer, CRT Controller, Graphics Controller, Attribute Controller, DAC Support Logic, Host Bus Interface, Display Memory Bus Interface and Command FIFO. These components are used to generate video output and timing for video memory and the monitor. See Figure 1 on page 2 for the TVGA8900D Functional Block Diagram.

Sequencer

The sequencer provides basic memory timing for DRAM interfacing, and a character clock for the CRTC and for controlling regenerative memory fetch. The sequencer uses a 32 byte video cache to let the CPU access display memory during active display intervals. Video data from the cache can be output to the video screen while the CPU accesses video memory. This greatly increases performance over standard implementations for CPU access.

CRT Controller

The CRT (Cathode Ray Tube) Controller provides complete control for horizontal and vertical synchronous timing, address interface between video memory and display screen, cursor and underline timing, and refresh addressing for dynamic RAMs.

Graphics Controller

During the active display interval, the Graphics Controller directs data from video memory to the Attribute Controller. In graphics modes, memory data is formatted into serialized form and sent to the Attribute Controller in 4-bit plane format. In text mode, the parallel attribute byte goes directly to the Attribute Controller without going through the Graphics Controller. During video memory read/write operations, the Graphics Controller acts as an interface to the CPU. The Graphics Controller can perform logic operations on memory data before it reaches the display memory or system data bus.

Attribute Controller

The Attribute Controller takes in data from video memory and formats it for output on the display monitor. In addition, the Attribute Controller takes care of blinking, underlining, cursor insertion, and PEL panning. In text mode, 16 bits of code are divided into 8 bits of character code and 8 bits of attribute code. The character code is used as a look-up into a font table. The attribute code is used to determine character color, blinking, bold, etc. In graphics mode, the Graphics Controller serializes memory bits. Each output color is translated through the internal color palettes and then sent to the Video DAC. Here it is used as an address to the 18/24-bit color look-up table. The value read from the color look-up table is converted into three analog signals (R, G, B) for driving an analog display.

DAC Support Logic

To simplify the chip hardware design, the TVGA8900D provides a pixel clock and DAC write, DAC read, and blank signals to an off-chip color look-up table/DAC. See Figure 7-A and 7-B for diagrams of standard applications (page 14 and 15). 15/16-bit color and true color DACs are supported.

Host Bus Interface

The TVGA8900D supports the PC/AT bus and the Micro Channel bus by setting or resetting configuration bits MD4 during the system reset time. When the TVGA8900D is part of a Micro Channel board solution, several host bus interface pins are defined or designated differently from a PC/AT solution. Reference Table 10 for details.

The TVGA8900D video ROM is located at C0000-C7FFF. The PROM data width can be configured as 16-bit or 8-bit at system reset time by pulling MD7 high or low, respectively. If the 16-bit mode is turned on, the TVGA8900D will return $\overline{\text{MCS16}}$ when the PROM is addressed. If the on-board BIOS is not used, the ROM chip(s) can be disabled by pulling MD6 low at system reset time.

The TVGA8900D can address up to 1MB of video memory depending on the mode (text or graphics). After system reset the TVGA8900D is configured for an 8-bit data width for video memory access. The 16-bit-wide data bus can be activated automatically by ROM. The TVGA8900D will drive $\overline{\text{MCS16}}$ when the 16-bit mode is set and video memory is accessed.

In order to comply with the Micro Channel specifications, the TVGA8900D supports channel ID (I/O address 100 and 101) as well as the card-enable control bit (bit 0 of I/O port 102). When the video memory or on-board I/O registers are accessed, the TVGA8900D responds with $\overline{\text{CD SFDBK}}$. $\overline{\text{CD SFDBK}}$ is generated by decoding the following address groups with a read/write command:

I/O Read/Write:

- 3BX - excluding 3B6, 3B7, 3BC, 3BD, and 3BX. For monochrome mode only.
- 3DX - excluding 3D6, 3D7, 3DE, and 3DF. For color mode only.
- 3CX - excluding 3CA, 3CB, and 3CD.

Memory Read/Write:

- $\overline{\text{ROMCS}}$ - on-board BIOS EPROM address from C0000 to C7FFF.
- $\overline{\text{MEMR/W}}$ - default display memory address space.

Since there is only the decoding delay for generation of $\overline{\text{CD SFDBK}}$, the signal will look very much like that of a system read/write command.

Display Memory Bus Interface

The TVGA8900D provides a bus interface for the video display DRAM. The interface provides address multiplexing, data multiplexing, refresh, and RAS, CAS, and write-enable signals. Nineteen address pins (MA9, MAA8-MAA0 and MAB8-MAB0 for Bank A and B) and 32 data pins (MD31-MD0) are available for display memory.

Command FIFO

The FIFO enhances the memory write performance. CPU write data is stored in the FIFO without being written into memory so the CPU does not have to wait when the video interface is busy. When the memory bus is available, data is written into memory from the FIFO.

MD & RMD Definitions at System Reset

Tables 2 through 4 list values and definitions for MD29-MD16, MD7-MD0 and RMD7-RMD0 at system reset.

Table 2. MD29-MD16 Definitions

MD	Logic Value[1]	Definition
MD29	-	Default logic value 1
MD28	0	Pins $\overline{WE3}$-$\overline{WE0}$ defined as $\overline{CASA3}$-$\overline{CASA0}$. Pin $\overline{CASA}$ defined as $\overline{WE}$
	1	Default
MD27-MD24	NA	Sets base address of the linear address window
MD23	0	Enables true color mode
	1	Disables true color mode
MD22	NA	Reserved
MD21	0	Reserved
	1	ISA/MCA bus
MD20	NA	Reserved
MD19-MD18	00	Supports 256Kx16 DRAM. Pin 158 is not used
	01	Supports 512Kx8 DRAM. Pin 158 is used as MA9
	10	Reserved
	11	Supports 256Kx4 or 256Kx8 DRAM up to 1MB. Pin 158 is used as $\overline{NMI}$.
MD17	0	Selects LA23-20
	1	Selects SA19-17, $\overline{HAD}$
MD16	0	8-bit ISA bus
	1	16-bit ISA bus
MD15	NA	Reserved

[1]No pull-up resistor required to set a Logical 1 value. Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor.

Table 3. MD7-MD0 Definitions

MD	Logic Value[1]	Definition
MD7	0	8-bit BIOS
	1	16-bit BIOS
MD6	0	ROM disabled
	1	ROM enabled
MD5	0	I/O port at 2xx
	1	I/O port at 3xx
MD4	0	MCA bus
	1	ISA bus
MD3-MD0		DIP switch settings[2]

[1]No pull-up resistor required to set a Logical 1 value. Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor.
[2]Data read into a 4-bit register. The data values can be used by the BIOS or application software.

Table 4. RMD7-RMD0 Definitions

RMD	Logic Value[1]	Definition
RMD7	0	8-bit video memory
	1	16-bit video memory
RMD6-RMD5	00	Reserved
	01	8-bit DRAM data bus
	10	16-bit DRAM data bus
	11	32-bit DRAM data bus
RMD4	0	Selects 46E8 for port control
	1	Selects 3C3 for port control
RMD3	0	24K BIOS
	1	32K BIOS
RMD2	1	Reserved
RMD1	0	Standard BIOS wait states
	1	Extended BIOS wait states
RMD0	0	Slow mode address detect
	1	Fast mode address detect

Chip Specifications

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typ.	Maximum	Units
Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_{IN}	GND		V_{DD}	V
Operating Temperature	T_{OP}	0		70	°C
Storage Temperature	T_{STO}	-40		100	°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

Table 6. DC Specifications

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Input Low Voltage	V_{IL}	GND	0.8	V	V_{DD}=5V
Input High Voltage	V_{IH}	2.0	V_{DD}	V	V_{DD}=5V
Input Low Current	I_{IL}	-	-0.5	µA	V_{IN}=0.0V
Input High Current	I_{IH}	-	20	µA	V_{IN}=V_{DD}
Output Low Voltage	V_{OL}	-	0.4	V	see Note 1
Output High Voltage	V_{OH}	2.4	-	V	see Note 1
High Impedence Leakage	I_{OZ}	-	10.0	µA	V_{SS}<V_{OUT}<V_{DD}
Supply Current	I_{OC}	-	100.0	mA	V_{DD}=5.25V (V_{DD} MAX.)

Note 1: I_{OL}/I_{OH} = 4/-4 mA for SC4-SC1, $\overline{ROMCS}$, EXTCLK, EXENPD, $\overline{DACRD}$, $\overline{DACWR}$, ESYNC, RS2-RS0. I_{OL}/I_{OH} = 6/-6 mA for MAA8-MAA0, MAB8-MAB0. I_{OL}/I_{OH}=8/-8 mA MD31-MD0, SD15-SD0, IREQ, P7-P0, VSYNC, HSYNC, $\overline{BLANK}$, $\overline{WE3}$-$\overline{WE0}$/$\overline{CAS3}$-$\overline{CAS0}$, PCLK. I_{OL}/I_{OH} = 16/-16 mA for $\overline{RAS}$, IOCHRDY, $\overline{NMI}$, $\overline{MCS16}$, $\overline{ZWS}$

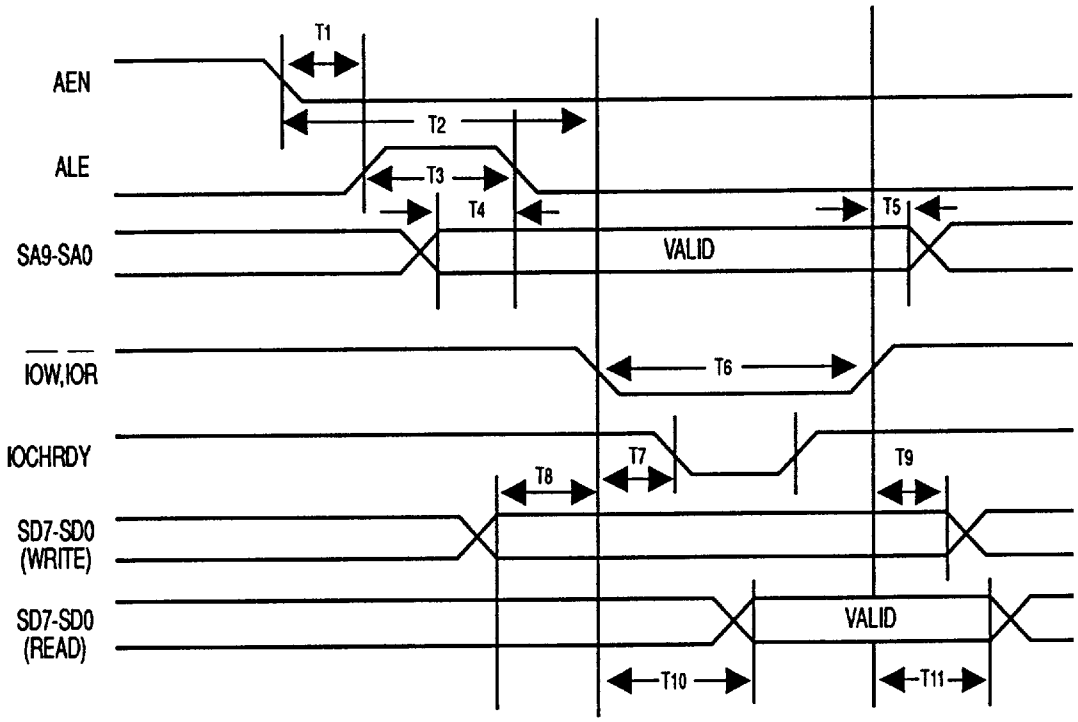

Figure 2. PC/AT ISA Bus I/O Read/Write Timing

Table 7. AC Specifications for ISA Bus I/O Read/Write in Nanoseconds

SYM	Description	Min	Typ	Max
T1	AEN Valid to Rising Edge of ALE	100		
T2	AEN Valid to I/O Command Active	5		
T3	ALE Active to Inactive	15.5		
T4	SA9-SA0 & $\overline{SBHE}$ Valid to Falling Edge of ALE	29.5		
T5	SA9-SA0 & $\overline{SBHE}$ Valid Hold From Command Inactive	18		
T6	I/O Command Active		60	
T7	IOCHRDY Inactive From Active Command	10		15
T8	Valid Write Data Setup to I/O Command Active	4.5		80
T9	Write Data Valid Hold From I/O Command Inactive	30		
T10	Read Data Valid From Read Command Active			60
T11	Read Command Inactive to SD7-SD0 Invalid			20

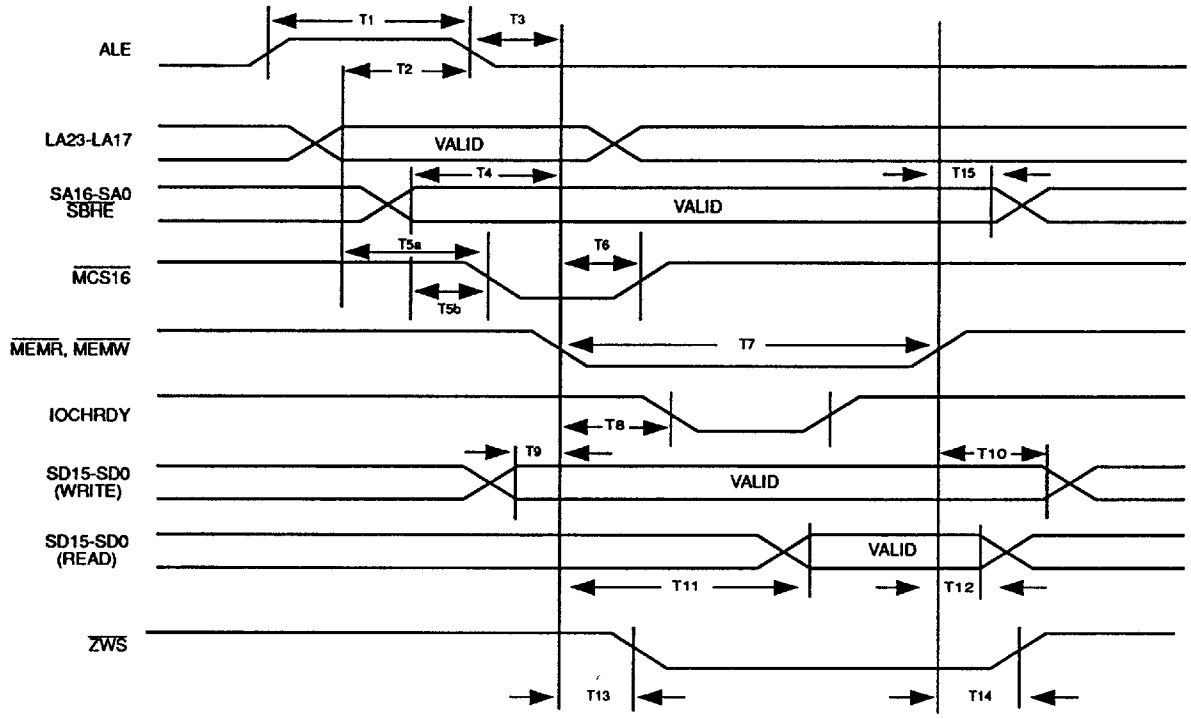

Figure 3. PC/AT ISA Bus Memory Read/Write Timing

Table 8. AC Specifications for ISA Bus Memory Read/Write in Nanoseconds

SYM	Description	Min	Typ	Max
T1	ALE Active to Inactive	15		
T2	LA23-LA17 Valid Setup to Falling Edge of ALE	20		
T3	ALE Inactive to Command Active	20		
T4	SA16-SA0 & $\overline{\text{SBHE}}$ Valid to Memory Command Active	5		
T5a	$\overline{\text{MCS16}}$ Active From Unlatched Address			20
T5b	$\overline{\text{MCS16}}$ Active From Latched Address			14
T6	$\overline{\text{MCS16}}$ Valid Hold From Invalid LA23-LA17			25
T7	Memory Command Active to Inactive	80		
T8	IOCHRDY Inactive From Memory Command Active	10		20
T9	Valid Write Data Setup to Memory Command Active	0		
T10	Write Data Valid Hold From Memory Command Inactive	10		
T11	Valid Read Data From Memory Command Active	0		
T12	Read Command Inactive to SD15-SD0 Invalid			20
T13	$\overline{\text{ZWS}}$ Active From Command Active	8		15
T14	$\overline{\text{ZWS}}$ Inactive From Command Inactive	10		15
T15	Latched Address Hold Time After Command	0		

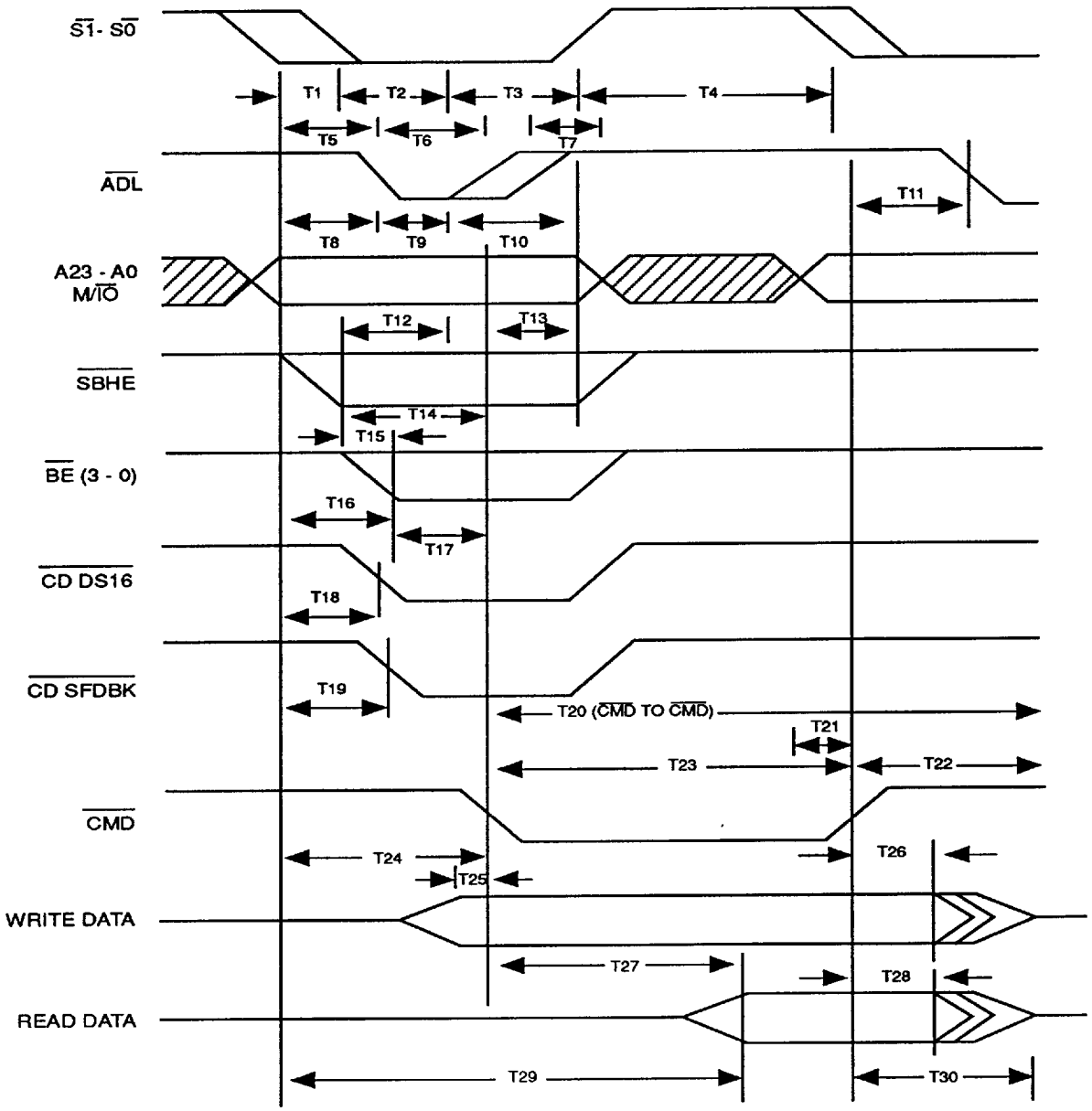

Figure 4. Micro Channel Bus Timing

Table 9. AC Specifications for MCA Bus in Nanoseconds

SYM	Description	Min	Typ	Max
T1	Status Active From ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$	10		
T2	$\overline{CMD}$ Active From Status Active	55		
T3	Status Hold From $\overline{CMD}$ Active	30		
T4	Next Status Active From Status Inactive	30		
T5	$\overline{ADL}$ Active From ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$	45		
T6	$\overline{ADL}$ Active to $\overline{CMD}$ Active	40		
T7	ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$, $\overline{SBHE}$ hold from $\overline{ADL}$ Inactive	25		
T8	$\overline{ADL}$ Active from Status Active	12		
T9	$\overline{ADL}$ Active to Inactive	40		
T10	Status Hold From $\overline{ADL}$ Inactive	25		
T11	$\overline{CMD}$ Inactive to next $\overline{ADL}$ Active	40		
T12	$\overline{SBHE}$ Setup to $\overline{ADL}$ Inactive	40		
T13	ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$, $\overline{SBHE}$ Hold From $\overline{CMD}$ Active	30		
T14	$\overline{SBHE}$ Setup to $\overline{CMD}$ Active	40		
T15	$\overline{BE3}$-$\overline{BE0}$ Active From $\overline{SBHE}$, A0, A1 Active			30
T17	$\overline{BE3}$-$\overline{BE0}$ Active to $\overline{CMD}$ Active	10		
T18	$\overline{CD\ DS\ 16}$ Active (n) From ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$ Valid			55
T19	$\overline{CD\ SFDBK}$ Active From ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$ Valid		60	
T20	$\overline{CMD}$ Active to Next $\overline{CMD}$ Active	190		
T21	Next Status Active to $\overline{CMD}$ Inactive		20	
T22	$\overline{CMD}$ Inactive to Next $\overline{CMD}$ Active	80		
T23	$\overline{CMD}$ Active to Inactive	90		
T24	$\overline{CMD}$ Active From Address Valid	85		
T25	Write Data Setup to $\overline{CMD}$ Active	0		
T26	Write Data Hold From $\overline{CMD}$ Inactive	30		
T27	Read Data Valid From $\overline{CMD}$ Active		60	
T28	Read Data Hold From $\overline{CMD}$ Inactive		0	
T29	Status to Read Data Valid			125
T30	Read Data Bus Tri-state From $\overline{CMD}$ Inactive			40

Table 10. Vertical and Horizontal Timing

Mode	CLK (MHz)	Type	Display	Max Colors	VERTICAL T1	T2	T3	T4	CLK T5	Polarity	MAX T6	T7	T8	T9	T10	T11	Polarity
0,1	25.2	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2,3	25.2	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
0*,1*	25.2	A/N	40x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
2*,3*	25.2	A/N	80x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
0+,1+	28.3	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2+,3+	28.3	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
4,5	25.2	APA	320x200	4	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
6	25.2	APA	640x200	2	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
7	28.3	A/N	80x25	Mono	3.146	11.122	1.208	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
7+	28.3	A/N	80x25	Mono	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
D	25.2	APA	320x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
E	25.2	APA	640x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
F	25.2	APA	640x350	Mono	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
10	25.2	APA	640x350	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
11	25.2	APA	640x480	2	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
12	25.2	APA	640x480	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
13	25.2	APA	320x200	256	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.477	2.066	3.813	31.778	-
50	25.2	A/N	80x30	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
51	25.2	A/N	80x43	16	1.652	15.031	0.540	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
52	25.2	A/N	80x60	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
53	40.0	A/N	132x25	16	3.168	11.200	1.248	14.368	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	+
54	40.0	A/N	132x30	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
55	40.0	A/N	132x43	16	1.600	15.136	0.576	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
56	40.0	A/N	132x60	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
57	44.9	A/N	132x25	16	3.079	11.225	1.219	14.304	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	+
58	44.9	A/N	132x30	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
59	44.9	A/N	132x43	16	1.539	15.170	0.417	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5A	44.9	A/N	132x60	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5B	36.0	APA	800x600	16	0.711	17.067	0.028	17.715	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5B	50.35	APA	800x600	16	1.395	12.489	0.479	13.883	0.125	+	4.926	15.889	0.794	2.066	2.066	20.814	+
5C	50.35	APA	640x400	256	1.557	12.711	0.413	14.268	0.064	+	6.356	25.422	0.556	1.668	4.131	31.778	-
5C	25.2	APA	640x400	256	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
5D	50.35	APA	640x480	256	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.556	1.668	4.131	31.778	-
5D[1]	25.2	APA	640x480	256	1.430	12.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
5E	72.0	APA	800x600 (I)	256	0.711	17.067	0.028	17.778	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5E[1]	36.0	APA	800x600 (NI)	256	0.711	17.067	0.028	17.778	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5E[2]	50.3	APA	800x600 (NI)	256	1.395	12.489	0.479	13.883	0.125	+	4.926	15.889	0.794	2.066	2.066	20.814	+
5F[1]	44.9	APA	1024x768 (I)	16	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	0.204	1.260	3.956	28.151	+
5F	65.0	APA	1024x768 (NI)	16	0.945	15.785	0.329	16.731	0.041	+	4.800	15.754	0.615	1.108	3.077	20.554	+
5F[2]	75.0	APA	1024x768	16	0.673	13.599	0.053	14.272	0.106	+	4.053	13.653	0.320	1.920	1.813	17.707	+
60	44.9	APA	1024x768(I)	4	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	1.069	1.782	2.494	28.151	+
61	44.9	APA	768x1024 (I)	16	0.791	13.501	0.119	14.292	0.040	+	9.265	17.105	-1.782	4.633	4.811	26.370	+
62	44.9	APA	1024x768 (I)	256	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	-.178	2.851	2.316	28.151	+
62	65.0	APA	1024x768 (NI)	256	0.945	15.785	0.329	16.731	0.041	+	4.800	15.754	0.615	1.108	3.077	20.554	+
62[2]	75.0	APA	1024x768	256	0.673	13.599	0.053	14.272	0.106	+	4.053	13.653	0.320	1.920	1.813	17.707	+
63	75.0	APA	1280x1024	16	1.120	10.705	0.379	11.835	0.084	+	3.765	17.035	0.255	0.205	3.400	21.000	+
6C	75.0	APA	640x480	16M	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
70/71	77.0	APA	512x480	32/64K	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
74/75	50.35	APA	640x480	32/64K	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
76/77	72.0	APA	800x600	32/64K	0.711	17.067	0.028	17.715	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-

[1]Same timing for 32K and 64K color modes

[2]Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801

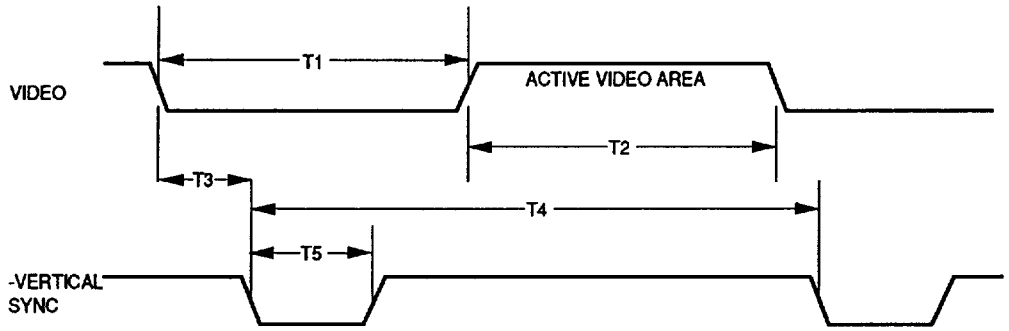

Figure 5-A. Vertical Timing (ms)

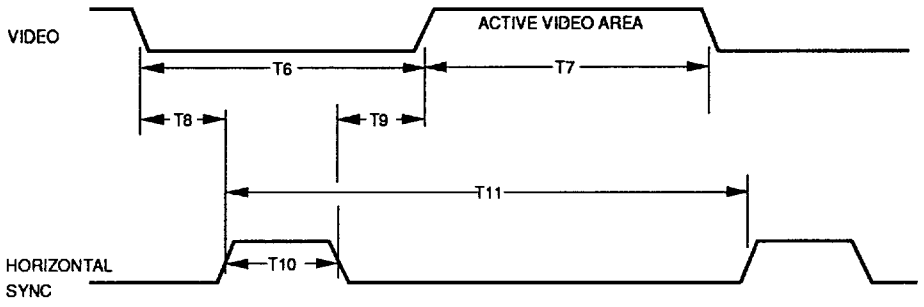

Figure 5-B. Horizontal Timing (μs)

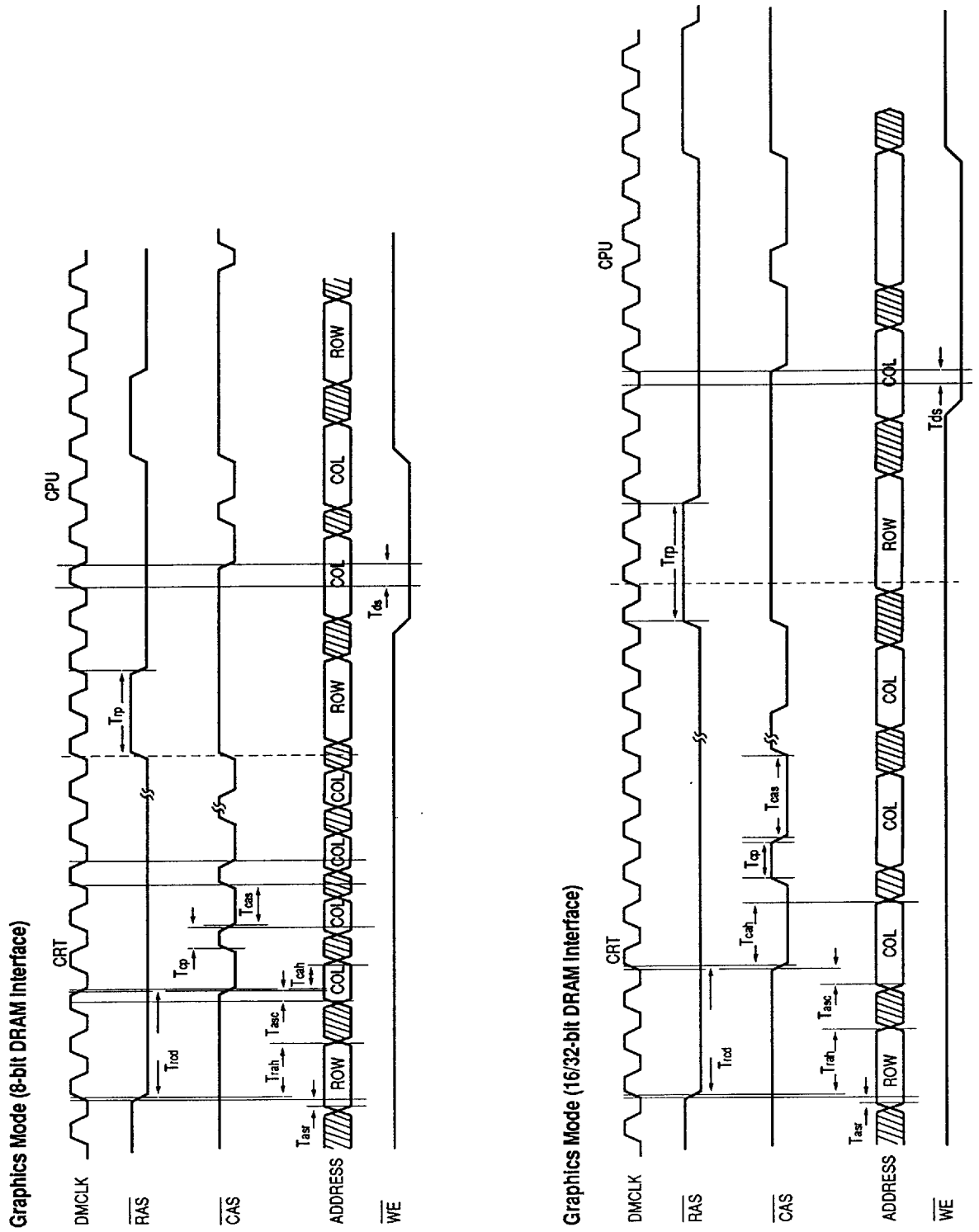

Figure 6-A. Trident TVGA8900D DRAM Timing (Graphics)

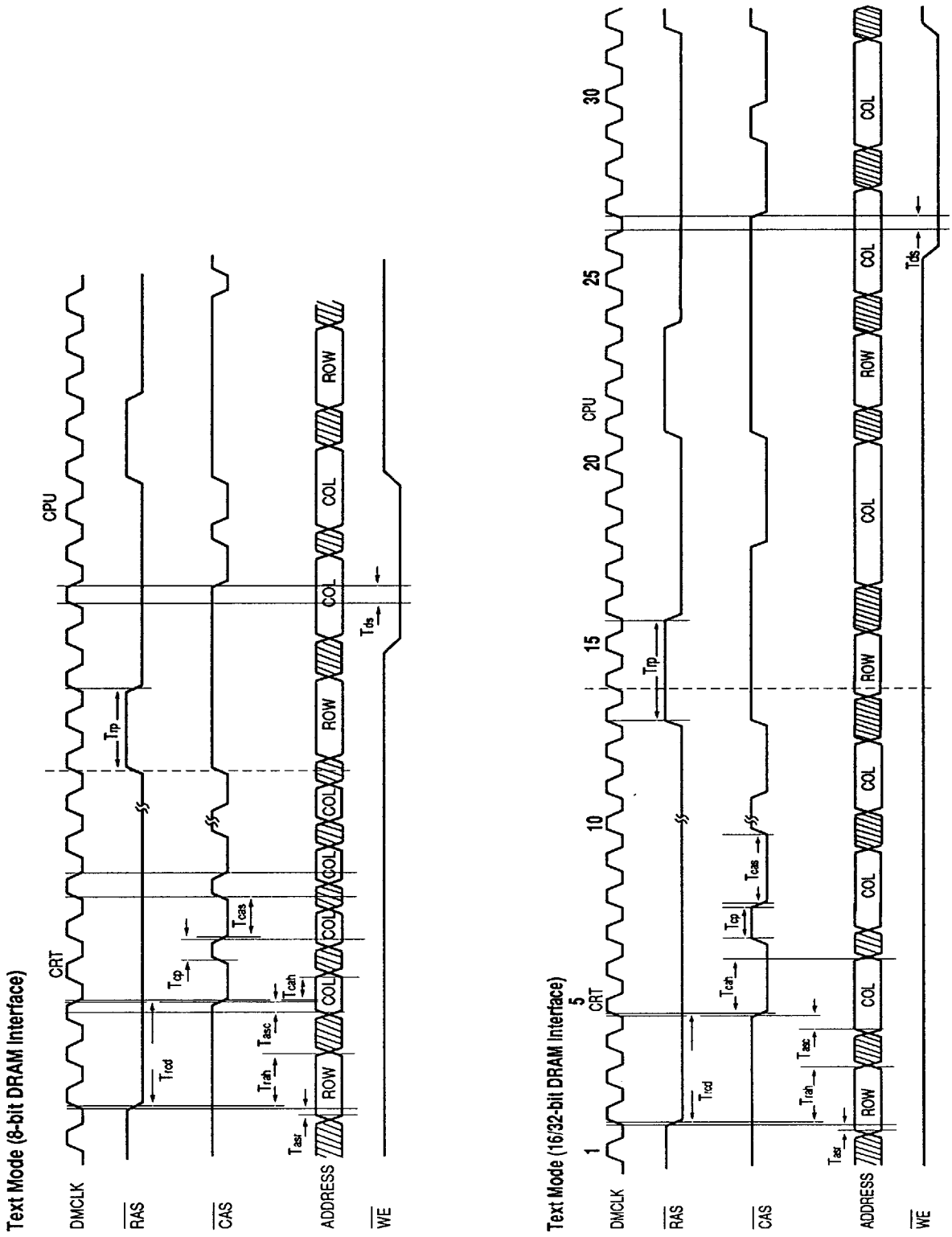

Figure 6-B. Trident TVGA8900D DRAM Timing (Text)

Table 11. Worst Case Memory Timing Parameters[1]

Parameter	8 bit DRAM Interface	16 bit DRAM Interfeace	32 bit DRAM Interface
Trcd 1	2.5t + 1.5ns	3t + 1.5ns	3t + 3ns
Trah 2	1.5t + 2ns	2t + 2ns	2t + 2ns
Tasr 3	≥ 0	≥ 0	≥ 0
Tasc 4	≥ 0.5t	≥ t	≥ t
Tcah 5	t	2t	2t
Tcp 6	0.5t - 2.5ns	t - 5ns	t - 6ns
Tcas 7	t - 4ns	2t - 6.5ns	2t - 10ns
Tds 8	≥ 0	≥ 0	≥ 0
Trp 9	2t - 1.5ns	3t - 4ns	3t - 6ns
Test Load	25pf	50pf	85pf

*(t=1/DMCLK)

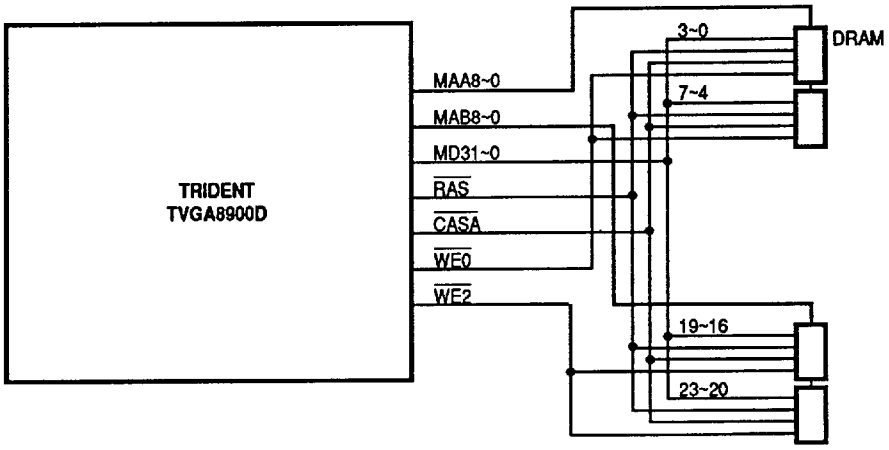

Figure 7-A. Application For Four 256Kx4 DRAM (ISA Bus)

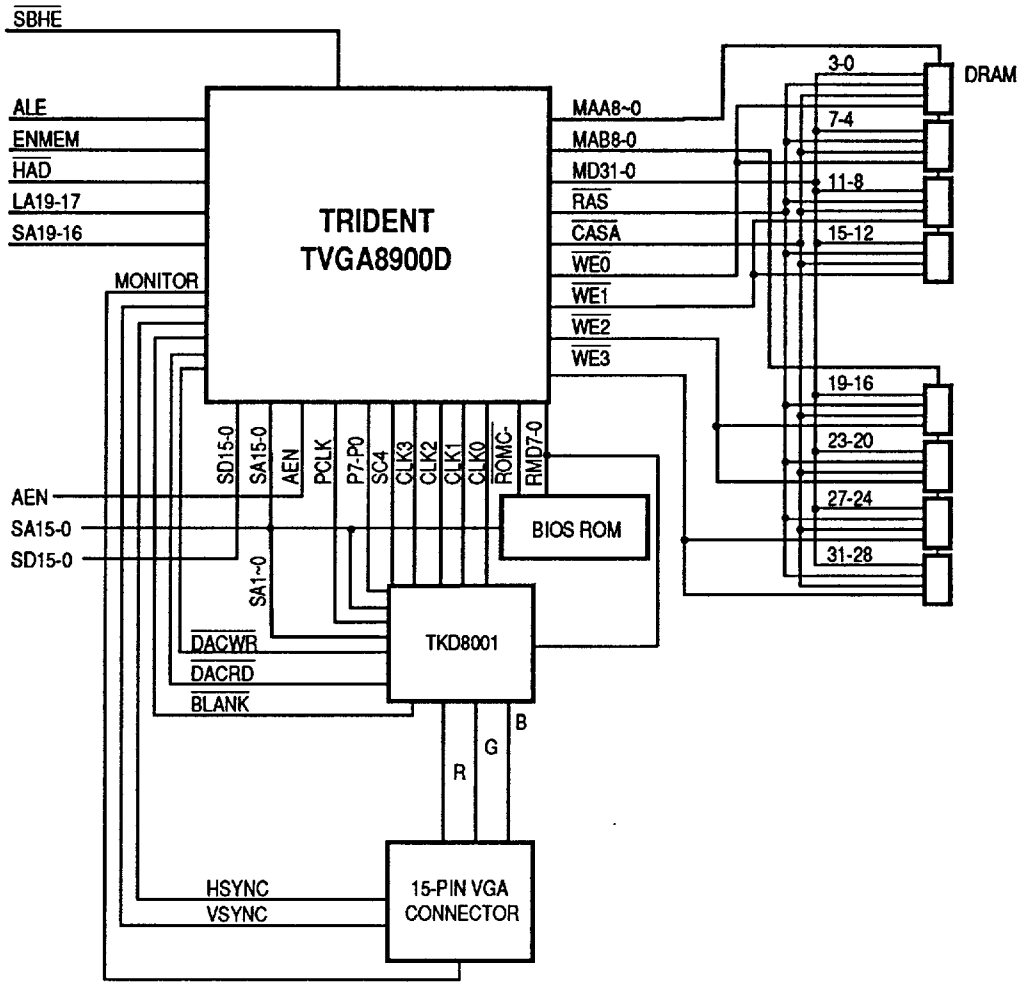

Figure 7-B. Application For Eight 256Kx4 DRAM (ISA Bus)

Trident

TVGA8900D DATA SHEET

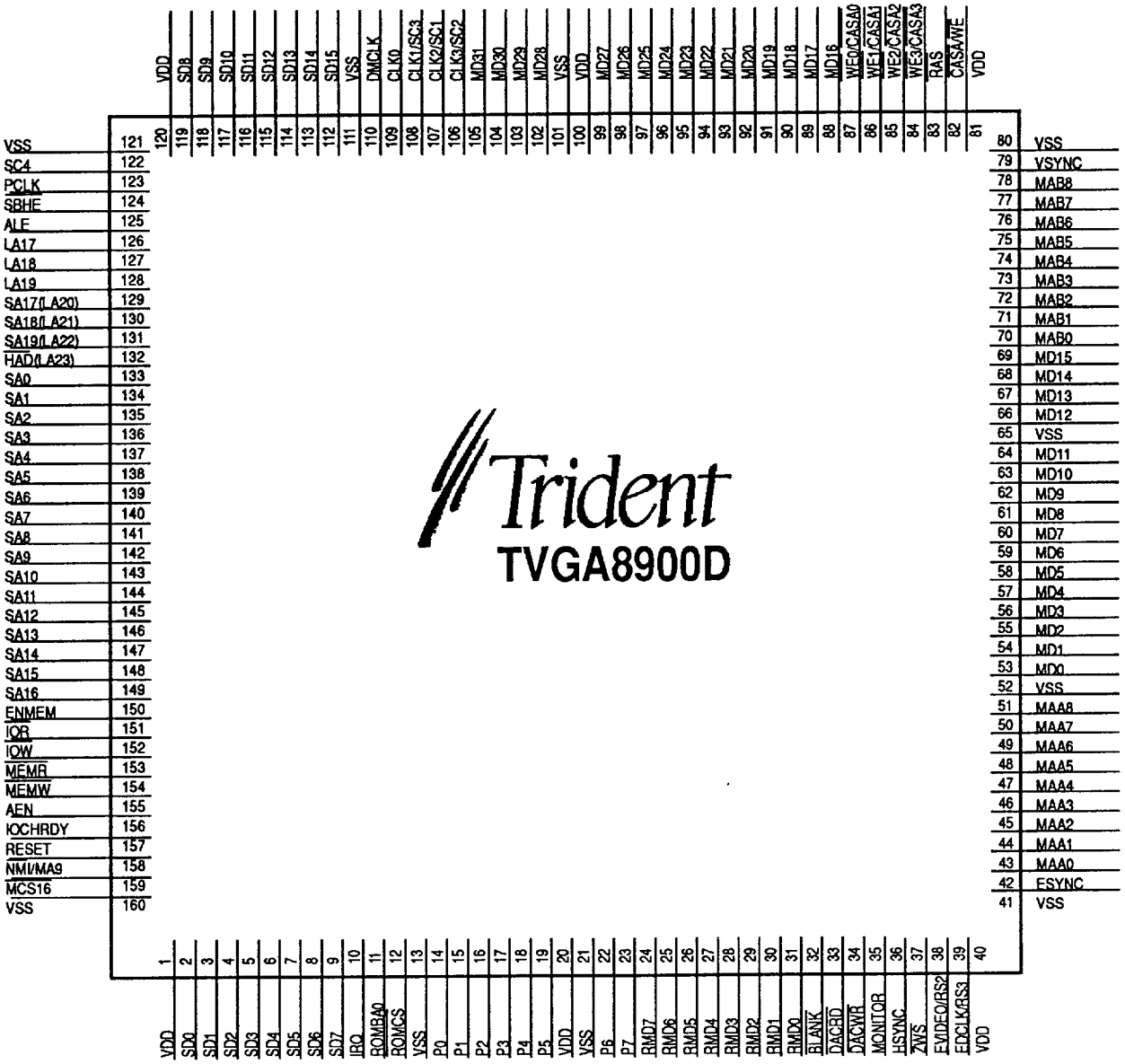

Figure 8-A. TVGA8900D Pin-Out (ISA Bus)

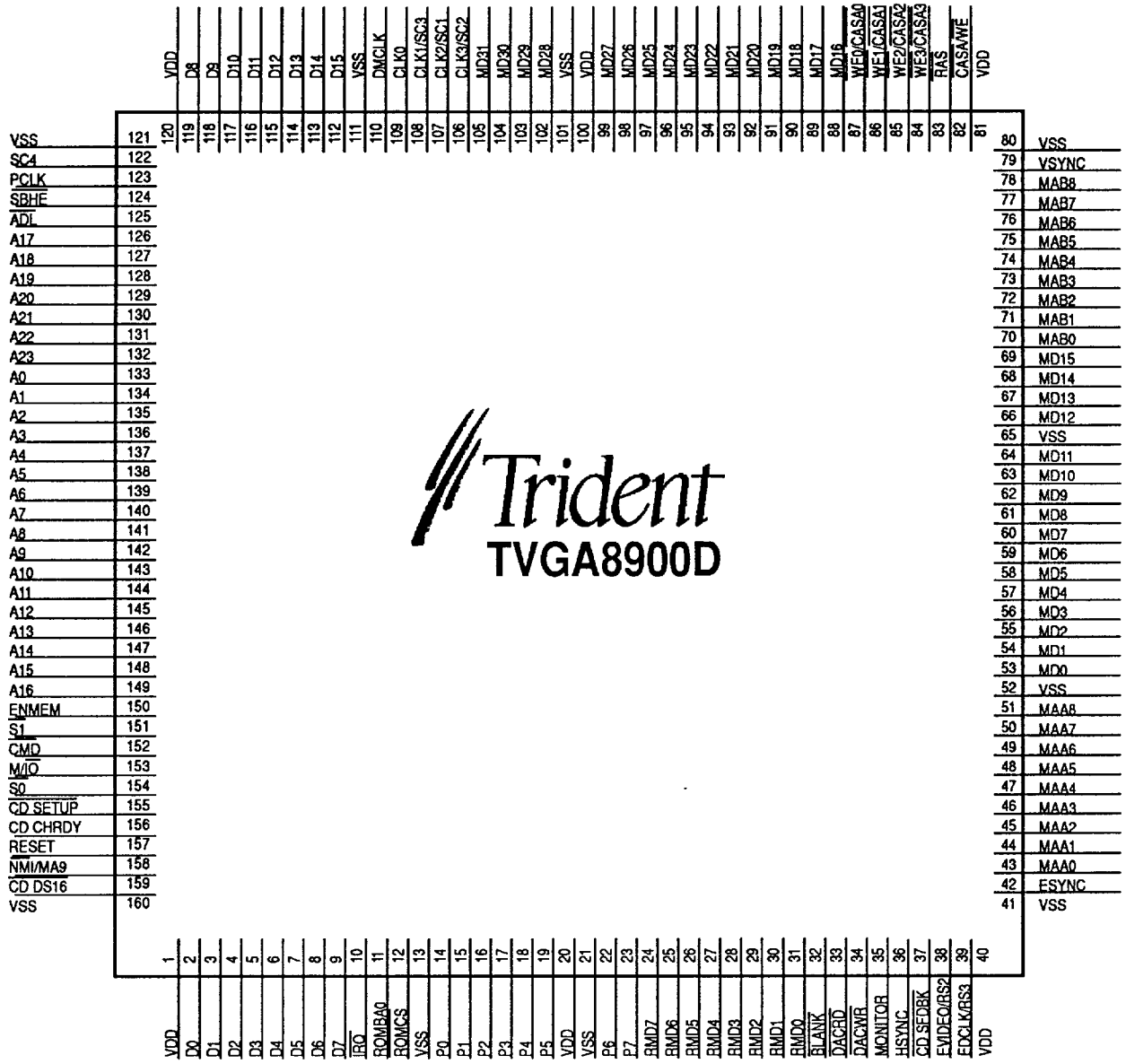

Figure 8-B. TVGA8900D Pin-Out (MCA Bus)

Table 12. TVGA8900D Pin Description

Pin	Pin Type	Pin Number	Description
Host Interface			
a. AT Bus Signals			
$\overline{IOR}$	I	151	I/O read strobe
$\overline{IOW}$	I	152	I/O write strobe
$\overline{MEMR}$	I	153	Memory read strobe
$\overline{MEMW}$	I	154	Memory write strobe
IOCHRDY	O	156	I/O channel ready
ALE	I	125	System address latch enable
AEN	I	155	Enable on-board I/O
LA19-LA17	I	128-126	Unlatched address bus, bit 19 to bit 17
SA19-SA17[1]	I	131-129	Address bus, bit 19 to bit 17
(LA22-LA20)			(Unlatched address bus, bit 22 to bit 20)
$\overline{HAD}$(LA23)	I	132	High address (Unlatched address bus bit 23)
SA16-SA0	I	149-133	Address Bus
$\overline{MCS16}$	O	159	Enable 16-bit transfer, open drain output
SD15-SD0	I/O	112-119,9-2	Data bus, bit 15 to bit 0
$\overline{ZWS}$	O	37	Zero wait state
IRQ	O	10	Interrupt request
$\overline{SBHE}$	I	124	Bus high-byte enable
ENMEM	I	150	Enable display memory
b. MCA Bus Signals			
$\overline{S1}$-$\overline{S0}$	I	151,154	Status bit 1-0
$\overline{CMD}$	I	152	Command
M/$\overline{IO}$	I	153	Bus memory or I/O cycle
CD CHRDY	O	156	Channel ready
$\overline{CD\ SETUP}$	I	155	Card setup
A23-A0	I	132-126,149-133	System address bus, bit 23 to bit 0
$\overline{CD\ DS16}$	O	159	Card data size 16-bit
D15-D0	I/O	112-119,9-2	System data bus, bit 15 to bit 0
$\overline{CD\ SFDBK}$	O	37	Card select feedback
$\overline{IRQ}$	O	10	Interrupt request
$\overline{SBHE}$	I	124	Bus high-byte enable
ENMEM	I	150	Enable display memory
$\overline{ADL}$	I	125	Address decode latch
Common Bus Signals			
RESET	I	157	System reset (active high); the falling edge latches configuration information into internal registers from memory data lines and AD7-AD0

Table 12. TVGA8900D Pin Description - Continued

Pin	Pin Type	Pin Number	Description
NMI/MA9	O	158	Non-maskable interrupt/additional address bus for 1MB of 512Kx8 or 256Kx16 DRAM chips
Display Memory Interface			
$\overline{\text{CASA}}/\overline{\text{WE}}$	O	82	Column address strobe for Bank A/memory write enable for DRAM requires multiple CAS and one memory write
$\overline{\text{WE3}}$-$\overline{\text{WE0}}$/ $\overline{\text{CASA3}}$-$\overline{\text{CASA0}}$	O	84-87	Write enable/column address strobe for Bank A when DRAM requires multiple CAS and one memory write
$\overline{\text{RAS}}$	O	83	Row address strobe
MAA8-MAA0	O	51-43	Multiplexing address bus of display memory Bank A
MAB8-MAB0	O	78-70	Multiplexed address bus of display memory Bank B
MD31-MD0	I/O	105-102,99-88 69-66,64-53	Memory data bus (bit 31 to bit 0)
DMCLK	I	110	DRAM clock
Video Interface			
VSYNC	O	79	Vertical synchronization pulse, polarity programmable
HSYNC	O	36	Horizontal synchronization pulse, polarity programmable
RMD7-RMD0	I/O	24-31	ROM/DAC data bus bit 7 to bit 0
P7-P0	O	23-22,19-14	Video DAC address, bit 7 to bit 0
PCLK	O	123	Pixel clock output
$\overline{\text{BLANK}}$	O	32	Blank output
$\overline{\text{DACRD}}$	O	33	DAC read strobe
$\overline{\text{DACWR}}$	O	34	DAC write strobe
MONITOR	I	35	Monitor type detect (analog monitor)
EVIDEO/RS2	I/O	38	External pixel data enable (feature connector)/extra DAC address (for true color mode)
EDCLK/RS3	I/O	39	External clock enable (feature connector)/extra DAC address (for true color mode
ESYNC	I/O	42	External sync enable (feature connector)
Clock Synthesizer Interface			
CLK1/SC3	I/O	108	Video clock input/Clock select output 3
CLK2/SC1	I/O	107	Video clock input/Clock select output 1
CLK3/SC2	I/O	106	Video clock input/Clock select output 2
CLK0	I	109	Video clock input
SC4	O	122	Clock select, output connect to pin 1 of TCK9004
BIOS Interface			
$\overline{\text{ROMCS}}$	O	12	BIOS EPROM chip select

Table 12. TVGA8900D Pin Description - Continued

Pin	Pin Type	Pin Number	Description
ROMBA0	O	11	BIOS EPROM address bit 0
Other External Interfaces			
MONITOR	I	35	Monitor type detect (analog monitors)
Power Pins			
VSS	GND	13,21,41,52,65,80 101,111,121,160	Ground
VDD	PWR	1,20,40,81,100,120	+5VDC

[1]Pins definition in parentheses are for linear addressing

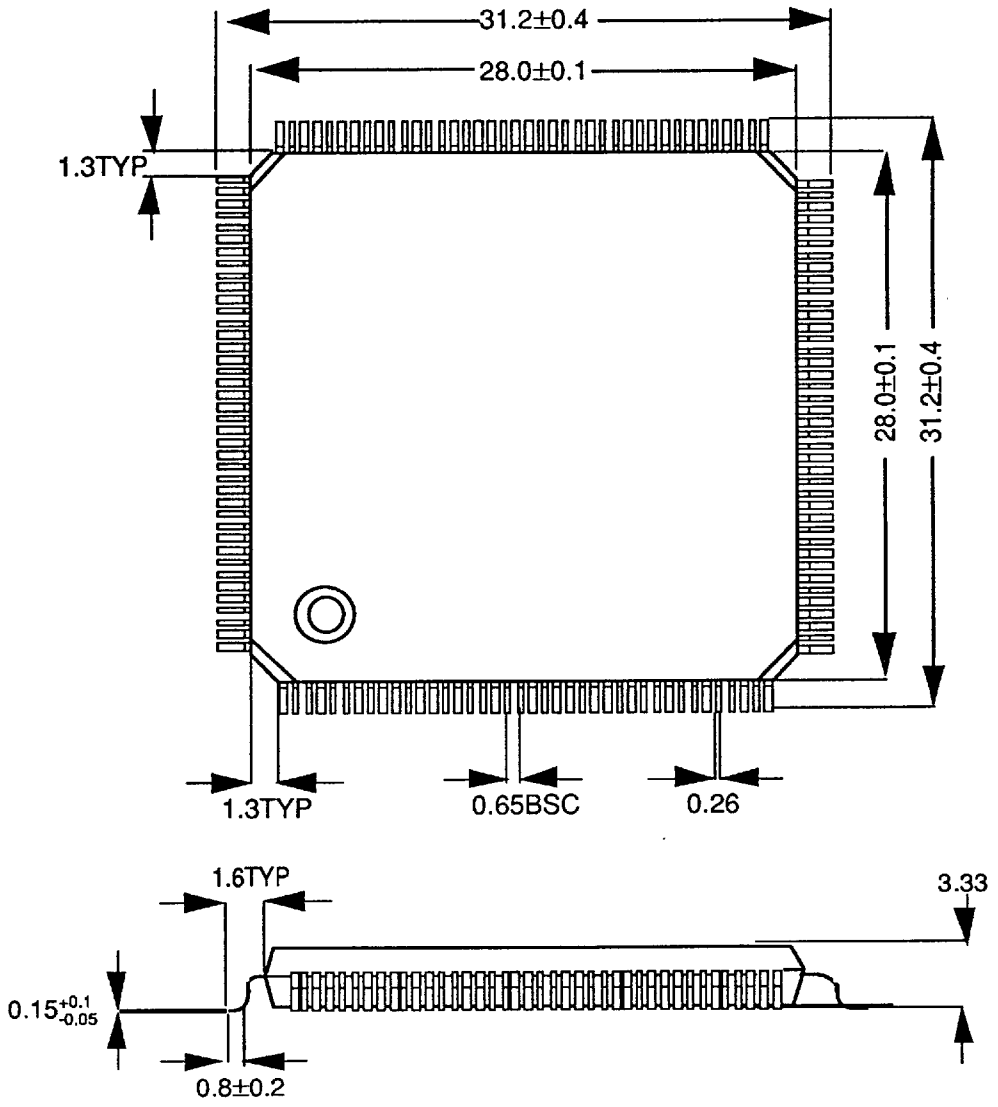

Figure 9. TVGA8900D Packaging PFP 160 Pins (dimensions in mm)