SGS-THOMSON MICROELECTRONICS

TS75C96

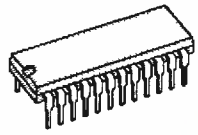
V.32, V.29, V.27ter, V.22bis, V.22, V.23, BELL 212A, BELL 103 MODEM CHIP SET

ADVANCE DATA

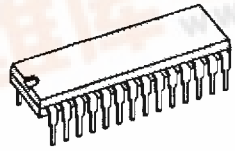
- CCITT V.32, V.22bis, V.22, V.21, V.23, Bell 212A, Bell 103 COMPATIBLE MODEM CHIP SET
- CCITT V.29, V.27ter FOR FAX APPLICATIONS
- INTEGRATED IMPLEMENTATION ON THREE DSP AND THREE MAFE CHIPS
- FULL DUPLEX OPERATION FROM 9600 TO 300bps
- FULL IMPLEMENTATION OF THE V.32 AND V.22bis HANDSHAKE
- V.29/4800bps AND V.27ter SHORT TRAIN SEQUENCES
- DYNAMIC RANGE : 43dB
- TWO SATELLITE HOPS AND FREQUENCY OFFSET CAPABILITIES (10Hz) FOR THE FAR END ECHO CANCELLER IN V.32 MODE
- TRELLIS ENCODING AND VITERBI DECODING
- 12.5% ROLL-OFF RAISED COSINE TRANSMITTER PULSE SHAPING
- HIGH PERFORMANCE PASSBAND FRACTIONALLY SPACED ADAPTIVE EQUALIZER
- SIGNAL QUALITY MONITORING
- PARALLEL INTERFACE TO STANDARD MICROPROCESSORS
- SERIAL DATA TRANSMIT CAPABILITY
- V.14 AND V.54 IMPLEMENTATION
- LOW POWER MODE AVAILABLE (PLCC)
- BIT RATE DATA CLOCKS PROVIDED FOR SYNCHRONOUS DATA TRANSFER
- FULL DIAGNOSTIC CAPABILITY
- DTMF GENERATION
- CALL PROGRESS TONE DETECTION
- PROGRAMMABLE FILTERS FOR "AUTOBAUD" IMPLEMENTATION
- SOFTWARE LICENSE AND DEVELOPMENT TOOLS AVAILABLE FOR EASY CUSTOMIZATION
- TOTAL POWER CONSUMPTION BELOW 1.5W

DESCRIPTION

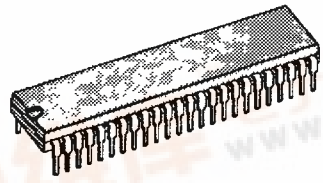
The SGS-THOMSON Microelectronics TS75C96 chip set is a highly integrated modem engine, which can operate in full duplex from 9600 to 300bps. The modem hardware consists of three analog front end (MAFE) chips, three DSP processor chips and additional memory chips plus the V.14 serial output converter. The three SGS-THOMSON analog front end chips (TS68950/1/2) are the transmit interface, the receive interface and the clock generator respectively. The modem signal processing functions are implemented on three ST18930 programmable digital signal processors.



DIP24
(Plastic Package)



DIP28
(Plastic Package)



DIP48
(Plastic Package)

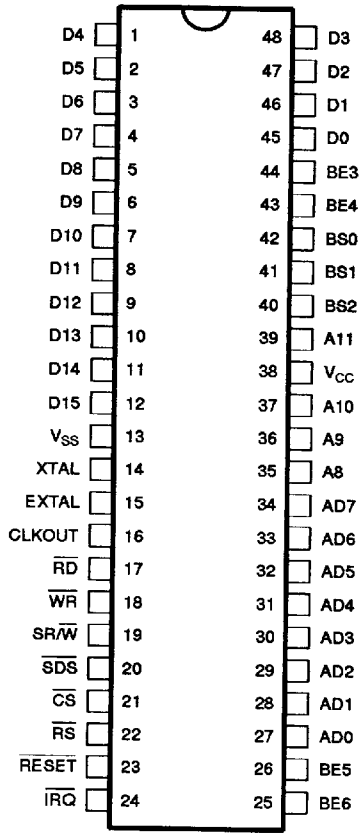
PLCC28
(Plastic Chip Carrier)

PLCC52
(Plastic Chip Carrier)

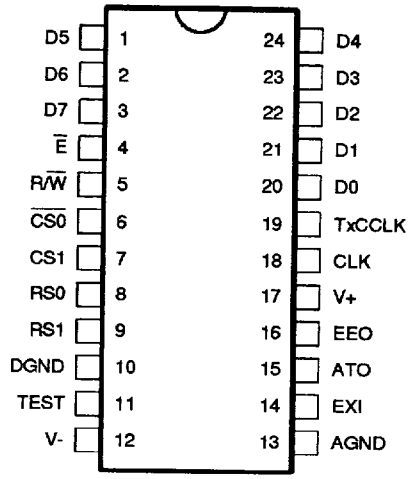
See Order Codes on Page 4

PIN CONNECTIONS

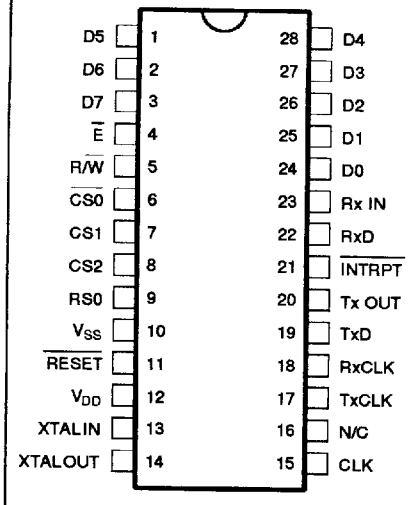
DIP48 : TS75C960 - TS75C961 - TS75C962



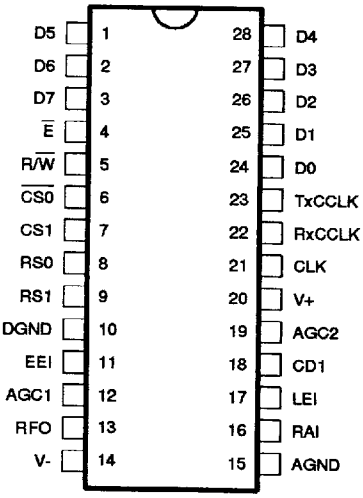
DIP24 :TS68950



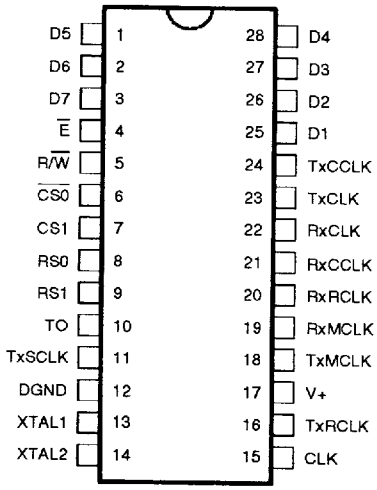
DIP28 : TS7538



DIP28 : TS68951



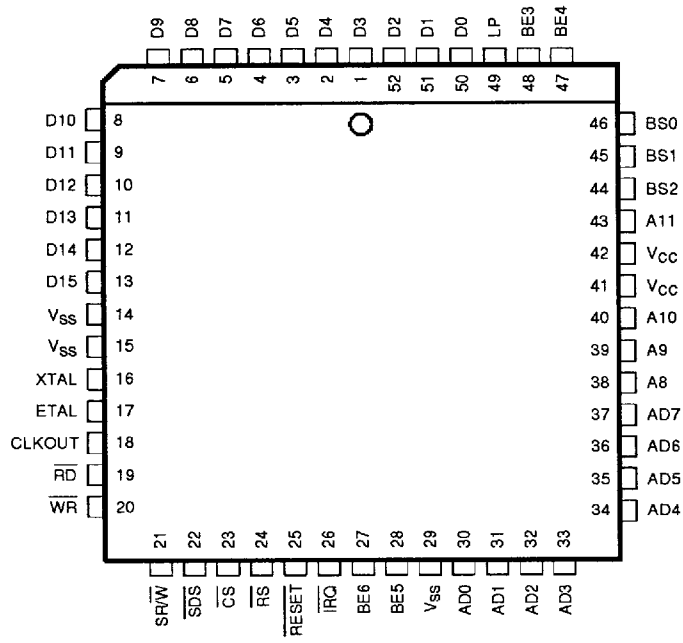
DIP28 : TS68952



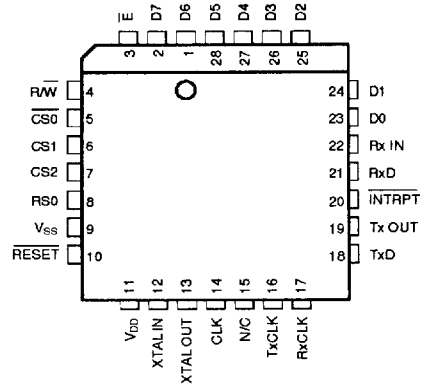
75C96-01 EPS/ 75C96-02 EPS/ 75C96-03 EPS/ 75C96-04 EPS/ 75C96-05 EPS

PIN CONNECTIONS

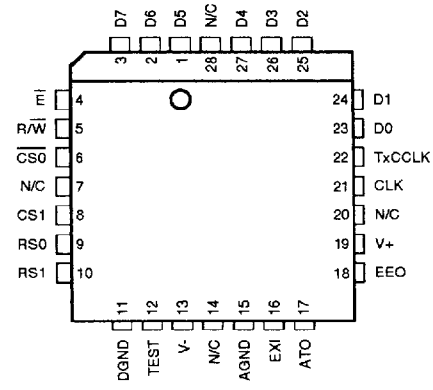
PLCC52 : TS75C960 - TS75C961 - TS75C962



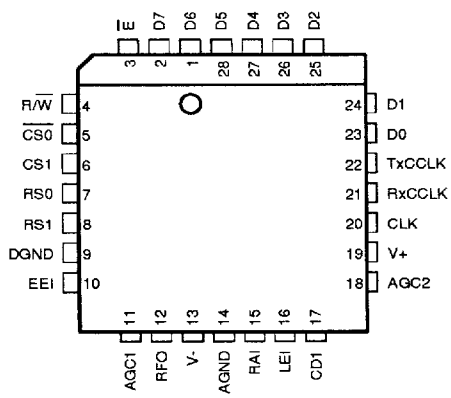
PLCC28 : TS7538



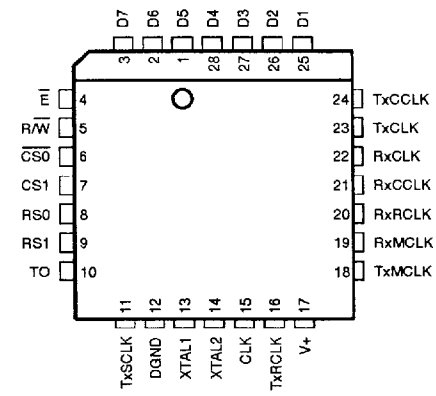
PLCC28 : TS68950



PLCC28 : TS68951



PLCC28 : TS68952



75C96-06 EPS / 75C96-07 EPS / 75C96-08 EPS / 75C96-09 EPS / 75C96-10 EPS

ORDER CODES

Part Number	Temperature Range	Package
TS75C960CP-S	0°C to + 70°C	DIP48
TS75C961CP-S	0°C to + 70°C	DIP48
TS75C962CP-S	0°C to + 70°C	DIP48
TS68950CP	0°C to + 70°C	DIP24
TS68951CP	0°C to + 70°C	DIP28
TS68952CP	0°C to + 70°C	DIP28

Part Number	Temperature Range	Package
TS7538CP	0°C to + 70°C	DIP28
TS75C960CFN-S	0°C to + 70°C	PLCC52
TS75C961CFN-S	0°C to + 70°C	PLCC52
TS75C962FN-S	0°C to + 70°C	PLCC52
TS68950CFN	0°C to + 70°C	PLCC28
TS68951CFN	0°C to + 70°C	PLCC28

75C96-01 TBL

PIN DESCRIPTION

SYSTEM INTERFACE

Pin Name	Type	Signal Name	Description
TS75C961 (DSP # 1 Transmitter and Handshake)			
AD0..AD7	I/O	D0H..D7H	System Data Bus : these lines are used for data transfer between the TS75C96 mailbox and the host processor
$\overline{CS}$	I	CSL	Chip Select : this input is asserted when the TSC75C96 is to be accessed by the host processor
$\overline{RS}$	I	RSL	Register Select : this signal is used to control the data transfers between the host processor and the TS75C96 mailbox
$\overline{SDS}$	I	DSL	System Data Strobe : synchronizes the transfer between the TS75C96 mailbox and the host processor
SR/$\overline{W}$	I	RWL	System Read/Write : control signal for the TSC75C96 mailbox operation
$\overline{IRQ}$	O	INTL	Interrupt Request : signal sent to the host processor to access the TS75C96 mailbox
$\overline{RESET}$	I	RSTL1	Master Reset (All DSP's RESET connected to this pin)

DATA INTERFACE

Pin Name	Type	Signal Name	Description
TS7538			
TxD	I	TxD	Serial Transmit Data
RxD	O	RxD	Serial Receive Data

ANALOG INTERFACE

Pin Name	Type	Signal Name	Description
TS68950 (Analog Front-end Transmitter)			
ATO	O	ATO	Analog Transmit Output
TS68951 (Analog Front-end Receiver)			
RAI	I	RAI	Receive Analog Input
LEI	I	LEI	Local Echo Input. Must be grounded.

CLOCK INTERFACE

Pin Name	Type	Signal Name	Description
TS68952 (Analog Front-end Clock Generator)			
TxCLK	O	TxCLK	Transmit Bit Clock
TxRCLK	O	TxRLCK	Transmit Baud Clock
TxCCLK	O	TxCCLK	Transmit Conversion Clock
TxMCLK	O	TxMCLK	Transmit Multiplex Clock
RxCLK	O	RxCLK	Receive Bit Clock
RxRCLK	O	RxRCLK	Receive Baud Clock
RxCCLK	O	RxCCLK	Receive Conversion Clock
RxMCLK	O	RxMCLK	Receive Multiplex Clock
TxSCLK	I	TxSCLK	Transmit Synchro Clock : can be used to synchronize the transmitter on an external bit clock provided by the RS232C (or V.24) junction

75C96-02 TBL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
TS75C960/1/2			
V_{CC} (1)	Supply Voltage	-3.0, 7.0	V
V_{IN} (1)	Input Voltage	-3.0, 7.0	V
T_{amb}	Operating Temperature	0, + 70	°C
T_{stg}	Storage Temperature	-55, + 150	°C
TS68950/1/2			
	Supply Voltage between V + and AGND or DGND	-0.3, +7	V
	Supply Voltage between V - and AGND or DGND	-7, +0.3	V
	Voltage between AGND and DGND	-0.3, +0.3	V
	Digital Input Voltage	DGND -0.3, V_{CC}^+ + 0.3	V
	Digital Output Voltage	DGND -0.3, V_{CC}^+ + 0.3	V
	Digital Output Current	-20, + 20	mA
	Analog Input Voltage	V_{CC} -0.3, V_{CC}^+ + 0.3	V
	Analog Output Voltage	V_{CC} -0.3, V_{CC}^+ + 0.3	V
	Analog Output Current	-10, + 10	mA
T_{oper}	Operating Temperture	0, + 70	°C
T_{stg}	Storage Temperture	-65, + 150	°C

75C96-03 TBL

Note : 1. With respect to V_{SS}.
Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

DC ELECTRICAL CHARACTERISTICS (DGND = AGND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DIGITAL SUPPLY (V_{CC} = 5.0V ±10%, V_{SS} = 0V, T_{amb} = 0 to +70°C, unless otherwise specified)					
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IL}	Input Low Voltage	-0.3		0.8	v
V_{IH}	Input High Voltage	2.4		V_{CC}	V
I_i	Input Extal Current	-50		+50	µA
V_{OH}	Output High Voltage (I_{load} =-300 µA)	2.7			V
V_{OL}	Output Low Voltage (I_{load} =3.2 mA)			0.5	V
P_D	Total Power Dissipation		1.0		W
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (Off State) Input Current	-20		-20	mA
ANALOG SUPPLY					
V^+	Positive Power Supply	4.75		5.25	V
V^-	Negative Power Supply	-5.25		4.75	V
I^+	Positive Supply Current			35	mA
I^-	Negative Supply Current	-35			mA

75C96-04 TBL

Note : Case Temperature T mustbe mantained below 100°C.

AC ELECTRICAL SPECIFICATIONS

CLOCK AND CONTROL PINS TIMINGS

(V_{CC} = 5.0V ±10%, T_{amb} = 0 to + 70°C, see Figure 1 - Output Load = 50pF + DC characteristics I load
Reference Levels : V_{IL} = 0.8V, V_{IH} = 2.4V, V_{OL} = 1.4V, V_{OH} = 2.4V - t_r, $t_f \leq$ 5ns for input signal)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{cex}	External Clock Cycle Time T_C=2 x t_{cex}		40		43.4	ns
t_{fex}	External Clock Fall Time				5	ns
t_{rex}	External Clock Rise Time				5	ns
t_{coh}	EXTAL to CLKOUT High Delay			25		ns
t_{col}	EXTAL to CLKOUT Low Delay			25		ns
t_{cor}	CLKOUT Rise Time				10	ns
t_{cof}	CLKOUT Fall Time				10	ns
t_{dlc}	CLKOUT to Control Output Low (INTL)				30	ns
t_{dhc}	CLKOUT to Control High (INTL)				30	ns

TS7538 CLOCK GENERATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CRYSTAL OSCILLATOR INTERFACE (V_{CC} = 5V ±10%, V_{SS} = 0V, T_{amb} = 0 to 70°C, unless otherwise specified)						
V_{IL}	Low Level Input Voltage		-0.3		0.8	V
V_{IH}	High Level Input Voltage	(all inputs except XTALIN)	2.4			V
V_{IHX}	Input High Voltage XTALIN			3.5	V_{DD}	V
I_{inX}	Input Laekage Curent on XTALIN	V_{IN} = 0V, V_{IN} = V_{DD}	-10		+10	µA
CLOCK TIMINGS (V_{CC} = 5V ±10%, T_{amb} = 0 to 70°C - Output Load = 50pF, DC characteristics load Reference Levels : V_{IL} = 0.8V, V_{IH} = 3.5V, V_{OL} = 0.8V, V_{OH} = 2.4V - t_r, $t_f \leq$ 5ns for input signals)						
t_{CX}	XTAL Cycle Time		40			ns
t_{CXW}	XTAL High or LOW		15			ns
t_{CXT}	XTALIN Fall and Rise Time				5	ns
t_{COD}	XTAL to CLK and XTALOUT Low and High Delay	XTAL to XTALOUT XTAL to CLK			30 40	ns ns
t_r, t_f	CLK and XTALOUT Fall and Rise Time			5		ns

LOCAL BUS TIMING

(V_{CC} = 5.0V ±10%, T_{amb} = 0 to + 70°C, see Figure 3)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{SDS}$ Pulse Widht (1)	32		tc/2	ns
t_{AH}	Address Hold Time	5			ns
t_{DDW}	Data Delay Time, Write Cycle			40	ns
t_{DHW}	Data Hold Time, Write Cycle	10			ns
t_{DDZ}	Data Valid to Z State			40	ns
t_{DSR}	Data Set-up Time, Read Cycle	20			ns
t_{DHR}	Data Hold Time, Read Cycle	5			ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{SDS}$, $\overline{RD}$ Low	20			ns

75C96-05.TBL

Note : 1. In multicycle exchanges, t_{pw} duration is extended by 1, 2, 3 machine cycle lenghts.

Figure 1 : Clock and Control Pins Timing

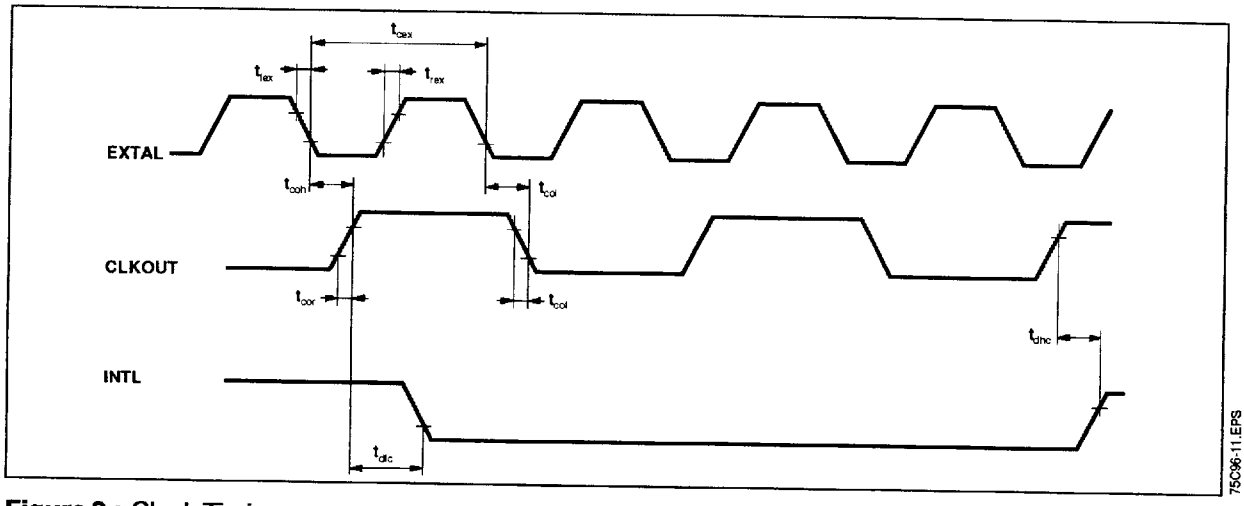


Figure 2 : Clock Timing

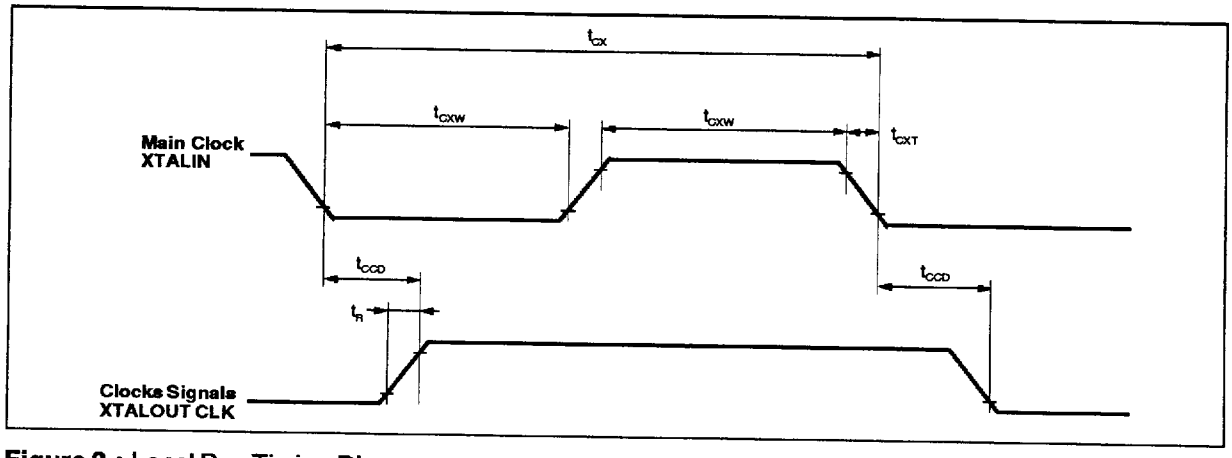
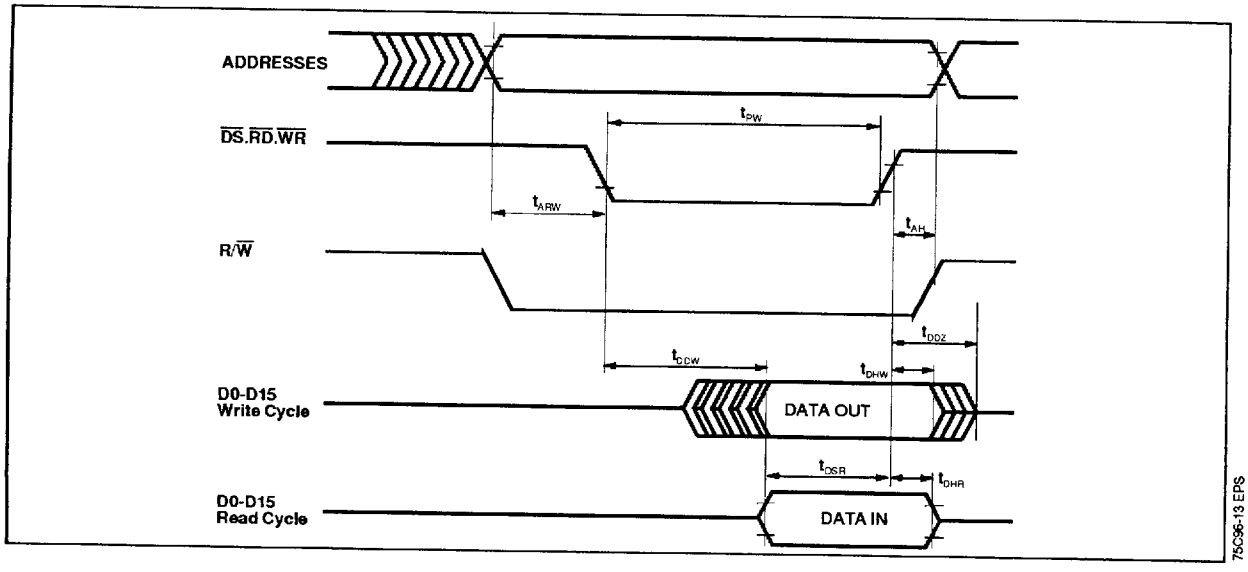


Figure 3 : Local Bus Timing Diagram



AC ELECTRICAL SPECIFICATIONS (continued)

SYSTEM BUS TIMING

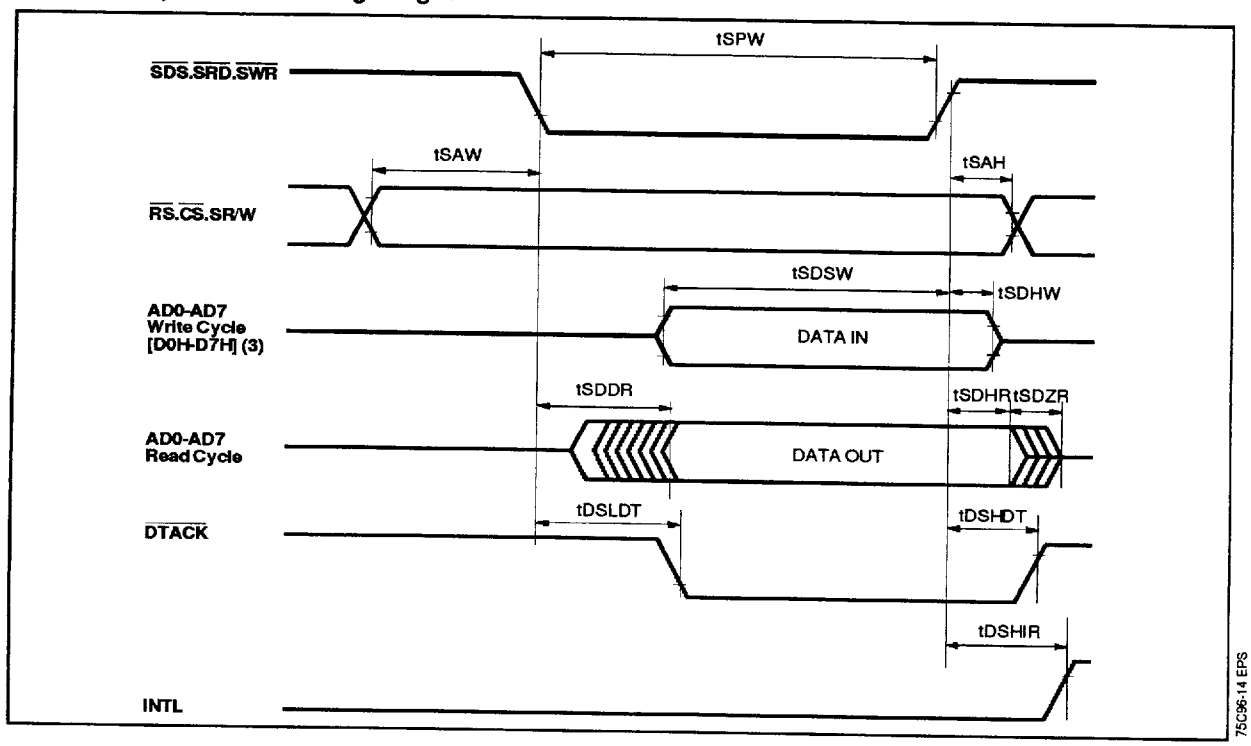
(V_{CC} = 5.0V ±10%, T_{amb} = 0 to + 70°C, see Figure 4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SPW}	$\overline{SDS}$, $\overline{SRD}$, $\overline{SWR}$ Pulse Widht	30			ns
t_{SAW}	SR/W, $\overline{CS}$, $\overline{RS}$ Sep-up Time15	15			ns
t_{SAH}	SR/W, $\overline{CS}$, $\overline{RS}$ Hold After SDS High	5			ns
t_{SDSW}	Data Set-up Time, Write Cycle	15			ns
t_{SDHW}	Data Hold Time, Write Cycle	5			ns
t_{SDDR}	Data Delay Time, Read Cycle			25	ns
t_{SDHR}	Data Hold Time, Read Cycle	5			ns
t_{SDZR}	$\overline{DSD}$, $\overline{SRD}$ High to Z State			25	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low			20	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ Desactivated (1)			20	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High			800	ns

75C96-06 TBL

Notes : 1. DTACK is an open drain output. Test load includes R_L = 820Ω V_{DD}.
2. This delay depends on programming mode. Its maximum value is $2T_c$ + 2 instruction cycles (see User's Manual).
3. Signal names on Host Processor Interface.

Figure 4 : System Bus Timing Diagram



75C96-14 EPS

FUNCTIONAL DESCRIPTION

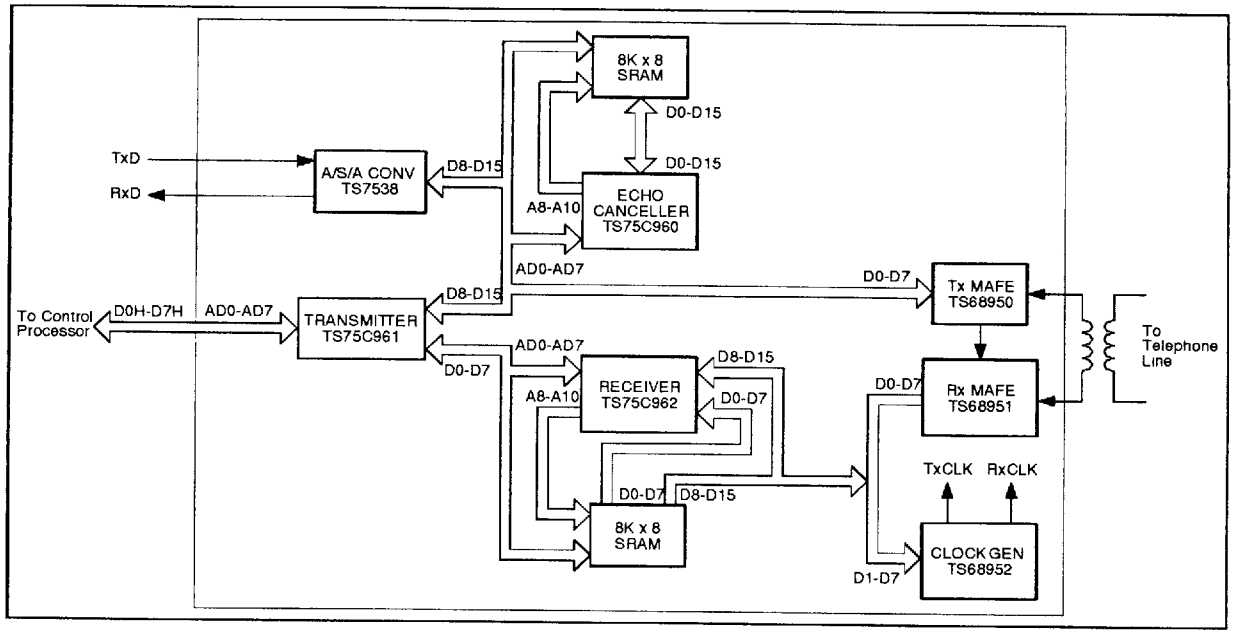
1 - SYSTEM ARCHITECTURE

The SGS-THOMSON TS75C96 chip set is a highly integrated modem engine which provides the functionality and performance requirements for full-duplex 9600bps modem solutions at a low cost and with a small circuit area. At the heart of the modem engine are three SGS-THOMSON DSP's which implement the complete signal processing and control functions. The analog front end of the modem engine consists of the SGS-THOMSON MAFE three-chip set which is designed to meet the requirements of high-speed modem applications and particularly V.32 modems. An asynchronous to synchronous and synchronous to asynchronous converter provides serial data inputs and outputs. The only other components in the modem engine are the external RAM chips used for the far-end echo canceller delay line and the Viterbi decoder.

2 - PROCESSOR AND MAFE CHIPS ARRANGEMENT

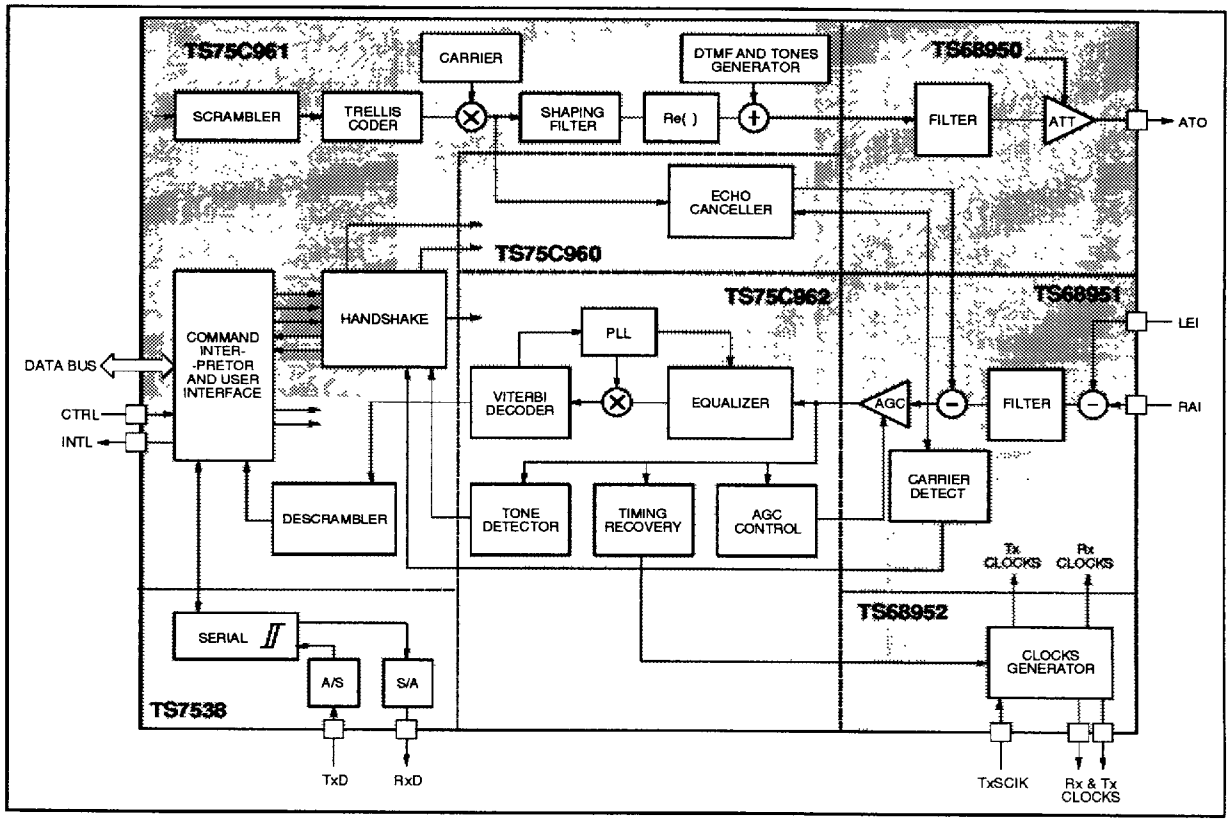
Figure 1 shows the interconnections between the MAFE signal processors and A/S - S/A converter. DSP# 1 (TS75C961) communicates with the control processor through its system bus, AD0-AD7. It is also connected to the two other DSP's and the TS7538 through its D0-D7 and D8-D15 data buses to transfer data, to pass a control command to the DSPs and to get the modem operation status and then pass it to the control processor. The transmitter, V.32 handshake and part of the receiver algorithms are implemented in this processor. DSP 0 implements the echo cancellation function. 4Kx16 of RAM are connected to this processor to implement the data delay line for the far end echo cancellation. DSP 2 implements most of the receiver functions. 2Kx16 of RAM are attached to it due to the requirements of the Viterbi decoder.
The transmitter interface chip, TS68950 (see ref 5 of Appendix D), is connected to the 8 MSB's of the DSP 1 data bus. The echo replica is sent from DSP 1 to TS68950 then to the receiver interface chip, TS68951 (see ref 6 of Appendix D), after conversion to analog format. This chip and the clock generator chip, TS68952 (see ref 7 of Appendix D), are connected to the 8 MSB's of the DSP 2 data bus. The clock generator chip generates the A/D and D/A sampling clocks and the data bit and baud rate clocks.

Figure 5 : Hardware Architecture



FUNCTIONAL DESCRIPTION (continued)

Figure 6 : Functional Block Diagram (V.32 Operation)



3 - OPERATION

3.1 - Modes

The modem implementation is fully compatible with many CCITT and Bell recommendations. It operates at different bit rates from 9600 to 300bps. In the 9600bps mode, the trellis encoder and the Viterbi decoder can be switched in or out. Both the bit rate and trellis options are determined during the initial modem handshake sequence.

3.2 - Signal Spectrum Shaping

A square root of 12.5 percent roll-off raised cosine filter is implemented in the transmitter to properly shape the transmit signal pulse. This filter is chosen based on a compromise of two considerations.

First, the signal should have a narrow spectrum to avoid severe distortion on the telephone line.

Second, the signal spectrum should be made as wide as possible to facilitate timing recovery in receiver.

3.3 - Echo Cancellation

The echo canceller is implemented on a single DSP with its associated external RAM. It cancels both near-end and far-end echoes even in the presence of frequency offset in the far-end echo path. The near-end echo cancellation is better than 55dB and the residual near-end echo is smaller than - 65dBm with a near-end echo level of -10dBm at the receiver input and a far-end signal level of - 43dBm.

The combined near-end and far-end echo cancellers maintain the residual echo level 24dB below the received signal even if the far-end echo signal path introduces up to 10Hz of frequency offset. This level of cancellation is achieved when the far-end echo is 8dB below the received far-end signal.

FUNCTIONAL DESCRIPTION (continued)

3.4 - Receiver Description

The incoming signal is sent to the receiver interface chip to have the echo removed before being sent to DSP 2. The timing recovery algorithm takes the signal after the echo cancellation to derive the timing error to control the sampling phase of the A/D. It is able to cope with distant modem frequency drifts up to 1.10^{-4} as per CCITT rec. The A/D output samples are sent to the adaptive equalizer and the signal energy estimator for the gain control. The adaptive equalizer outputs a complex number every baud interval, which is then phase corrected by the carrier recovery loop. The Viterbi decoder makes hard decisions on the phase corrected samples for the adaptation of the equalizer and carrier recovery. It also makes soft decisions with an optimum decoding depth.

3.5 - Equalization

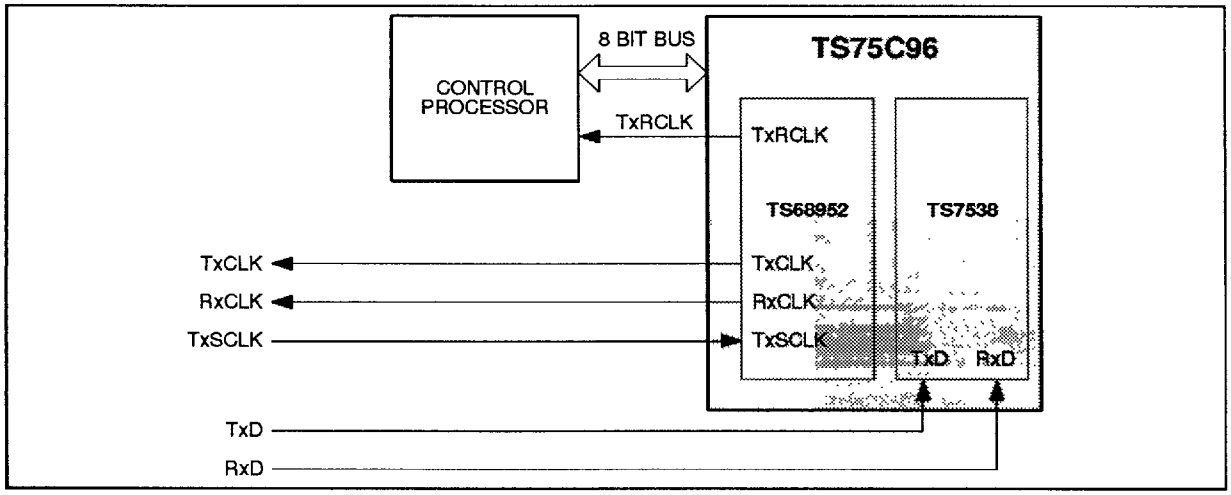
The modem receiver has a passband 26 bauds wide T/3 fractionally spaced automatic adaptive equalizer which can compensate for the signal degradation caused by low quality line conditions. The modem transmitter has a fixed compromise equalizer.

3.6 - Clock and Data Synchronization

Both transmit and receive clocks have the same nominal frequency value.
In fax modes, the transmit conversion clock signal (TxCCLK) is always set to 7200Hz, the transmit band clock signal (TxRCLK) is always set to 2400Hz.
Except in FSK modes, these clocks are plesiochronous. The nominal frequencies are :

Mode	TxCLK	TxRCLK	Byte/Irq	Rate
V.32TCM	9.6K	2.4K	1/2	9600bps Treillis
V.32QAM	9.6K	2.4K	1/2	9600bps QAM
V.32QAM	4.8K	2.4K	1/4	4800bps
V.29	9.6K	2.4K	1/2	9600bps
V.29	7.2K	2.4K	3/8	7200bps
V.29	4.8K	2.4k	1/4	4800bps
V.27ter	4.8K	2.4K	1/4	4800bps
V.27ter	2.4K	2.4K	1/8	2400bps
V.22bis	2.4K	0.6K	1/8	2400bps
V.22	1.2K	0.6K	1/16	1200bps
V.22	0.6K	0.6K	1/32	600bps
Bell 212A	1.2K	0.6K	1/16	1200bps
V.23	7.2K	1.2K	3/8	1200/75bps
Bell 103	7.2K	1.2K	3/8	300bps
V.21	7.2K	1.2K	3/8	300bps

Figure 7 : Clock Signals for Synchronous Transmission



FUNCTIONAL DESCRIPTION (continued)

The TxCCLK is always 7.2kHz. The TxRCLX is always 2.4kHz.
The TxMCLK is always set to 2.4kHz after a configuration command **CV32, CV22B**.
During the hansdshake (V.32 and V.22bis) the bit clock (TxCLK and RxCLK) is set to the maximum value (respectively 9600Hz and 240Hz). At the end of the handshake, depending of the negociation, this frequency is automatically set to the proper value.

3.7 - Tone Generator

The TS75C96 has thirteen tone commands to quickly program the tone generators to generate the 2100Hz Answer Tone (ANSWR) and the tone pairs for DTMF digits (DTMF0, ..., DTMF9, DTMF*, DTMF#). These commands provide the tones and control required for normal operation of the modem, but do not enable tone generation.
Some circumstances might arise where additional tones are desired. For such cases, the TS75C96 provides the user with the ability to generate such additional tones. This special feature is achieved through use of the tone control commands.
The TS75C96 maintains a pair of locations which are reserved for tone generation parameters. These locations are denoted as TONE1 and TONE2. These locations may be programmed by the use of the define tone commands, DEFT1 and DEFT2. These commands provide the two tone generators with the phase increment of the tone to be generated with respect to the 7200Hz sample rate. ($7FFF = +180°).
The normal tone commands automatically program the tone generators. The DEFT1 and DEFT2 commands do not change the enabled or disabled state of the tone generators. If a tone is being generated when the DEFT command is received, the new tone will be generated without further action. If tone generation was not in progress it is not started.
Enabling the tone generators is accomplished by the tone control commands TGEN0, TGEN1, TGEN2, and TGEN12. Each of these commands affects both tone generators. TGEN0 disables both tone generators and TGEN12 enables both tone generators. To enable tone generator 1 and disable tone generator2 the TGEN1 command is used. For the reverse condition, with generator 1 disabled and generator 2 enabled, the TGEN2 command is employed.
Refer to the command in appendix A for more detailed information.
Generation of special user tones is not part of the normal data communications operations of the modem. Use of this feature may interfere with data transfer operations. It is the responsability of the user to insure that the tone generators are used at a time when such interference will not occur and to disable both tone generators when the tone generation operations have been completed.

3.8 - Test Modes

The modem can be configured in two test modes, namely analog loop back and digital loop back modes. These loop back modes conform to the test loops 3 and 2 respectively defined in CCITT recommendation V.54.
In the local analog loop back mode, the transmitter signal is directly fed back into the local receiver input with the echo canceller enabled. The user is responsible for supplying a switch, which is controllable by the control processor, to enable or disable the analog loop back mode. The receiver descrambler is set as the inverse of the transmitter scrambler so that the receiver detects correct bits.

In all fax modes of operation, the TS75C96 supports the analog loop back capability. The command sequence is :
- CFAX to initialize FAX speed and parameter.
- SYNC to enable the receiver to demodulate FAX signal.
- HSHK to start FAX handshake (H status bit goes high).

When the H bit goes low, the TS75C96 can transmit and demodulate the incoming bit stream.
When using PLCC packages, a low power pin allows to drastically reduce the power consumption of the DSP's. The output clock frequency is divided by 16. The low power mode is disabled by a hardware reset on the 3 DSP's.

3.9 - Power-on Initialization

When the power is turned on, the transmitter interface sets the output signal attenuation to infinite. This avoids undesirable signal transmission on the telephone line (see ref 5 of Appendix D). The gain of the AGC in the receive interface is set at the lowest level to avoid signal clipping during the initial handshake. The clock generator is programmed to generate all the necessary clocks for the 9600bps mode. The clocks include the 7200Hz sampling clock, the 2400Hz baud rate clocks and the 9600bps bit rate clocks. The transmit clocks are free running when the TxSCLK pin is tied to a fixed logic level. Otherwise, the transmit bit clock is synchronized to the frequency present at the TxSCLK pin. DSP 1 is configured properly to receive commands from the control processor.

FUNCTIONAL DESCRIPTION (continued)

4 - MODEM INTERFACE (Figure 4)

4.1 - Analog Interface

The transmit signal at the tip and ring is programmable over a 22dB dynamic range by 2dB steps in TS68950. The signal level can be further scaled to any value by setting a scaling factor in the DSP. The nominal Transmit level, at the ATO pin is – 5.7dBm in V.32.

4.2 - Digital Interface

The DSP and control processor interface complies with the system bus interface of the ST18930. The interface to the control processor is managed by DSP 1 as shown in Figure 5. The DSP signals which are presented to the interface, and a brief definition of the signals are tabulated in Table 1.

All information exchanges across this interface conform to the three byte mailbox structure (see ref 4 of Appendix D) and protocol of the DSP. As may be seen in the table, the DSP generates a control signal, INTL, which defines the mailbox handshake operation.

Table 1 : Digital Interface Signals

Interface Signals	Signal Definition
D0H D1H D2H D3H D4H D5H D6H D7H	Data Bus (LSB) Data Bus Data Bus Data Bus Data Bus Data Bus Data Bus Data Bus (MSB)
RWL SDSL INTL CSL RSL	Write System Data Strobe Interrupt Request Mailbox Handshake DSP Select
TxD RxD	Transmit Data Receive Data
TxRCLK TxRCLK TxCLK RxCLK TxMCLK RxMCLK TxSCLK	Transmit Baud Rate Clock Receive Baude Rate Clock Transmit Bit Rate Clock Receive Bit Rate Clock Transmit Multiplex Clock Receive Multiplex Clock Transmit Terminal Clock

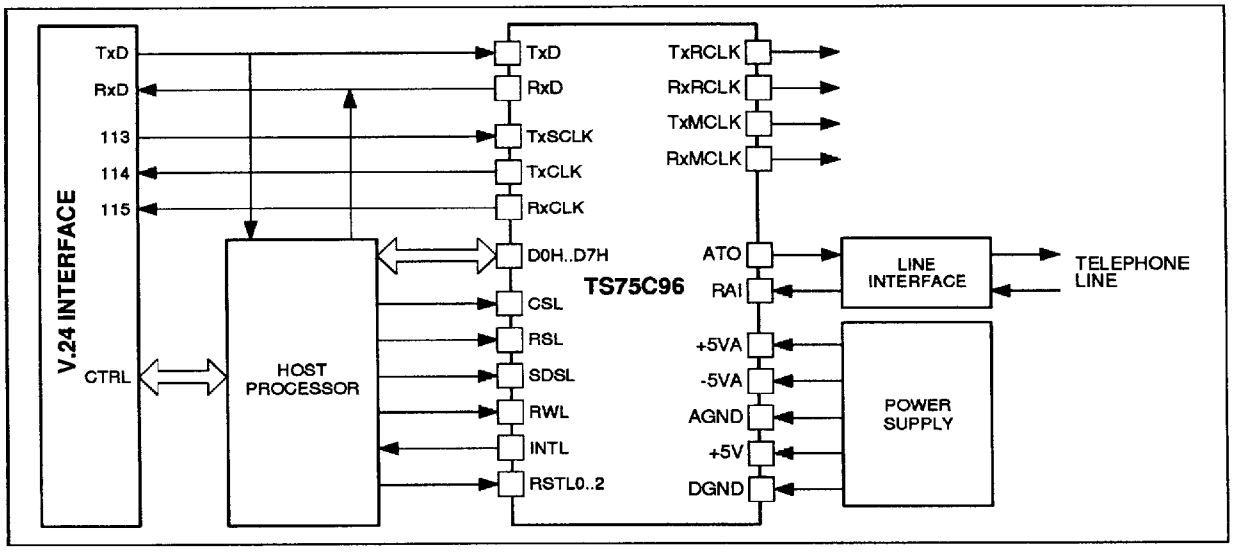
4.2 - V.24 Data Interface

The TS75C96 provides two different modes for data transfer :

- Serial V.14 interface synchronous or asynchronous.
- Parallel 8bit synchronous interface.

The mode of operation is selected using the SERIAL command of the CCI (Control Command Interpreter). The TS75C96 does also include dedicated hardware (scramblers and detectors) to detect all the V.54 specific signals.

Figure 8 : Functional Interconnect Diagram



FUNCTIONAL DESCRIPTION (continued)

4.3 - Memories Interface

DSP0 and DSP2 require external static RAM Memory. A minimum of 2Kx16 is required by DSP2 for Virterbi decoding and 4Kx16 by DSP0 for echo cancellation. The maximum access time to allow proper operation is 100ns for both memories. The use of 8Kx8 Static RAM from SGS-THOMSON is recommended. However DSP0 allows use of different type of memory. When using 8Kx8 memory pin BS0 of DSP0 must be tied to +5V otherwise tied to ground. (Intel or Motorola bus choice)

4.4 - Control Processor/DSP Interface

As seen by the software in the user provided control processor, DSP 1 is a synchronous machine. It requires the attention of the control processor at regular intervals in order to perform properly. Any failure of the control processor to interact with the modem engine in a timely manner will result in reduced performance or improper operation.

Each interaction begins when the control processor sends a three byte command to the mailbox. Once the command has been written to the mailbox, the ownership of the mailbox is relinquished by the control processor. Upon acquisition of the mailbox, DSP 1 reads the command bytes and then sends a three byte response to the mailbox. Then, DSP 1 relinquishes the ownership of the mailbox back to the control processor. The received command is then decoded and the embedded data and/or operational parameters are extracted and acted upon as appropriate. The modem status information will be collected for the next mailbox exchange. The control processor handles the returned information as soon as it regains the ownership of the mailbox.

Because the control processor owns the mailbox initially, it may store a command at any time before it is required by DSP 1. After this, the mailbox becomes available to DSP1 and can be read by it when required. The rate of exchange beetwen the TS75C96 mailbox and the control processor is nominally 2400 interrupts per second. However, this rate can be reduced down to 20 interrupts per second when using the SERIAL command. If the collected status information does not induce any specific command from the last, then a NOP command must be sent to ensure proper operation

4.5 - Mailbox Description

The mailbox located internally to the DSP contains 3-byte input (RIN) and 3-byte output (ROUT) shift registers.

The DSP has an internal flag RDYOIN which indicates whether the DSP (RDYOIN = 0) or control processor (RDYOIN = 1) has access to the mailbox.

The DSP can relinquish its accessability to the mailbox by setting RDYOIN but it can no longer regain access to the mailbox as RDYOIN is reset only after the control processor relinquishes its accessability to the mailbox.

The access protocol and system bus transfers are controlled by an internal I/O sequencer within the DSP described as follows :

1. The mailbox is made available to the control processor by the DSP program which sets RDYOIN flag to 1. This action will cause INTL mailbox handshake signal to switch to the active (low) state.
2. The control processor detects INTL active and dummy reads the mailbox by forcing DSP Select (CSL) and Register Select (RSL) low along with write signal (RWL) high. The activated Data Strobe signal (SDSL = 0) validates the above signals.
3. The DSP detects the dummy read of its mailbox via the control signals mentioned in 2 and negates INTL mailbox handshake signal within 800ns.
4. The control processor detects the negation of INTL indicating that the DSP mailbox is available for data transfers. The control processor writes three 8-bit bytes and reads three 8-bit bytes in the mailbox shift registers RIN, ROUT respectively.
5. The exchange protocol described above is terminated by the control processor performing a dummy read of the mailbox as in 2 but with RSL in the high state.
6. The RDYOIN flag within the DSP is cleared to 0 by the dummy read of the mailbox in step 5 and the DSP now has access to RIN and ROUT registers within the mailbox.

USER INTERFACE - COMMAND SET

The command set has the following attractive features :

- User friendly with easy to remember mnemonics.
- Allows straightforward expansion with new commands to suit specific customization requirements.
- Fully compatible with other SGS-THOMSON DSP-based modem products.

The command set has been designed to provide the necessary functional control of the TS75C96. Each command falls into one of several groups, based on function and the presence or absence of parameters. The length of the OP code varies with instruction type, but in all cases, a command consists of three bytes. If no specific command is necessary to drive the TS75C96, a NOP command must be sent to the mailbox. The commands which pass parameters or data to DSP 1 have a short OP code format. Byte 0 forms the OP code portion of the command. Bytes 1 and 2 are data and/or parameters associated with each OP code. The meaning of the last two bytes is dependent on the specific instruction.Other instructions command the TS75C96 to perform certain specific tasks. These do not pass parameters or data to the TS75C96. These commands have an OP code which is a full 24 bits in length. When a command requires an answer from DSP#1, the control processor has to wait until the answer has been received before issuing a new command requiring an answer. However, the control processor can still send commands which do not require an answer. The command set of the TS75C96 is summarized below. The descriptions are of the form :

MNEMONIC (OPCODE) : DESCRIPTION

For detailed information and data format specifics of each command, please refer to appendix A.

1 - COMMAND SUMMARY

1.1 - Operational Control Commands

FREZ (16,17,1B,1C) : Freezes adaptive processes.

HSHK (040000) : Handshake. Begins the handshake sequence. The TS75C96 carries out all the steps defined in the CCITT recommendation. The status reported to the control processor will indicate the success or failure of the process and its progress.

INIT (0600C0) : Initialize. Initialize the modem. Set all parameters to default values and wait for commands for the control processor.

NOP (000000) : No Operation. No new operation is commanded. The state of the TS75C96 remains unaltered and a previously invoked multi-baud command (such as HSHK) continues.

RTRA (050000) : Retrain. Start sending the retrain sequence as defined in the CCITT recommendation.

SCRM (18) : Enable /disable the V.22bis transmit scrambler. At the end of a handshake, both scramblers are enabled. The purpose of this command is for the use in loop 2 configurations (Digital loopback). During normal transmission mode this command must not be used.

SETGN (02) : Set Gain. This command sets a global gain factor, which will be multiplied by all transmit samples before being sent to the TS68950. Bytes 1 and 2 store the gain factor.

SYNC (1A) : Start fax receiver synchronization.

STOP (19) : Stop fax transmitter according with CCITT V.27ter.

1.2 - Data Communications Commands

XMIT(01) : Transmit data.

SERIAL(15) : Enables the use of the TS7538. Using it informs the TS75C96 that it must get/send Bytes of data from/to the TS7538. When this mode is enabled, one must not use the XMIT command. To return to parallel synchronous mode (For V.22bis digital loopback handshake, for example) one must first disable the SERIAL mode (SERIAL,0,0). When enabled, the serial mode allows the reduction of the frequency of the IRQ signal. This period can be reduced down to 100ms.

Warning: the status word of the modem, furnished by the TS75C96, is updated by the mailbox exchange. Even if the microcontroller does not want to send a specific command, it must not program the IRQ rate to a value which inhibits overall modem performance. The serial command allows the programming of the TS7538.

Changing the CR0 and CR1 register values of the TS7538, when in data mode, can cause a loss of data.

1.3 - Memory Manipulation Commands

SPAC (13) : Store Parameter And Count. Store parameter in addressed memory and increment the pointer. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable memory location currently specified by the Memory Address Register. The contents of the Memory Address Register are incremented by 1 at the completion of this command.

USER INTERFACE - COMMAND SET (continued)

SPAM (12) : Store Parameter in Addressed Memory. This command passes data in bytes 1 and 2, least significant byte in byte 1. It is used to write an arbitrary 16-bit value into the writable memory location currently specified by the Memory Address Register.

WARP (10) : Write Address and Return Parameter. This command allows the controller to read any of the XRAM, YRAM, ERAM or CROM (DSP internal or external memory areas) of any of the three modem DSPs without interrupting the processors. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP# 1 stores the address in the Memory Address Register and returns the contents of the addressed location.

WARPX (11) : Write Address and Return Parameter Complex. The address to the V.32 modem engine is provided in bytes 1 and 2 of the command (least significant byte first). DSP 1 stores the address in the Memory Address Register. The most significant bytes of the real and imaginary parts of a complex number are returned. The 8 most significant bits of the data addressed by the Memory Address Register are returned to the control processor through byte 1. Byte 2 stores the 8 most significant bits of the data at the location immediately higher. The Memory Address Register retains the address provided. (i.e. it is not incremented).

1.4 - Configuration Control Commands

CV32 (20) : Configure modem for V.32. Configure the modem as Originate / Answer, 9600/4800, Viterbi / No-Viterbi, Analog Loopback.

CFSK (1D) : Configure modem for FSK modes of operation (V.23/V.21/Bell103).

CFAX (1F) : Configure for Fax modes. (V.29/V.27ter)

CV22B (1E) : Configure modem for V.22bis/V.22/Bell212A modes.

1.5 - Mafe Manipulation Commands

CMAFE (07) : Configure MAFE. The following two bytes of this command are written directly to the MAFE chip set (TS68950/1/2).

RRR1 (080000) : Read Register 1. Causes the TS75C96 to read the 12 bit contents of the MAFE register RR1.

RRR2 (090000) : Read Register 2. Causes the TS75C96 to read the 12 bit contents of the MAFE register RR2.

WTR1 (0A) : Write Register 1. Causes the TS75C96 to write the supplied data to the MAFE register TR1.

WTR2 (0B) : Write Register 2. Causes the TS75C96 to write the supplied data to the MAFE register TR2.

1.6 - Tone Select Commands

TONE (0C) : Select Tone. Program the tone generator(s) for the desired tone(s). Examples include :

ANSWR (0C1000) : Program the tone generator for the 2100Hz answer tone.

DTMF (see appendix) : Program the tone gene-rators for the tone pair which forms the specified DTMF digit.
This command selects the tones to be transmitted, but does not enable the tone generators. To transmit the tones, the TONE control commands must be issued.

1.7 - Tone Control Commands

DEFT1 (0E) : Define Tone 1. Define tone 1 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 1. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment. (+ 180° = $7FFF)

DEFT2 (0F) : Define Tone 2. Define tone 2 as specified by the parameter provided. The two data bytes following the opcode are used to program, but not enable, tone generator 2. The data for the tone is represented as a phase offset per sample. Byte 1 stores the least significant byte of the phase increment.

TGEN (0D) : Tone Generator control. Enable or disable tone generator 1 and tone generator 2 according to parameter provided. If both tone generators are enabled, the level of tone 2 is 2dB higher than that of tone 1.

USER INTERFACE - COMMAND SET (continued)

2 - STATUS REPORTING

Whenever DSP 1 owns the mailbox, it transmits the modem status to the control processor. The status consists of three bytes of information which are stored by DSP 1 in its ROUT register for access by the control processor. At each mailbox exchange a set of 3 bytes is returned to the microcontroller. Three type of information can be given to the host processor. The order of priority is :

1. Bytes of received data.
2. Answer to a Command.
3. The status of TS75C96, including RS232 circuits, signal quality information, multiple tone detector flags. Bits D4, D3 of byte 0 of the status word select the type of data contained in the current status word. Data are available both in parallel and serial mode unless the user makes the choice of reducing the IRQ rate.Data bits have higher priority than the answer to the previous command. If both data byte and command answer are ready to be sent, the data will be sent. The TS75C96 supports 3 different phases to which correspond 3 different possibilities of status words.

1. At the beginning (master reset or INIT command) the TS75C96 is in a state called CALL ESTABLISHMENT mode. The user is establishing a call and is waiting for an answer from the far end modem.
2. After that state, the hanshake with the far end modem is started using the HSHK command (associated with one of the CV32, CV22B commands). The state of the TS75C96 becomes HANDSHAKE.
3. At the end of the handshake, the TS75C96 goes into the DATA TRANSFER mode. At that step, bytes of data can be exchanged with the far end modem. When the TS75C96 detects a far end retrain, or when the host processor sends a RTRA command, the TS75C96 goes back into the HANDSHAKE mode. The bit D1 of status Byte indicates that the TS75C96 is in HANDSHAKE mode.

Byte 0 contains status flags. Refer to appendix B for the detailed format of the status response. The four most significant bits, F00, F01, F10 and F11, indicate various conditions during the call establishment, handshaking and the data modes. They have different meanings in different modes. The flag DAV1 and DAV2 are used to indicate the type of information contained in bytes 1 and 2. Bit H is used to indicate the condition of the handshake and bit 107 informs the control processor whether the 107 flag has to be set.

DAV1 and DAV2. If both DAV1 and DAV2 are set to 1, bytes 1 and 2 contain the data in response to the previous command. Refer to the relevant commands in appendix A to get the detailed information on the interpretation of the data in bytes 1 and 2. Otherwise, they contain either the received data bits or the handshake detection status or both.

The least significant bit is the first bit received. The data bits are stored in byte 1 when DAV2 is 1 and DAV1 is 0. When DAV1 is 1 and DAV2 is 0, the control processor should ignore the data in byte 1 and get the detection status from byte 2. During handshake operations the TS75C96 reports the detection status regularly. When the rate sequence is received, it will be transferred in byte 1 of the response. Each bit in byte 2 indicates the detection of a specific event in the training sequence. It has different meanings for call and answer modems. For detailed information, refer to appendix B. During the data mode, byte 2 is always provided, but is used only when there are two bytes of data to transmit.

F00-F11 bits. During the call establishment operation, the TS75C96 reports call progress tones through the F01 and F00 flags. F00 is set to 1 when the signal energy in frequency band 1 is above the threshold level. F01 is set to 1 when the signal energy in band 2 is above the threshold level. Detection of the 2100Hz or 2225Hz answer tone is indicated by setting the F10 flag to a 1. During handshake operations, all four bits are used to indicate the line condition and some detection results. F01 is set to 1 if any segment in the training sequence is not detected within a time out. This bit can be used to indicate a non V.32 detection if either AA is not detected in the answer modem or the AC is not detected in the call modem. Both F00 and F01 are set to 1 when an illegal mode or a GSTN cleardown is received in the rate sequence.The detection of the rate sequence is reported in the flags F11 and F10. When the modem is operating at 9600bps without trellis coding, these bits are both set to 0. With trellis coding at 9600bps, F11 is set to 1 and F10 is cleared to 0. For 4800bps, 0 and 1 will be placed in F11 and F10, respectively.

USER INTERFACE - COMMAND SET (continued)

During data mode, the perceived line quality is reported in the flags F01 and F00. The line conditions are reported as either good (code 00), poor (code 01), or terrible (code 10). The code 10 should be interpreted as a local modem retrain request. Upon receipt of this code, the controller can issue the RTRA command to begin the retrain procedure. The code 11 is used when the remote modem begins a retrain sequence. The control processor is then responsible for manipulating the appropriate data communications interface signals.

H and 107 bits. When the TS75C96 is required to perform the CCITT handshake sequence, the H bit is set to 1 for the duration of the handshake. At the successful completion of the handshake operation the H flag will go to 0 and the control processor is then responsible for manipulating the appropriate data communications interface signals. e.g. 106 and 109.

The 107 flag is set to 1 to indicate that the controller should assert signal 107 on the data communication interface.

In FAX mode, the H bit can indicate a handshake in progress, either in the transmit path (transmitting segment 1 to 5 or A to B), or in the receiver.

C106, Clear To Send.
Tells the transmit section that the modem can sends bits of data. The bit stream of data can come from the TS7538 when the serial mode is enabled, or directly from the microcontroller in parallel mode.

C19F, Fast Carrier Detect.
Tells the receive section that a signal is present in the line. The threshold for detection is equal to the high level of the regular carrier detect.

C109, Carrier Detect.
Tells the receive section that a coherent V.29/V.27ter signal is present on the line. The high level for detection is set by default to -43dBm, the low level to -48dBm, the minimum hysteresis is 2dB. This signal is also used internally to clamp outgoing received data.

3 - COMMAND LIST

Operational Control Commands

Command Mnemonic	OP Code (HEX)	Description
UFZEC	170000	UnFreeZe Echo Canceller
FREZQ	1B0000	FREeZe the EQualizer adaptation
FRELC	160000	FREeZe the Echo Canceller adaptation
UFZEQ	1C0000	UnFreZe EQualizer
HSHK	040000	HandSHaKe with Other Modem
INIT	0600C0	NITialize modem
NOP	000000	No OPeration
RTRA	050000	ReTRAin
SCRM	18	Enable / Disable V.22bis SCRambler
SETGN	02	SET the scaling factor for the transmitter
STOP	19	Stop FAX Transmitter
SYNC	1A	Start FAX Receiver Synchronization

Data Communication Commands

Command Mnemonic	OP Code (HEX)	Description
XMIT	01	Transmit Data and Initiate Additional Transfer (in parallel data mode)
SERIAL	15	Transmit Data in SERIAL mode

MAFE Communication Commands

Command Mnemonic	OP Code (HEX)	Description
CMAFE	07	Configure MAFE Chipset
RRR1	080000	Read Mafe Reg RR1
RRR2	090000	Read Mafe Reg RR2
WTR1	0A	Write MAFE Reg TR1
WTR2	0B	Write MAFE Reg TR2

USER INTERFACE - COMMAND SET (continued)

TONE Select Commands

Command Mnemonic	OP Code (HEX)	Description
ANSW	0C1000	Select 2100Hz ANSWeR Tone
DTMF0	0C0000	Select DTMF Digit 0
DTMF1	0C0100	Select DTMF Digit 1
DTMF2	0C0200	Select DTMF Digit 2
DTMF3	0C0300	Select DTMF Digit 3
DTMF4	0C0400	Select DTMF Digit 4
DTMF5	0C0500	Select DTMF Digit 5
DTMF6	0C0600	Select DTMF Digit 6
DTMF7	0C0700	Select DTMF Digit 7
DTMF8	0C0800	Select DTMF Digit 8
DTMF9	0C0900	Select DTMF Digit 9
DTMF*	0C0E00	Select DTMF Digit *
DTMF#	0C0F00	Select DTMF Digit #
TONE	0C	Select TONE(s)

Configuration Control Commands

Command Mnemonic	OP Code (HEX)	Description
CV32	20	Configure Modem for V.32
CFAX	1F	Configure for FAX modes (V.29/V.27ter)
CFSK	1D	Configure Modem for FSK (V.23/V.21/Bell 103)
CV22B	1E	Configure Modem for V.22/V.22bis/ Bell 212A

Memory Manipulation Commands

Command Mnemonic	OP Code (HEX)	Description
SPAC	13	Write MEM and Increment MEM Pointer
SPAM	12	Write MEM
WARP	10	Write MEM and Pointer & Read MEM
WARPX	11	Write MEM and Pointer & Read MEM & MEM +1

TONE Control Commands

Command Mnemonic	OP Code (HEX)	Description
DEFT1	0E	Define Tone 1
DEFT2	0F	Define Tone 2
SLNT	0D0000	Transmit no Tone
TGEN0	0D0000	Tone Generators Disabled
TGEN1	0D0100	Tone Generator 1 Enabled
TGEN2	0D0200	Tone Generator 2 Enabled
TGEN12	0D0300	Tone Generators 1 & 2 Enabled

APPENDIX A : COMMAND SET DESCRIPTION

CFAX - Configure for FAX Modes

INSTRUCTION TYPE
Configuration control command

OPCODE
1F

SYNOPSIS
CFAX mode al atn

DESCRIPTION
CFAX is used to select the FAX mode of operation.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	1	1	1

BYTE 1 DEFINITION

0	0	EP1	EP0	0	M2	M1	M0

BIT		DEFINITION	
EP1	EP2	Echo protection tone	
0	0	no echo protection tone	
0	1	Short protection tone 30ms	
1	0	Long echo protection tone 190ms	
M2	M1	M0	FAX Mode
0	0	0	V.29 9600bps
0	0	1	V.29 7200bps
0	1	0	V.29 4800bps
1	0	0	V.27Ter 4800bps
1	0	1	V.27Ter 2400bps
1	1	0	V.27Ter 4800bps short train
1	1	1	V.27Ter 4800bps short train

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	0	0	LL	0

BIT	DEFINITION
ATN3 ... 0	Transmit Attenuation
LL	Carrier Detect Level
0	PSTN (43dBm/-48dBm)
1	Leased line (33dBm/-38dBm)

CFSK - Configure for FSK Modes

INSTRUCTION TYPE
Configuration control command

OPCODE
1D

SYNOPSIS
CFSK al orig atn mode ll

DESCRIPTION
CFSK is used to select the FSK mode of operation.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	1	0	1

BYTE 1 DEFINITION

0	0	0	0	AL	MOD1	MOD0	ORIG

BIT		DEFINITION
AL	0/1	Analog loopback disabled/enabled
ORIG	0/1	Answer mode/Originate mode
MOD1		MOD0
0		0 V.23
0		1 V.21
1		0 Bell 103

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	0	0	LL	0

BIT	DEFINITION
ATN3 ... 0	Transmit Attenuation (cF CV32)
LL	Leased line carrier detect
0	43dBm/-48dBm
1	33dBm/-38dBm

APPENDIX A : COMMAND SET DESCRIPTION (continued)

CMAFE - Configure the TS68950/1/2 components of the TS75C96

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
07

SYNOPSIS
CMAFE address register code data

DESCRIPTION
CMAFE is used to directly manipulate the operating parameters of the TS68950/1/2 components of the TS75C96. This is a low level command which allows the controller to alter such things as the transmit level, transmit timing, receive timing, and receiver parameters, etc. The command consists of a single byte OPcode followed by a byte containing the address code for the desired register and a data byte for the addressed register. The data bytes will be transferred in the order received and interpreted by the addressed device. Refer to the data sheets of the TS68950, TS68951, and TS68952 for programming specifics.

BYTE DEFINITION (OP CODE)

0	0	0	0	0	1	1	1

BYTE 1 DEFINITION

R	R	R	0	0	0	0	0

REG CODE (Refer to TS68950 Data Sheet).

BYTE 2 DEFINITION

*	*	*	*	*	*	*	*

DATA BYTE (Refer to TS68950 Data Sheet)

CV22B - Configure for CCITT V.22bis, CCITT V.22 and Bell 212A Modes

INSTRUCTION TYPE
Configuration control command

OPCODE
1E

SYNOPSIS
CV22B al mode orig atn LL guard fallback

DESCRIPTION
CV22B is used to select the CCITT V.22bis mode of operation. Select also, depending of Mode bits, the V.22, V.22 600bps and the Bell 212A.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	1	1	0

BYTE 1 DEFINITION

G1	G0	0	0	AL	MOD1	MOD0	ORIG

BIT		DEFINITION
AL	0/1	Analog loopback disabled/enabled
MOD1	MOD0	Select Mode
0	0	V.22bis 2400bps
0	1	V.22 1200bps
1	0	Bell 212A 1200bps
1	1	V.22 600bps
ORIG	0/1	Answer mode/Originate mode
G1	G2	Guard tone selection
0	0	No tone
0	1	550Hz
1	0	1800Hz

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	0	0	LL	FB

BIT	DEFINITION
ATN3-0	Transmit Attenuation (cF CV32)
FB	Fallback mode for V.22bis
0	disabled
1	enabled
LL	Leased line carrier detect
0	43dBm/-48dBm
1	33dBm/-38dBm

APPENDIX A : COMMAND SET DESCRIPTION (continued)

CV32 - Configure for V.32 Mode

INSTRUCTION TYPE
Configuration control command

OPCODE
20

SYNOPSIS
CV32 speed ec orig atn al fc

DESCRIPTION
CV32 is used to alter the operating parameters of the TS75C96. The passed parameters provide a two bit speed code (SP0 & SP1) which selects the desired baud rate. EC parameter explicitly turns on or off the echo canceller. If the TS75C96 is operating in the originate mode, the ORIG parameter must be set. When this parameter is not set, the TS75C96 is configured as an answer mode device. The Al parameter allows the user to select the analog loopback test conditions. The transmit attenuation level is selected by the ATN parameter. etc.

BYTE 0 DEFINITION (OP CODE)

0	0	1	0	0	0	0	0

BYTE 1 DEFINITION

RSV	RSV	FC	EC	AL	SP1	SP0	ORIG

Flag	Bit	Definition
RSV	-	Reserved
FC	0/1	Do not/Do force cleardown
EC	0/1	For end echo canceller off/on
AL	0/1	Analog Loopback test disabled/enabled
ORIG	0/1	Answer mode / Originate mode

SPEED CODE : SP1-0
00 : 9600 bps
10 : 9600 bps treillis
01 : 4800 bps
11 : 2400 bps

BYTE 2 DEFINITION

ATN3	ATN2	ATN1	ATN0	RSV	RSV	RSV	RSV

Flag	Bit	Definition
ATN	3-0	Transmit attenuation 0dB to 22dB : codes 0000 to 1011 in 2dB steps Infinite : codes 1100 to 1111
RSV	-	Reserved

APPENDIX A : COMMAND SET DESCRIPTION (continued)

DETF1 - Define Tone 1

INSTRUCTION TYPE
Tone control command

OPCODE
0E

SYNOPSIS
DEFT tone descriptor

DESCRIPTION
DEFT1 is a command which used to program tone generator 1. The 16 bit value provided is used as the phase offset per sample for the generator. The DEFT1 command does not enable the tone generator. See also TGEN.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	0

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR

DETF2 - Define Tone 2

INSTRUCTION TYPE
Tone control command

OPCODE
0F

SYNOPSIS
DEFT tone descriptor

DESCRIPTION
DEFT2 is a command which used to program tone generator 2. The 16 bit value provided is used as the phase offset per baud for the generator. The DEFT2 command does not enable the tone generator. See also TGEN.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	1	1

BYTE 1 DEFINITION

P7	P6	P5	P4	P3	P2	P1	P0

LOW BYTE OF DESCRIPTOR

BYTE 2 DEFINITION

P15	P14	P13	P12	P11	P10	P9	P8

HI BYTE OF DESCRIPTOR

Example : f = 1kHz frequency

$$P = \frac{32768 \cdot F}{3600} = 9102 = \$\ 238E$$

Note : Frequencies over 3kHz are attenuated.

APPENDIX A : COMMAND SET DESCRIPTION (continued)

FREZ - Freeze the Equalizer or Echo Canceller Adaptation

INSTRUCTION TYPE
Operational control command

OPCODES
16/17/1B/1C

SYNOPSIS
FREZ freeze code

DESCRIPTION
FREZ causes the TS75C96 to enable or disable the adaptation of the equalizer and / or the echo canceller, according to the parameter provided.

FREZ includes four different opcodes, each one with a specific option :

Frezc (16) : Freeze the echo canceller adaptation
uFzec (17) : Unfreeze the echo canceller
Frezq (1B) : Freeze the equalizer adaptation
uFzeq (1C) : Unfreeze the equalizer

HSHK - Begin Handshake Sequence

INSTRUCTION TYPE
Operational control command

OPCODE
040000

SYNOPSIS
HSHK

DESCRIPTION
HSHK is used to command the TS75C96 to begin the handshake sequence processing. The progress of the handshake is reported to the control processor along with the data bits. For detailed information, refer to appendix B.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	0

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

LOW BYTE OF DESCRIPTOR

BYTE 2 DEFINITION

0	0	0	0	0	0	0	EA

EA : V.25bis (answer only)
0 Start handshake while enabling V.25bis answer tone generation
1 Start handshake whithout enabling V.25bis answer tone generation

APPENDIX A : COMMAND SET DESCRIPTION (continued)

INIT - Initialize the TS75C96

INSTRUCTION TYPE
Operational control command

OPCODE
060000

SYNOPSIS
INIT

DESCRIPTION
INIT forces the TS75C96 to reset all parameters to their default conditions and restart operations.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	1	0

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

NOP - No Operation is Specified

INSTRUCTION TYPE
Operational control command

OPCODE
000000

SYNOPSIS
NOP

DESCRIPTION
NOP is used when communications with the TS75C96 are required but no particular action is desired.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	0

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX A : COMMAND SET DESCRIPTION (continued)

RRR1 - Read MAFE Register RR1

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
080000

SYNOPSIS
RRR1

DESCRIPTION
RRR1 causes the TS75C96 to read the 12 bit contents of the MAFE chipset register RR1. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	0

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

RRR2 - Read MAFE Register RR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
090000

SYNOPSIS
RRR2

DESCRIPTION
RRR2 causes the TS75C96 to read the 12 bit contents of the MAFE chipset register RR2. The data is returned in a standard three byte format. The least significant data byte is returned in byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Consult the data sheet of the TS68951 for the specifics of the returned data.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	0	1

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX A : COMMAND SET DESCRIPTION (continued)

RTRA - Force a Retrain of the V.32 Engine

INSTRUCTION TYPE
Operational control command

OPCODE
050000

SYNOPSIS
RTRA fall

DESCRIPTION
RTRA is used to force the TS75C96 to initiate a retrain sequence on the channel.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	1	0	1

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	FALL

Fallback (V.22bis only)
1 Fallback to 1200Bps
0 goes up to 2400Bps

SCRM - Enable/Disable V.22bis Scrambler

INSTRUCTION TYPE
Operational control command

OPCODE
180000

SYNOPSIS
SCRM enable disable

DESCRIPTION
SCRM is a command which is used activate or deactivate the V.22bis/V.22 transmit scrambler.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	1	0	1

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	TS

TS
0 Scrambler disabled
1 Scramble enabled

APPENDIX A : COMMAND SET DESCRIPTION (continued)

SERIAL - Configure Serial Data Port

INSTRUCTION TYPE

Data communication command disable/enable and configure TS7538

OPCODE

15

SYNOPSIS

SERIAL subopcode value, subopcode argument (see TS7538 datasheet).

DESCRIPTION

BYTE 1

0 : Set mode to synchronous parallel (defauft).
1 : Enable serial mode (TS7538).
2 : Modify TS7538 register CR0.
3 : Modify TS7538 register CR1.
4 : Reserved.
5 : Modify TS7538 register CR3.

BYTE 2

0 : Byte 2 must be 0.
1 : Byte 2 contains the IRQ ratio from 0 to 255 (respectively 1 IRQ 2400 times per second to 1 IRQ 2400/256 times per second).
2 : D0 must be 0.
D1 digital loop back.
D2 enable Rx ata output.
D3 must be 0.
D4 ... D7 data speed :
3 : 9600
5 : 4800
6 : 2400
7 : 1200
8 : 600
9 : FSK
3 : D0 ... D3 must be 0.
D4 extended overspeed.
D5 ... D6 character lenght :
0 : 8 bit
1 : 9 bit
2 : 10 bit
3 : 11 bit
D7 synchronous/asynchronousmode.

SETGN - Set Global Gain Factor

INSTRUCTION TYPE

Operational control command

OPCODE

02

SYNOPSIS

STEGN gain value

DESCRIPTION

SETGN is a command which used to scale the transmit samples. The 16 bit value provided is the multiplicative constant to be multiplied with each transmit sample (initial value is 7FFF).

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	1	0

BYTE 1 DEFINITION

G7	G6	G5	G4	G3	G2	G1	G0

LOW BYTE OF GAIN VALUE

BYTE 2 DEFINITION

G15	G14	G13	G12	G11	G10	G9	G8

HI BYTE OF GAIN VALUE

APPENDIX A : COMMAND SET DESCRIPTION (continued)

SPAC - Store Parameter And Count

INSTRUCTION TYPE
Memory manipulation command

OPCODE
13

SYNOPSIS
SPAC low byte high byte

DESCRIPTION
SPAC is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. The content of the Memory Address Register is incremented by 1 at the completion of command execution. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA

SPAM - Store Parameter in Addressed Memory

INSTRUCTION TYPE
Memory manipulation command

OPCODE
12

SYNOPSIS
SPAM low byte high byte

DESCRIPTION
SPAM is a command which used to write an arbitrary 16 bit value into the writable memory location currently specified by the Memory Address Register. See also WARP.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	1	0

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

LOW BYTE OF DATA

BYTE 2 DEFINITION

D15	D14	D13	D12	D11	D10	D9	D8

HI BYTE OF DATA

APPENDIX A : COMMAND SET DESCRIPTION (continued)

STOP - Stop FAX Transmitter

INSTRUCTION TYPE
Operational control command

OPCODE
19

SYNOPSIS
STOP

DESCRIPTION
STOP is used to stop transmitting FAX signal generating the segment A, segment B, according with the V.27ter CCITT specification. In V.29 mode the transmit signal is immediatly stopped after receiving this command.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	0	0	1

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

LOW BYTE OF DATA

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

SYNC - Start FAX Receiver Synchronization

INSTRUCTION TYPE
Operational control command

OPCODE
1A

SYNOPSIS
SYNC

DESCRIPTION
SYNC is used to Arm the receiver to detect the FAX synchronizing signal as describe in the V.27 and V.29 CCITT specification. Depending on whether the short train option is selected by the CFAX command, the receiver will use fast training for the equalizer (V.27ter only).

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	1	0	1	0

BYTE 1 DEFINITION

0	0	0	0	0	0	0	0

LOW BYTE OF DATA

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX A : COMMAND SET DESCRIPTION (continued)

TGEN - Enable and Disable Tone Generators

INSTRUCTION TYPE
Tone control command

OPCODE
0D

SYNOPSIS
TGEN tg code

DESCRIPTION
TGEN causes the TS75C96 to enable or disable tone generator 1 and tone generator 2, according to the parameter provided.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	1

BYTE 1 DEFINITION (TONE CODE)

0	0	0	0	0	0	TGC2	TGC1

TG CODE TGC2-1	TONE GEN 1	TONE GEN 2
00	Disabled	Disabled
01	Enabled	Disabled
10	Disabled	Enabled
11	Enabled	Enabled

TONE - Select and Transmit Tone(s)

INSTRUCTION TYPE
Tone select and command

OPCODE
0C

SYNOPSIS
TONE tone code

DESCRIPTION
TONE causes the TS75C96 to program the tone generators for the specified tone or tones. The tones are defined by the tone code parameter passed in the second byte of the command. See also tonetab for the predefined single and double tones, and the commands DEFT and TGEN for user definable tones and tone generator control.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	1	0	0

BYTE 1 DEFINITION

0	0	0	T4	T3	T2	T1	T0

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

Tone Code	Tone Parameters
0	DTMF 0 (941 & 1336Hz)
1	DTMF 1 (697 & 1209Hz)
2	DTMF 2 (697 & 1336Hz)
3	DTMF 3 (697 & 1477Hz)
4	DTMF 4 (770 & 1209Hz)
5	DTMF 5 (770 & 1336Hz)
6	DTMF 6 (770 & 1477Hz)
7	DTMF 7 (852 & 1209Hz)
8	DTMF 8 (852 & 1336Hz)
9	DTMF 9 (852 & 1477Hz)
A	DTMF A (697 & 1633Hz)
B	DTMF B (770 & 1633Hz)
C	DTMF C (852 & 1633Hz)
D	DTMF D (941 & 1633Hz)
E	DTMF * (941 & 1209Hz)
F	DTMF # (941 & 1477Hz)
10	Answer tone (2100Hz)

APPENDIX A : COMMAND SET DESCRIPTION (continued)

WARP - Write Address & Return Parameter

INSTRUCTION TYPE
Memory manipulation command

OPCODE
10

SYNOPSIS
WARP address

DESCRIPTION
WARP is a command which is used to write the Memory Address Register of the TS75C96. The TS75C96 responds with the contents of the addressed location. The data is returned in a standard three byte transfer. The least significant data byte is returned in the byte 1, followed by the most significant data byte. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	0

BYTE 1 DEFINITION (TONE CODE)

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

PROC CODE P1-0	MEM CODE M1-0	ADDRESS HI A11-A8
00 : Master	00 : XRAM	
10 : Receiver	01 : YRAM	
01 : Echo Canceller	10 : EMEM	
	11 : CROM	

WARPX - Write Address & Return Complex Parameter

INSTRUCTION TYPE
Memory manipulation command

OPCODE
11

SYNOPSIS
WARPX address

DESCRIPTION
WARPX is a command which is used to write the Memory Address Register of the TS75C96. The TS75C96 responds with the contents of the most significant bytes of the addressed location and the addressed location +1. The data is returned in a standard three byte transfer. Byte 0 is the standard response format (refer to appendix B) with DAV1 and DAV2 bits set to 1. Byte 1 is used to return the 8 most significant bits contained in the addressed location. The most significant bits of the addressed location +1 are returned in byte 2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	1	0	0	0	1

BYTE 1 DEFINITION (TONE CODE)

A7	A6	A5	A4	A3	A2	A1	A0

LOW BYTE OF DATA

BYTE 2 DEFINITION

P1	P0	M1	M0	A11	A10	A9	A8

PROC CODE P1-0	MEM CODE M1-0	ADDRESS HI A11-A8
00 : Master	00 : XRAM	
10 : Receiver	01 : YRAM	
01 : Echo Canceller	10 : EMEM	
	11 : CROM	

APPENDIX A : COMMAND SET DESCRIPTION (continued)

WTR1 - Write MAFE Register TR1

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0A

SYNOPSIS
WTR1

DESCRIPTION
WTR1 causes the TS75C96 to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR1.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	0

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

WTR2 - Write MAFE Register TR2

INSTRUCTION TYPE
MAFE manipulation command

OPCODE
0B

SYNOPSIS
WTR2

DESCRIPTION
WTR2 causes the TS75C96 to take the two supplied data bytes and write them in sequence to the MAFE chipset register TR2.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	1	0	1	1

BYTE 1 DEFINITION (DATA)

D3	D2	D1	D0	0	0	0	0

BYTE 2 DEFINITION (DATA)

D11	D10	D9	D8	D7	D6	D5	D4

APPENDIX A : COMMAND SET DESCRIPTION (continued)

XMIT - Transmit data to other modem

INSTRUCTION TYPE
Data communication command

OPCODE
01

SYNOPSIS
XMIT data

DESCRIPTION
XMIT is used to command the TS75C96 to send data. The OP code for the XMIT command is a single byte. The data bits to be transmitted are stored in the second byte, where D0 is the first bit to be transmitted.

This command is not active when SERIAL mode is declared.

BYTE 0 DEFINITION (OP CODE)

0	0	0	0	0	0	0	1

BYTE 1 DEFINITION

D7	D6	D5	D4	D3	D2	D1	D0

D0-D7 DATA BITS

BYTE 2 DEFINITION

0	0	0	0	0	0	0	0

APPENDIX B : STATUS REPORTING DESCRIPTION

STATUS WORD FORMAT

The three bytes sent from the data pump, make reference to different information. The bits D3 and D2 define the corresponding format as follows :

X	X	X	X			X	X

Status Word Format :

0 0 : reserved
0 1 : Mode status word in byte 1 and 2
1 0 : Byte of receive data in byte 1
1 1 : Answer to a command in byte 1 and 2

Refer to page 34 for answer status word format. Refer receive data format.

After selecting the modem standard with a configuration command, either **CV32** for V.32 mode or **CV22B** for V.22bis/V.22/Bell212A modes or **CFSK** for V.23/V.21/Bell103 modes, the data pump goes into the next state and sets the transmit and receive parts to send and detect different events. Note that the transition from **Call Establish** to **V.32 Call** is equivalent to a reset or **INIT** command for the detectors, IRQ rate etc. and so all parameters are reset to their default value.

STATE MACHINE

The TS75C96 data pump can be seen as a state machine. Depending on the current state the modem status word reflects different information. Transitions between states are obtained either by sending a command or by internal detection events.

Where : words in ***italic*** are regular commands. **Boxes** are state names. **End of handshake** is signaled by a falling transition of the H Bit (D1 of Byte 0). **Remote retrain detected** is signaled by a rising transition of the H bit (D1 of Byte 0).

After an **INIT** command or a hardware RESET, the data pump goes into the Call Establish State. In that state the data pump can generate tones, for dialling, and detect Call Progress Tones and/or Answer Tone. One can note that all 4 tone detectors can be changed if needed.

DETECTORS

Call Progress Tone Detectors 1 and 2

These two tone detectors are always enabled, even during Handshake or Data Mode. Their coefficients can be changed to support a wide range of requirements for different countries. These detectors are composed of a common prefilter followed by two separate 4th order IIR filters. The two outputs of these filters are rectified and filtered by a low pass filter whose output is compared with a threshold. Bits B1 (D4 of Byte 1) and B2 (D5 of Byte 1) give the information that the level is higher than the threshold. In addition to these two bits, Bit B21 (D3 of Byte 1) gives the information that the level out of the filter 2 is greater than the level out of filter 1. Refer to Appendix C for default templates.

Answer Tone Detectors 1 an 2

These two tone detectors must be used for answer tone recognition. They are composed by two independant 6th order IIR filters. Refer to Appendix D for default templates.

AC Tone Detector

This detector is only active in the **V.32 Call** State when in **Originate** mode. Note that this bit is a fugitive signal, and can be lost if the IRQ rate is not 1 over 2400.

Circuit 107 on/off

This signal is set near the end of the handshake, according to the CCITT specification.

Handshake in Progress

This signal, called the H bit, informs the microcontroller that a handshake (or retrain) is in progress. At the end of the Handshake it goes low and so defines the transition from **Handshake State** to **Data State**. When in data mode, if a remote retrain is detected, the H bit goes high and defines the transition from **Data State** to **Handshake State**.

Timeout

When in **V.32 Handshake State** a Timeout can occur while waiting for an **AC** or **AA** sequence. The timeout value is set to 13 sec.

Cleardown

A cleardown detect can occur when :
- The remote Modem sends a Cleardown to Stop the connection.
- Both Modems have no common mode of exchanging data. This event can occur in **R1**, **R2**, **R3** or **E** CCITT V.32 segment.

Rate Negotiation

The last rate negotiation value of the Bits D7, D6 of Byte 0, before the H Bit goes low, define the data exchange rate and format.

APPENDIX B : STATUS REPORTING DESCRIPTION

Handshake Detection Monitoring

The third byte of the modem status word indicates, during **Handshake States**, where the state machine is in the handshaking sequence.

Circuit 109 on/off

For V.22bis/V.22/Bell 212A/V.21/Bell 103 operation, this signal (also called **Carrier Detect**) indicate the presence or absence of a carrier in the corresponding mode.

Unscrambled 1

For V.22bis/V.22/Bell 212A this signal (**Usc1**) detects an unscrambled "1" sequence at 1200bps in the receive path.

Scrambled 1

For V.22bis/V.22/Bell212A this signal (**Sc1**) detects a scrambled bit sequence of receive "1", depending of the receive speed (2400 or 1200bps). Note that this signal can be active during handshake while detecting unscrambled "1" as defined by bit **Usc1**.

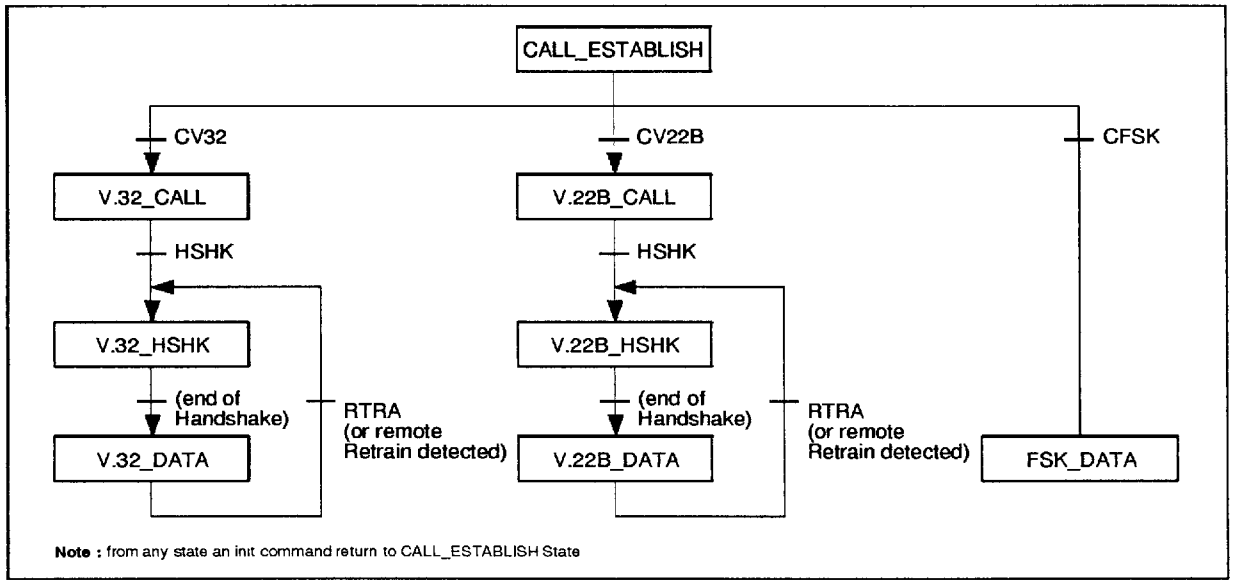
S1

This signal detects a S1 signal as defined in the CCITT V.22Bis specification (binary unscrambled "1000.." at 1200bps). Note that S1 and Usc1 detectors directly process the receive signal and does not depend on the receive bit speed. Scrambled 1 processes the receive bit stream and so depends on the receive speed (2400 or 1200bps).

Line Quality

This two-bit signal gives information on the quality of the line such as noise level, amplitude and phase distortion etc. for V.32 (9600 TCM) mode, on flat line : **good** is signal to noise ratio > 23dB ; **poor** is signal to noise ratio 22dB ; **terrible** is signal to noise ratio < 15dB.

Figure 9 : State Diagram



APPENDIX B : STATUS REPORTING DESCRIPTION

COMMAND ANSWER STATUS WORD

D7			Byte 0				D0
X	X	X	X	1	1	X	X

Flag

D7			Byte 1				D0

Low Byte (LSB) for WARP, RR1, RR2
Real part MSB for WARPX

D7			Byte 2				D0

High Byte (MSB) for WARP, RR1, RR2
Immaginary part MSB for WARPX

DATA STATUS WORD

D7			Byte 0				D0
X	X	X	X	1	0	X	X

Flag

D7			Byte 1				D0
						,	

Receive Byte of Data

D7			Byte 2				D0
						,	

Reserved

CALL ESTABLISH STATUS WORD

D7			Byte 0				D0
X	ANSW	B2	B1	0	1	0	X

ANSW : Answer tone detected (answer 1 or 2)
B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected

D7			Byte 1				D0
ANS1	ANS2	B2	B1	B21	0	0	0

AN1 : Answer tone 1 detected (2100Hz)
AN2 : Answer tone 2 detected (2225Hz)
B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected
B21 : Band 2 level greater than band 1

D7			Byte 2				D0
X	X	X	X	X	X	X	X

V.32 CALL STATUS WORD

D7			Byte 0				D0
AC	X	B2	B1	0	1	0	X

AC : AC sequence detected (V.32)
B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected

D7			Byte 1				D0
X	X	B2	B1	B21	0	0	0

B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected
B21 : Band 2 level greater than band 1

D7			Byte 2				D0
X	X	X	X	X	X	X	X

V.32 HSHK STATUS WORD

D7			Byte 0				D0
(1)	(1)	(2)	(2)	0	1	H	C107

C107 : Circuit 107 on/off
H : Handshake in progress (set to 1)
(1) : Handshake event :
1 0 : Timeout
1 1 : Cleardown
(2) Rate negociation :
0 0 : 9600 QAM
0 1 : 4600
1 0 : 9600 QAM trellis

D7			Byte 1				D0
X	X	B2	B1	B21	0	0	0

B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected
B21 : Band 2 level greater than band 1

D7			Byte 2				D0

Handshake Detection Monitoring

	ANSWER	ORIGINATE
00000000		
10000000	AA	AC
11000000	AA - CC	AC - CA
11100000	Silence	CA - AC
11110000	S	S
11111000	S - SBar	S - SBar
11111100	R2	R1
11111110	R3	-
11111111	E	E

APPENDIX B : STATUS REPORTING DESCRIPTION

V.32 DATA STATUS WORD

D7			Byte 0				D0
X	X	(1)	(1)	0	1	H	C107

C107 : Circuit 107 on/off
H : Handshake in progress (set to 1)
(1) : Line Quality :

0	0	: Good
0	1	: Poor
1	0	: Line terrible
1	1	: Remote retrain detected

D7			Byte 1				D0
X	X	B2	B1	B21	X	X	X

B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected
B21 : Band 2 level greater than band 1

D7			Byte 2				D0
X	X	X	X	X	X	X	X

Reserved

FAX HSHK STATUS WORD (First)

D7			Byte 0				D0
C19F	C106	X	X	0	1	H	C109

C19F : Fast carrier detect
C106 : Clear to send
C109 : Carrier detect
H : Handshake in progress (set to 1)

D7			Byte 1				D0
X	X	B2	B1	B21	X	X	X

B1 : Call progress tone 1
B2 : Call progress tone 2
B21 : Band 2 greater band 1

D7			Byte 2				D0

Handshake Detection Monitoring
10000000 Segment 3 detected
11000000 Segment 4 detected

FAX HSHK STATUS WORD (Second)

D7			Byte 0				D0
C19F	C106	Q1	Q0	0	1	H	C109

C19F : Fast carrier detect
C106 : Clear to send
C109 : Carrier detect
H : H = 0 data mode
Q1, Q0 : Line Quality :

0	0	: Good
0	1	: Poor
1	0	: Line terrible

D7			Byte 1				D0
X	X	B2	B1	B21	X	X	X

B1 : Call progress tone 1
B2 : Call progress tone 2
B21 : Band 2 greater band 1

D7			Byte 2				D0
X	X	X	X	X	X	X	X

Reserved

V.22bis CALL STATUS WORD

D7			Byte 0				D0
X	X	B2	B1	0	1	0	X

B1 : Call progress tone 1
B2 : Call progress tone 2

D7			Byte 1				D0
X	X	B2	B1	B21	0	0	0

B1 : Call progress tone 1
B2 : Call progress tone 2
B21 : Band 2 greater band 1

D7			Byte 2				D0
X	X	X	X	X	X	X	X

APPENDIX B : STATUS REPORTING DESCRIPTION

V.22bis HSHK STATUS WORD

D7			Byte 0				D0
X	X	0	0	0	1	H	C109

C109 : Circuit 109 on/off
H : Handshake in progress (set to 1)
X : Rate negociation :
0 0 : 2400 QAM
0 1 : 1200

D7			Byte 1				D0
X	X	B2	B1	B21	S1	Scr1	Usc1

B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected
B21 : Band 2 level greater than band 1
S1 : S1 signal detected
Scr1 : Scrambled 1 detected
Usc1 : Unscrambled 1 detected

D7			Byte 2				D0
X	X	X	X	X	X	X	X

Handshake Detection Monitoring

	ANSWER	ORIGINATE
00000000		
10000000	-	Unscr 1
11000000	S1	S1
11100000	Scr 1 (1200)	Scr 1 (1200)
11110000	Scr 1 (2400)	Scr 1 (2400)

V.22bis DATA STATUS WORD

D7			Byte 0				D0
X	X	(1)	(1)	0	1	H	C109

C109 : Circuit 109 on/off
H : Handshake in progress (set to 1)
(1) : Line quality :
0 0 : Good
0 1 : Poor
1 0 : Line terrible

D7			Byte 1				D0
X	X	B2	B1	B21	S1	Scr1	Usc1

B1 : Call progress tone 1 detected
B2 : Call progress tone 2 detected
B21 : Band 2 level greater than band 1
S1 : S1 signal detected
Scr1 : Scrambled 1 detected
Usc1 : Unscrambled 1 detected

D7			Byte 2				D0
X	X	X	X	X	X	X	X

Reserved

FSK DATA STATUS WORD

D7			Byte 0				D0
X	X	0	0	0	1	0	C109

C109 : Circuit 109 on/off

D7			Byte 1				D0
X	X	B2	B1	B21	X	X	X

B1 : Call progress tone 1
B2 : Call progress tone 2
B21 : Band 2 greater band 1

D7			Byte 2				D0
X	X	X	X	X	X	X	X

Reserved

APPENDIX C : This appendix shows the Call Progress Tone Detectors default set-up

Figure 10 : Band 1 Tone Detector

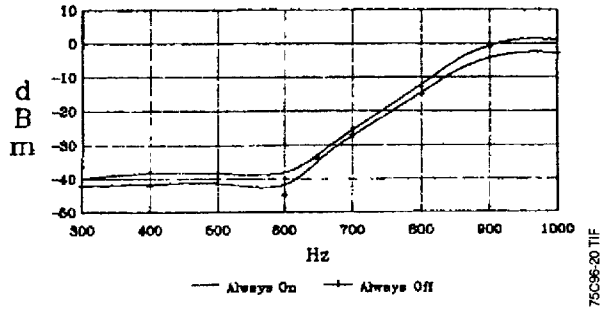
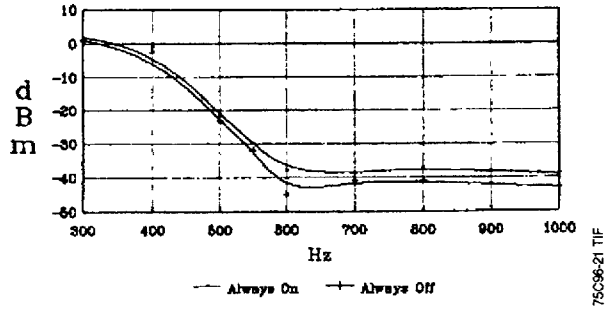


Figure 11 : Band 2 Tone Detector



APPENDIX D : This appendix shows the Answer Tone Detectors default set-up

Figure 12 : 2100 Answer Tone Detector

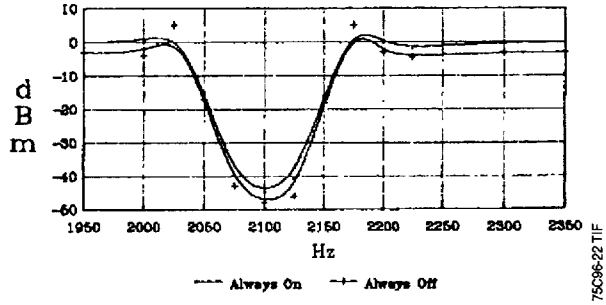
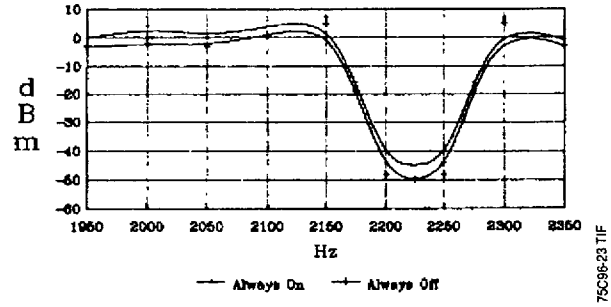
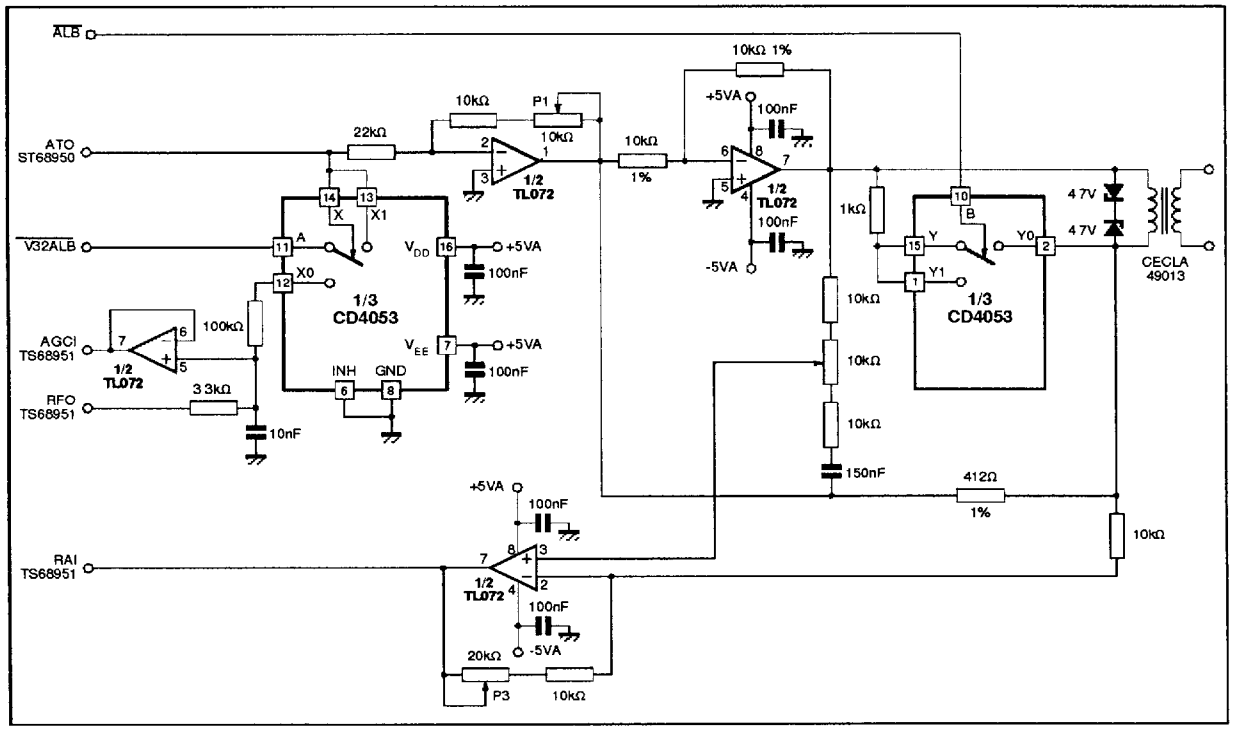


Figure 13 : 2225 Answer Tone Detector



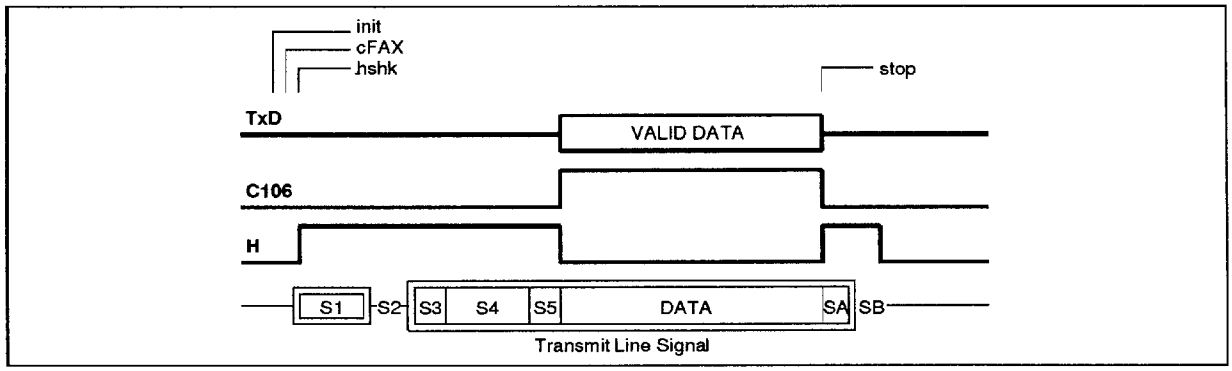
APPENDIX E : This appendix shows an example of hybrid line interface (for more details, refer to application notes)

Figure 14 : Hybrid/Line Interface Example



APPENDIX F : Fax Information

Figure 15 : FAX Transmitter Sequence



Segment Duration

Mode	S1	S2	S3	S4	S5	SA	SB	Unit
V.29 9600								
V.29 7200								
V.29 4800								

APPENDIX F : Fax Information (Continued)

Figure 16 : FAX Receiver Sequence

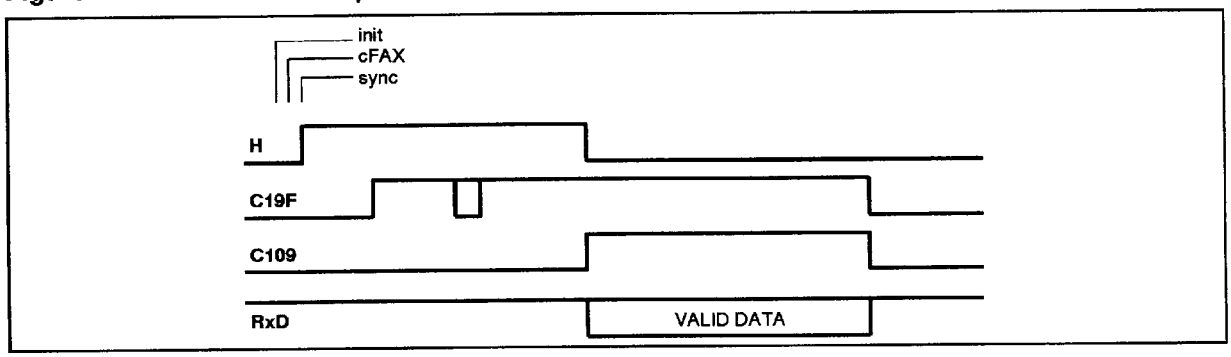
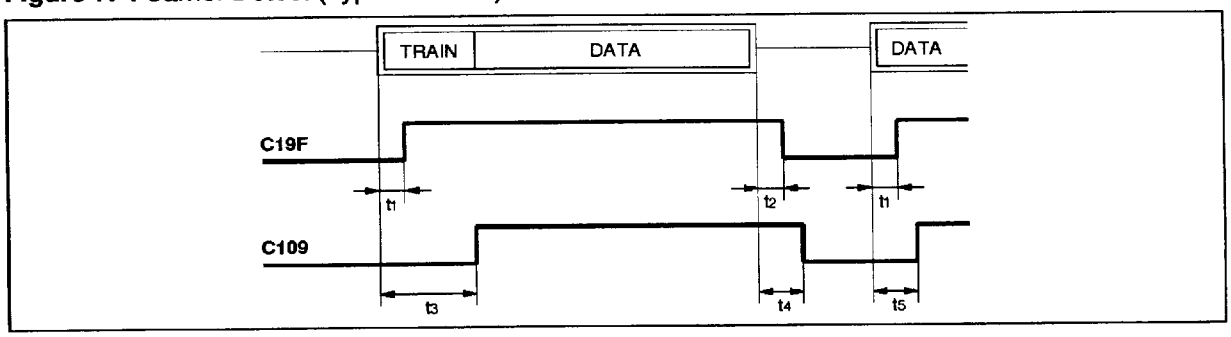


Figure 17 : Carrier Detect (Typical Values)



APPENDIX G : References

1. CCITT recommendation V.32

2. CCITT recommendation V.54

3. Data Sheet of the TS75320, V.32 modem echo canceller, SGS-THOMSON Microelectronics

4. Data Sheet of the ST18930/31 programable signal processor, SGS-THOMSON Microelectronics

5. Data Sheet of TS68950 transmitter interface chip, SGS-THOMSON Microelectronics

6. Data Sheet of TS68951 receiver interface chip, SGS-THOMSON Microelectronics

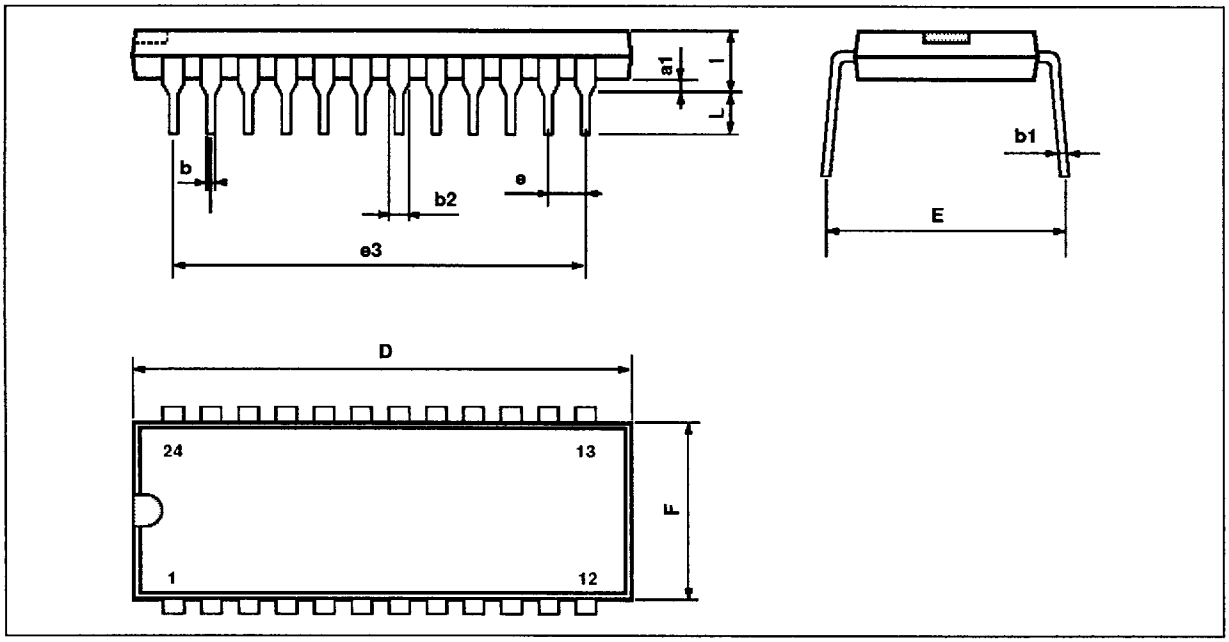
7. Data Sheet of TS68952 clock generation chip, SGS-THOMSON Microelectronics

8. Data Sheet of TS7538 async-sync converter, SGS-THOMSON Microelectronics

9. Data Sheet of TS75C32 V.32 modem chip set, SGS-THOMSON Microelectronics

10. Application notes: TS75C32, SGS-THOMSON Microelectronics

PACKAGE MECHANICAL DATA
24 PINS - PLASTIC DIP



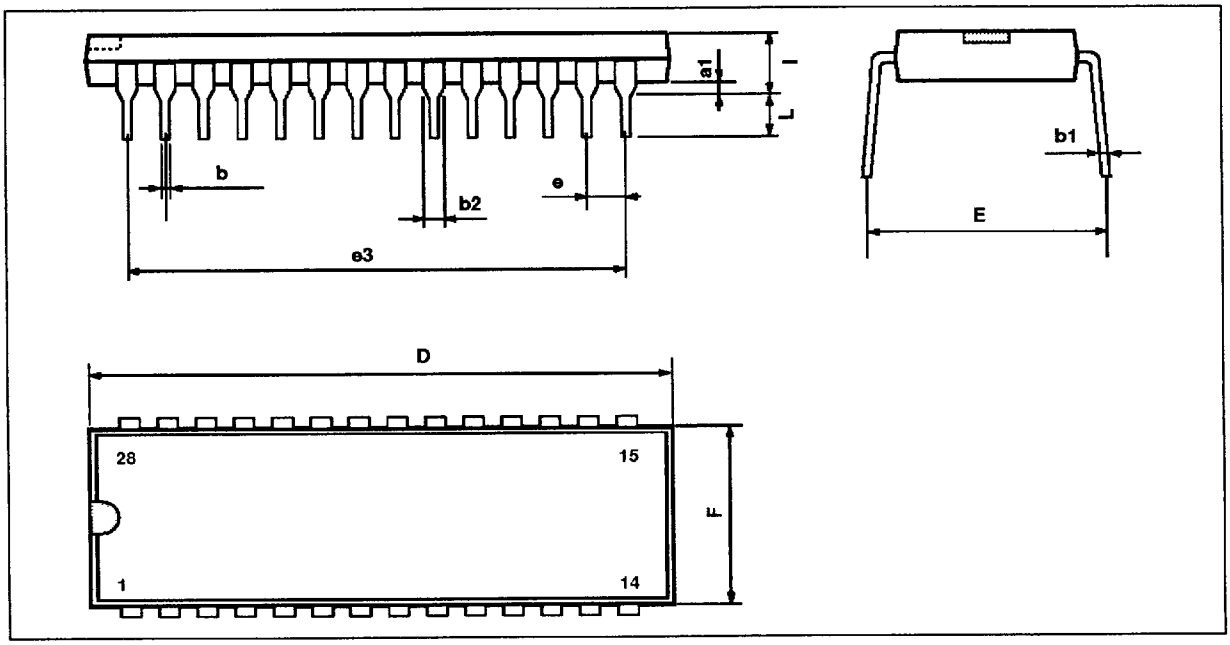
PM-DIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP24.TBL

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



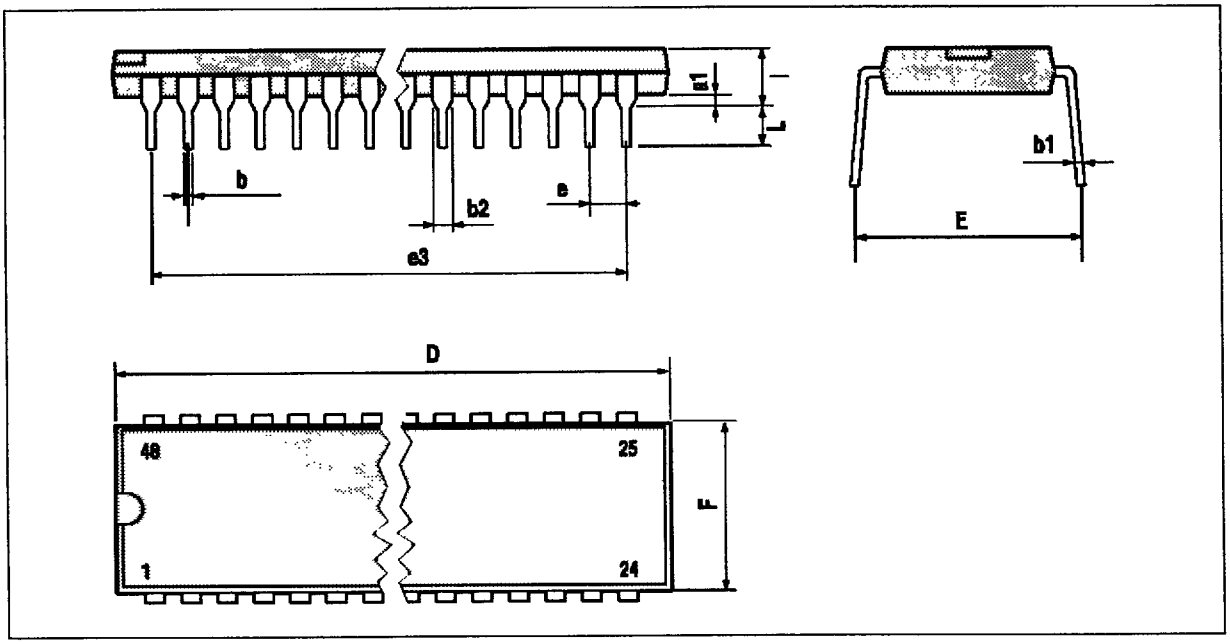
PM-DIP28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.4			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP28.TBL

PACKAGE MECHANICAL DATA

48 PINS - PLASTIC DIP



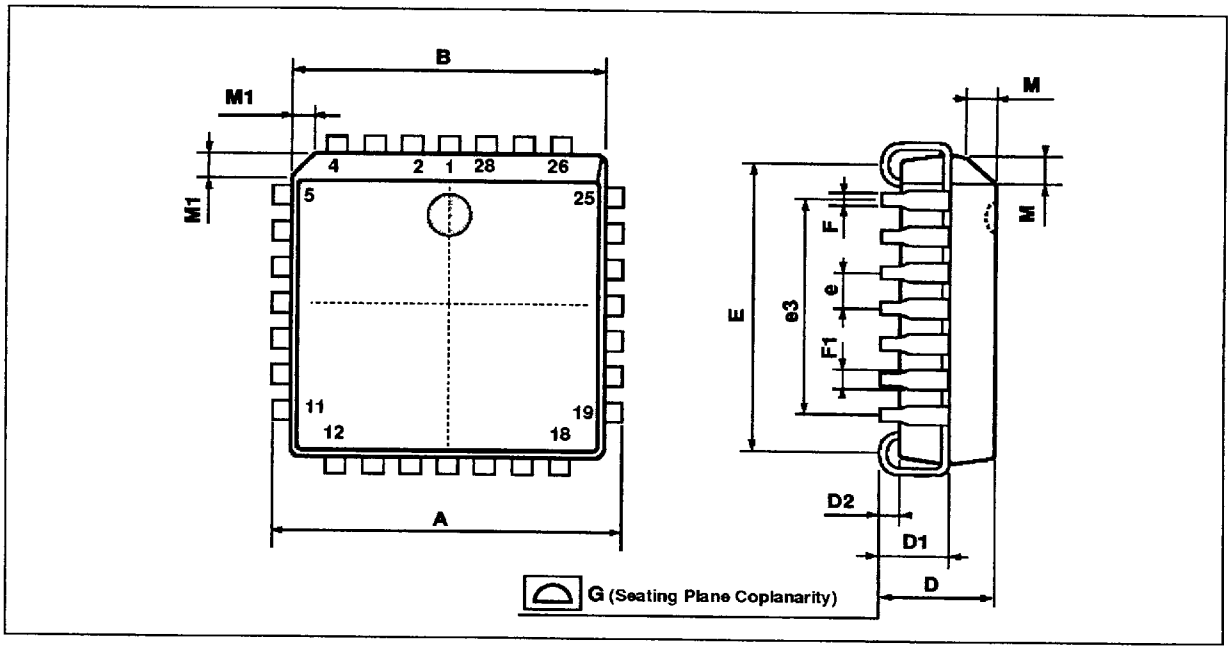
PM-DIP48.WMF

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			62.74			2.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		58.42			2.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP48.TBL

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC CHIP CARRIER

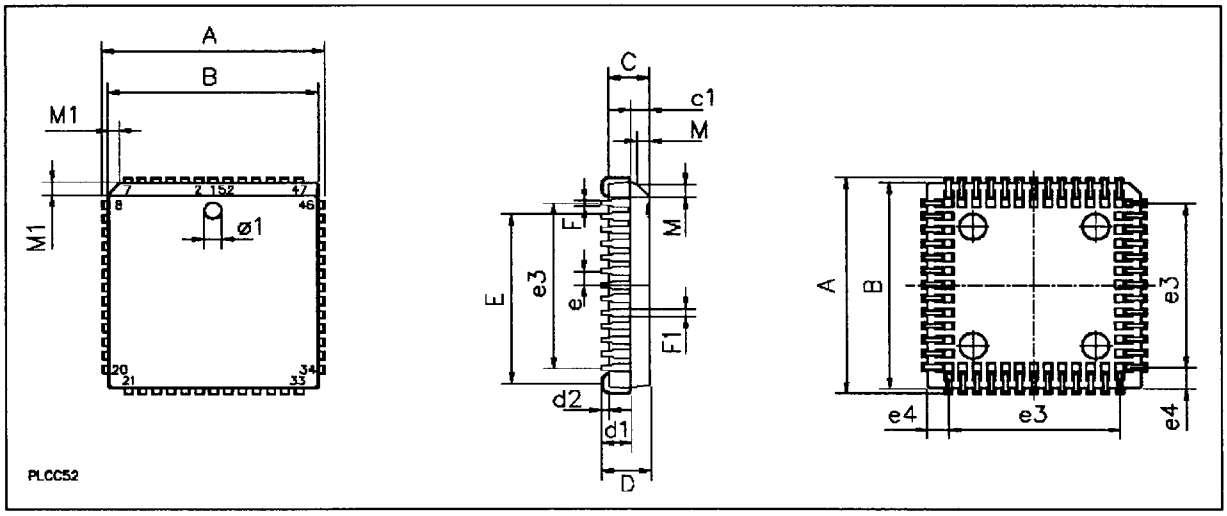


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

PLCC28 TBL

PACKAGE MECHANICAL DATA

52 PINS - PLASTIC CHIP CARRIER



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		4.20	5.08		0.165	0.20
A1		0.51			0.020	
A3		2.29	3.30		0.090	0.13
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C	0.25			0.01		
D		19.94	20.19		0.785	0.795
D1		19.05	19.20		0.750	0.756
D2		17.53	18.54		0.690	0.730
D3	15.24			0.60		
E		19.94	20.19		0.785	0.795
E1		19.05	19.20		0.750	0.756
E2		17.53	18.54		0.690	0.730
E3	15.24			0.60		
e	1.27			0.05		
L		0.64			0.025	
L1		1.53			0.060	
M		1.07	1.22		0.042	0.048
M1		1.07	1.42		0.042	0.056

PLCC52 TBL