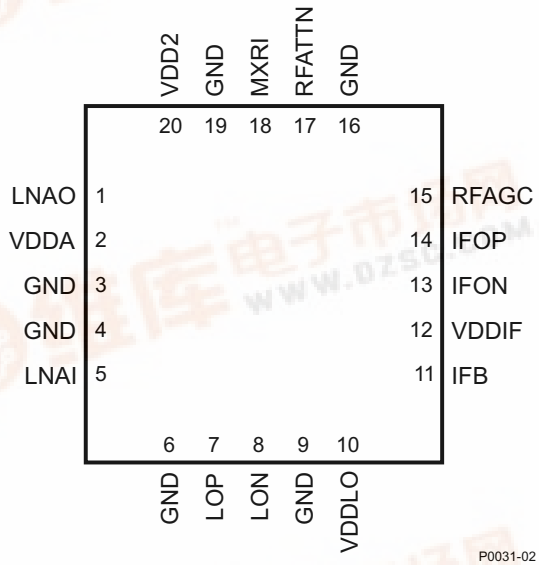
3.5-GHz, HIGH DYNAMIC RANGE, LOW-NOISE DOWN-CONVERTER

FEATURES

- Performs First Down-Conversion in 3.5-GHz Radios (3300–3800 MHz)
- Integrated LNA/Mixer/IF Amp/LO Buffer
- Provision for External Image Reject/Band-Pass Filter
- Low Noise-Figure/High Linearity
- Digital 10-dB Attenuator for High-Level Signals
- Frequency Range: 3.3–3.8 GHz
- 28 dB of Gain with 20 dB of Gain Control (10-dB Fixed)
- 2.5-dB Noise Figure, Typical
- LO Drive Level = 0 dBm, Typical

DEVICE INFORMATION

RGP PACKAGE
(TOP VIEW)



DESCRIPTION

The TRF1216 is the first of two integrated circuits used in the receiver section of Texas Instruments' 3.5-GHz radio chipset. The TRF1216 down-converts the 3.5-GHz input frequency to an intermediate frequency in the range of 400 MHz to 500 MHz. The device provides a differential output that passes through a SAW filter before connecting to a second down converter. For the best performance, Texas Instruments TRF1212 should be used to perform both the second down conversion and also provide the local oscillator for the TRF1216.

The TRF1216 includes a LNA with switchable attenuation, a balanced mixer, a variable gain IF amplifier and a differential LO Buffer for improved performance. In order to provide exceptional image rejection and extra jammer immunity, the TRF1216 offers a signal path to an off-chip filter. Specifications are provided assuming an in-band 2-dB insertion loss filter. To maximize input dynamic range, a 10-dB switchable attenuator is provided in the RF path as well as 10 dB of analog IF gain control. After the image reject filter, an on-chip Balun converts the signal from single ended to differential in order to provide better noise immunity at the mixer.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

The detailed block diagram and the pin-out of the ASIC are shown in Figure 1 and Table 1.

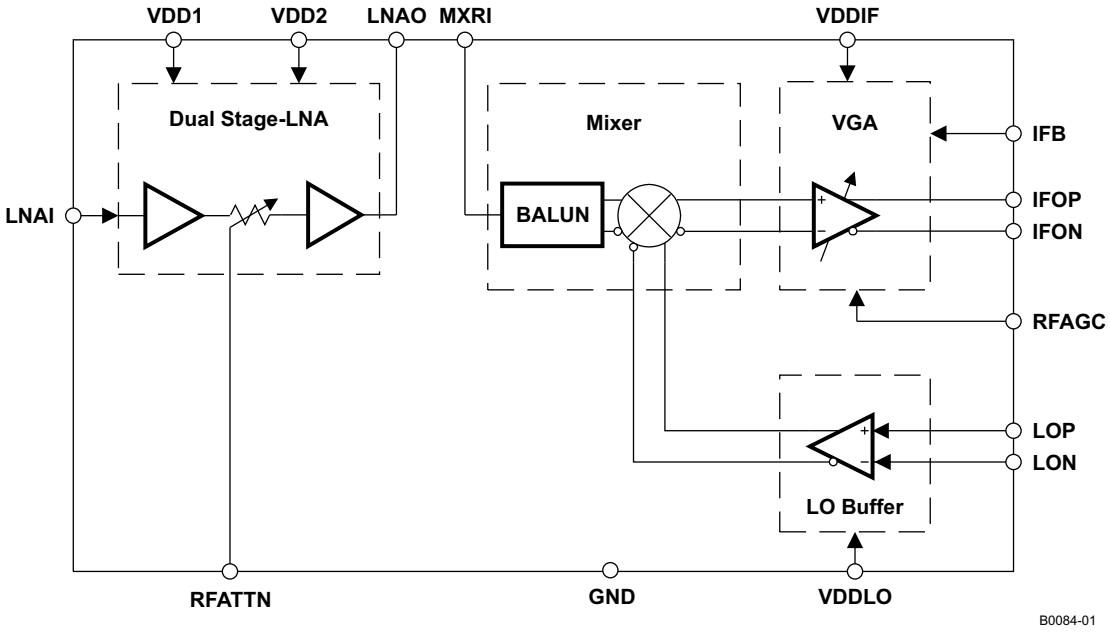


Figure 1. Detailed Block Diagram of TRF1216

TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	LNAO	O	Analog	LNA Output, 50 Ω, ac-coupled
2	VDD1	I	Power	LNA1 DC Bias (+5 V nominal)
3, 4, 6, 9, 16, 19	GND	–	–	Ground
5	LNAI	I	Analog	RF input – Needs dc block and input matching for optimum noise figure
7	LOP	I	Analog	LO input positive, ac coupled
8	LON	I	Analog	LO input negative, ac coupled
10	VDDLO	I	Power	LO DC Bias (+5 V nominal)
11	IFB	–	–	Not connected for normal operation. IF Bias Adjustment. Do not ground this pin or connect to any other pin.
12	VDDIF	I	Power	IF Bias Network dc Bias (+5 V nominal)
13	IFON	O	Analog	IF output and bias (see the application schematic for connections).
14	IFOP	O	Analog	IF output and bias (see the application schematic for connections).
15	RFAGC	I	Analog	Input voltage for analog gain control V_{RFAGC} = 0 V to 1.5 V Max gain at V_{RFAGC} = 0 V Min gain at V_{RFAGC} = 1.5 V
17	RFATTN	I	Digital	TTL control for switched attenuator TTL low – Attenuator switched in TTL high – Attenuator switched out
18	MXRI	I	Analog	Mixer Input 50 Ω
20	VDD2	–	Power	LNA2 dc bias (+5 V nominal)
Back	GND	–	–	Back of package has metal base that must be grounded for thermal and RF performance.

ABSOLUTE MAXIMUM RATINGS

		VALUES	UNIT
V_{DD}	DC supply voltage, VDD	0 to 5.5	V
P_{IN}	RF input power	10	dBm
T_J	Junction temperature	200	°C
P_D	Power dissipation	1100	mW
V_D	Digital input voltage	–0.3 to 5.5	V
V_A	Analog input voltage	–0.3 to 5	V
θ_{JC}	Thermal resistance junction-to-case(1)	9.1	°C/W
T_{stg}	Storage temperature	–40 to 105	°C
T_{op}	Operating temperature	–40 to 85	°C
	Lead temperature (40 Sec Max)	260	°C

(1) Thermal resistance is junction to ambient assuming thermal pad with nine thermal vias under package metal base. See the recommended PCB layout.

ELECTRICAL CHARACTERISTICS

The characteristics listed in the following tables are at V_{CC} = 5 V, T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{DD}	Supply voltage			5	5.5	V
I_{DD}	Total supply current			175	200	mA
I_{LNA1}	LNA1 supply current	Pin 2 (VDD1)		35		mA
I_{LNA2}	LNA2 supply current	Pin 20 (VDD2)		35		mA
I_{IF}	IF AMP supply current	Pin 12 (VDDIF) plus IF drain bias on pins 13 and 14 (IFOP, IFON)		55		mA
I_{LO}	LO supply current	Pin 10 (VDDLO)		50		mA
V_{AGC}	Gain control voltage		0		2	V
I_{AGC}	Gain control current		0		100	µA
V_{IH}	Input high voltage		2.5		5	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current				300	µA
I_{IL}	Input low current				–50	µA

DOWNCONVERTER CHARACTERISTICS

Unless otherwise stated V_{DD} = 5 V, FRF = 3500 MHz, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{RF}	RF input frequency		3300		3800	MHz
F_{LO}	LO input frequency		2800		3400	MHz
F_{IF}	IF output frequency		400	480	500	MHz
G	Maximum gain	V_{AGC} = 0 V, RFATTN disabled, Measured into 100-Ω differential load	27	30	33	dB
Δ_{AGC}	Analog gain control range	V_{AGC} from 0 to 1.5 V, Any RFATTN setting. Measured into 100-Ω differential load	7	10		dB
Δ_{ATTN}	Switched attenuator range	RFATTN from high-to-low, any VAGC setting. Measured into 100-Ω differential load	8.5	10	11.5	dB
G_{HG}	Gain flatness full band	Any 200-MHz band		1	2	dB
G_{NB}	Gain flatness / 6 MHz	Any 6-MHz band			0.4	dB
NF	Noise figure(1)	V_{AGC} = 0 V, RFATTN disabled		2.5		dB
		V_{AGC} = 0 V, RFATTN enabled		4.8		
		V_{AGC} = 1.5 V, RFATTN disabled		3.2		
		V_{AGC} = 1.5 V, RFATTN enabled		6.8		
IP-1dB	Input power at 1-dB compression	V_{AGC} = 0 V, RFATTN disabled		–17		dBm
		V_{AGC} = 0 V, RFATTN enabled		–6		
		V_{AGC} = 1.5 V, RFATTN disabled		–10		
		V_{AGC} = 1.5 V, RFATTN enabled		–4		
IIP3	Input 3rd order intercept point	V_{AGC} = 0 V, RFATTN disabled		–7		dBm
		V_{AGC} = 0 V, RFATTN enabled		-1		
		V_{AGC} = 1.5 V, RFATTN disabled		–5		
		V_{AGC} = 1.5 V, RFATTN enabled		5		
P_{LO}	LO input power	Referenced to 100-Ω differential		0		dBm
	LO to MXRI leakage	LO input = 3 dBm, V_{AGC} = 0 V	–35	–45		dB
	LO to IF leakage	LO input = 3 dBm, V_{AGC} = 0 V	–40	–50		dB
	LNAO to RXI isolation	F_{RF} F = 3300 to 3800 MHz, RFATTN = TTL High	40			dB

(1) Assured by lab characterization/design and not subject to production test.

TYPICAL CHARACTERISTICS

Measurements resulting in the following graphs were taken on the evaluation board of the ASIC (see Figure 9).

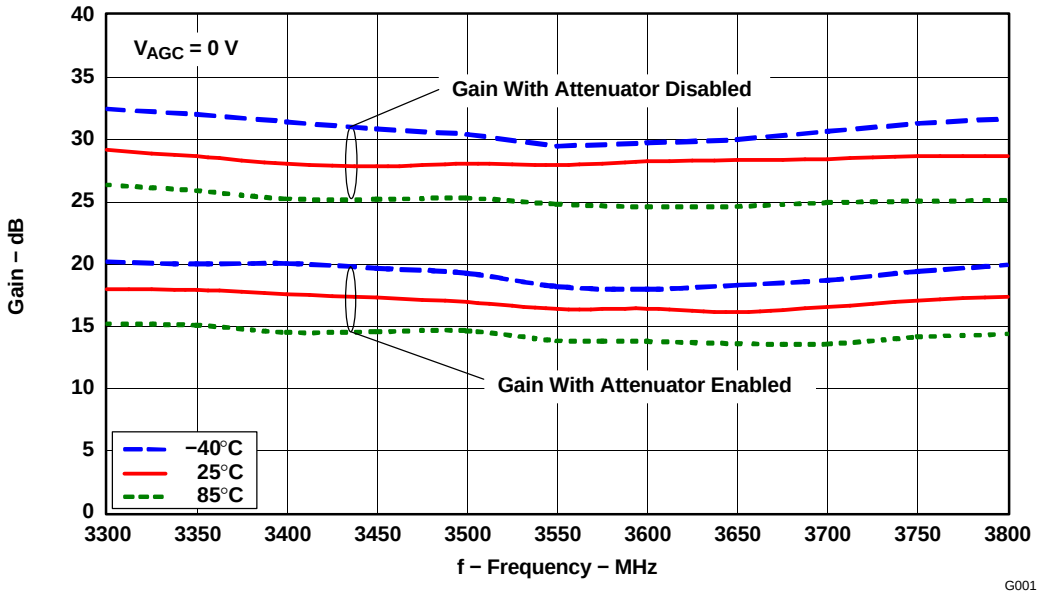


Figure 2. Gain vs Frequency for VAGC = 0 V

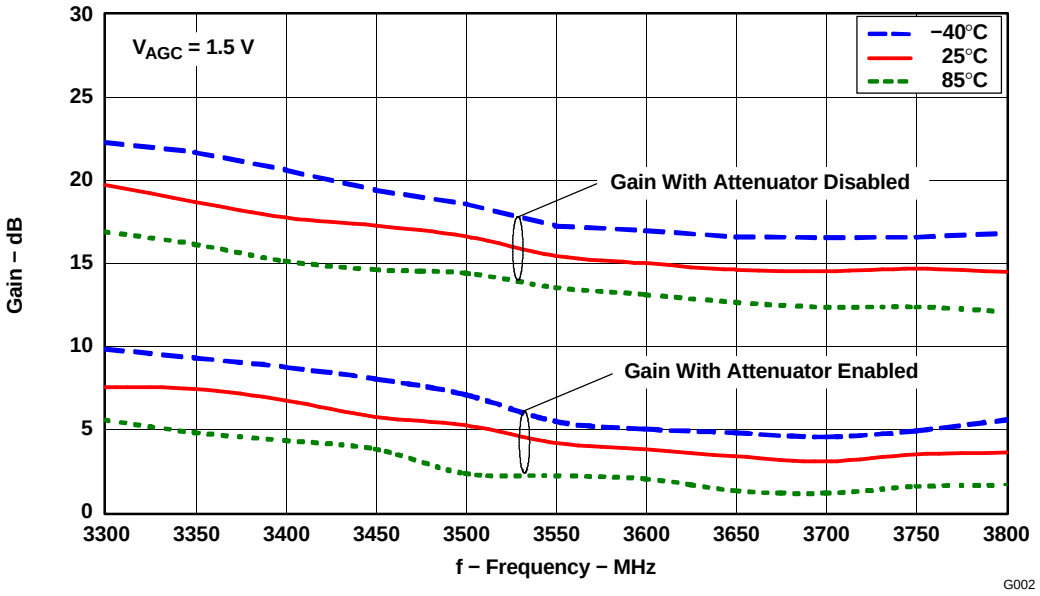


Figure 3. Gain vs Frequency for VAGC = 1.5 V

TYPICAL CHARACTERISTICS (continued)

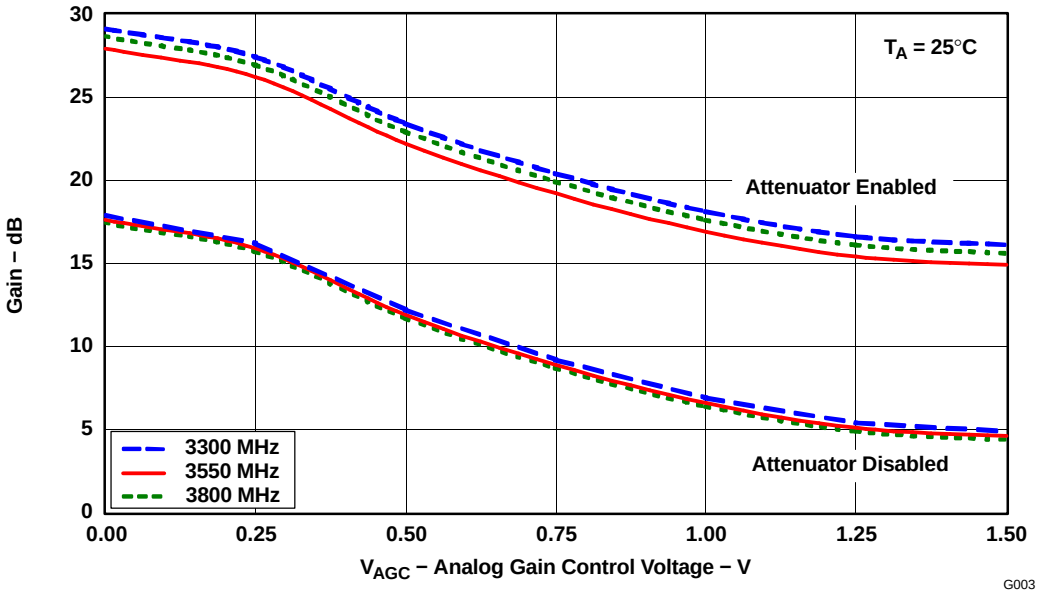


Figure 4. Gain vs VAGC for Different Frequencies, (T_A = 25°C)

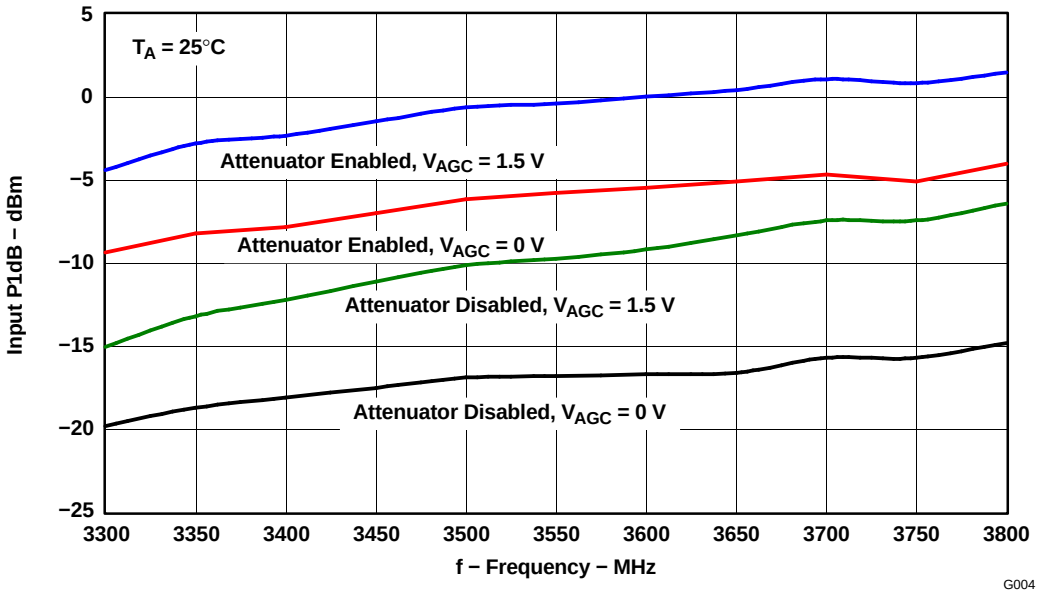


Figure 5. Input P1dB vs Frequency, (T_A = 25°C)

TYPICAL CHARACTERISTICS (continued)

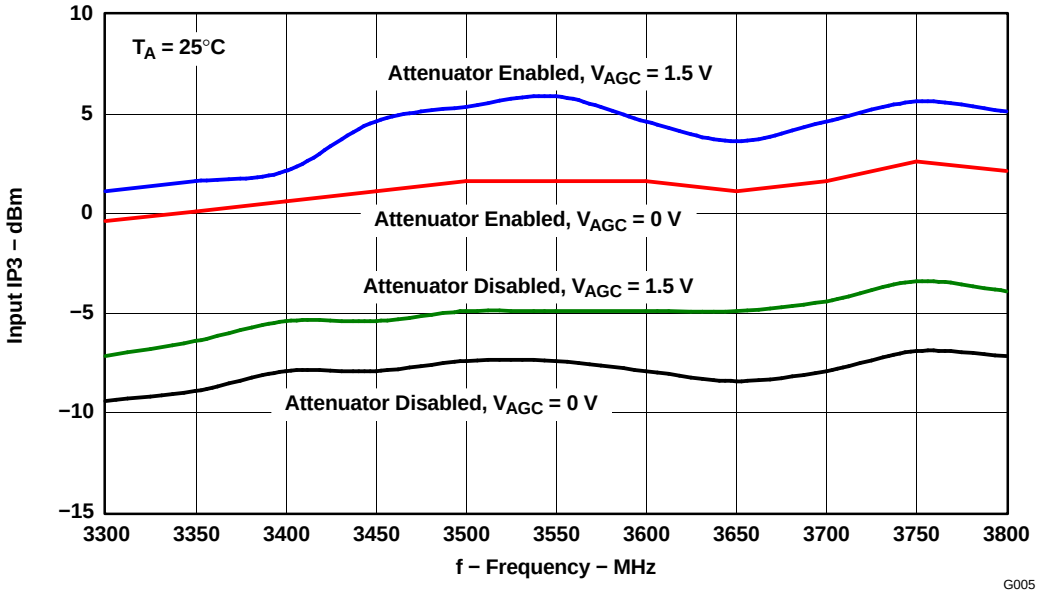


Figure 6. Input IP3 vs Frequency, (T_A = 25°C)

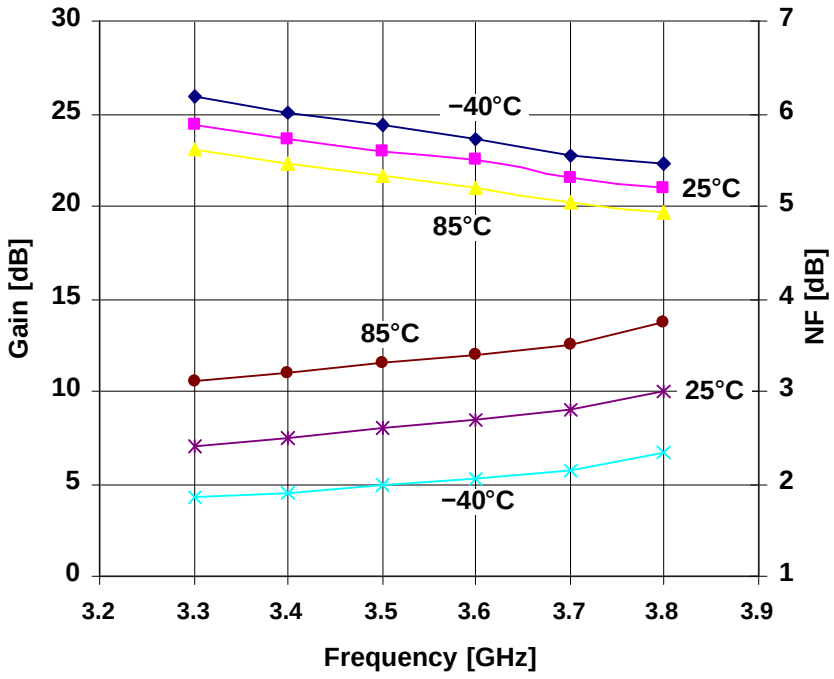


Figure 7. LNA Noise Figure vs Frequency With VAGC = 0 V

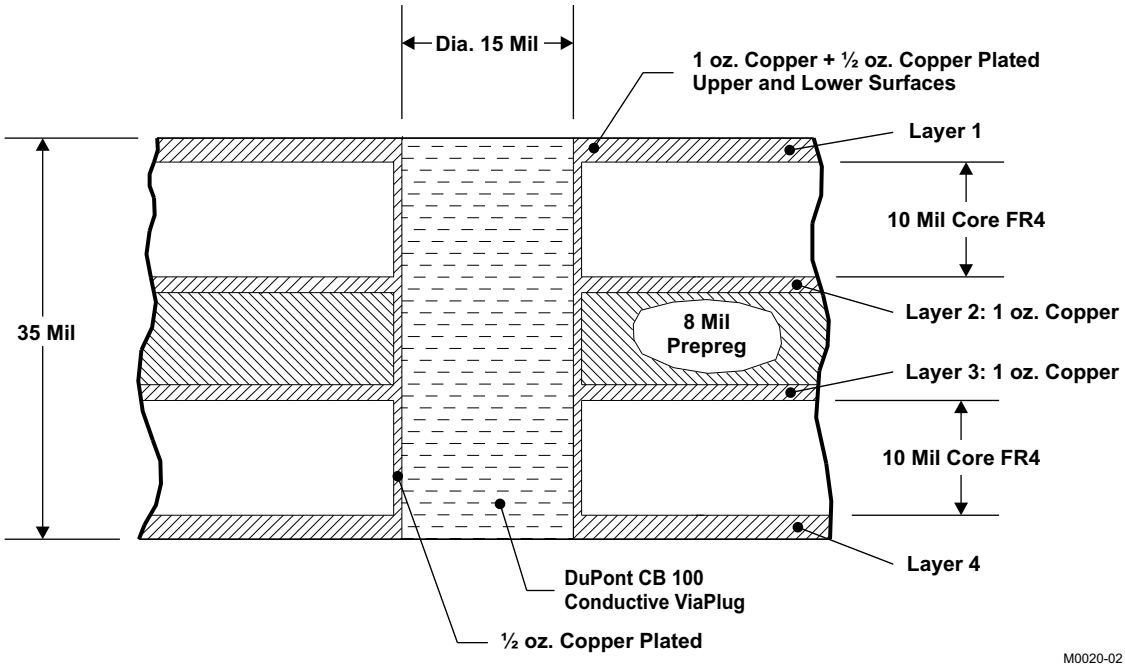
APPLICATION INFORMATION

A typical application schematic is shown in Figure 9.

The PCB material recommendations are shown in Table 1 and Figure 8.

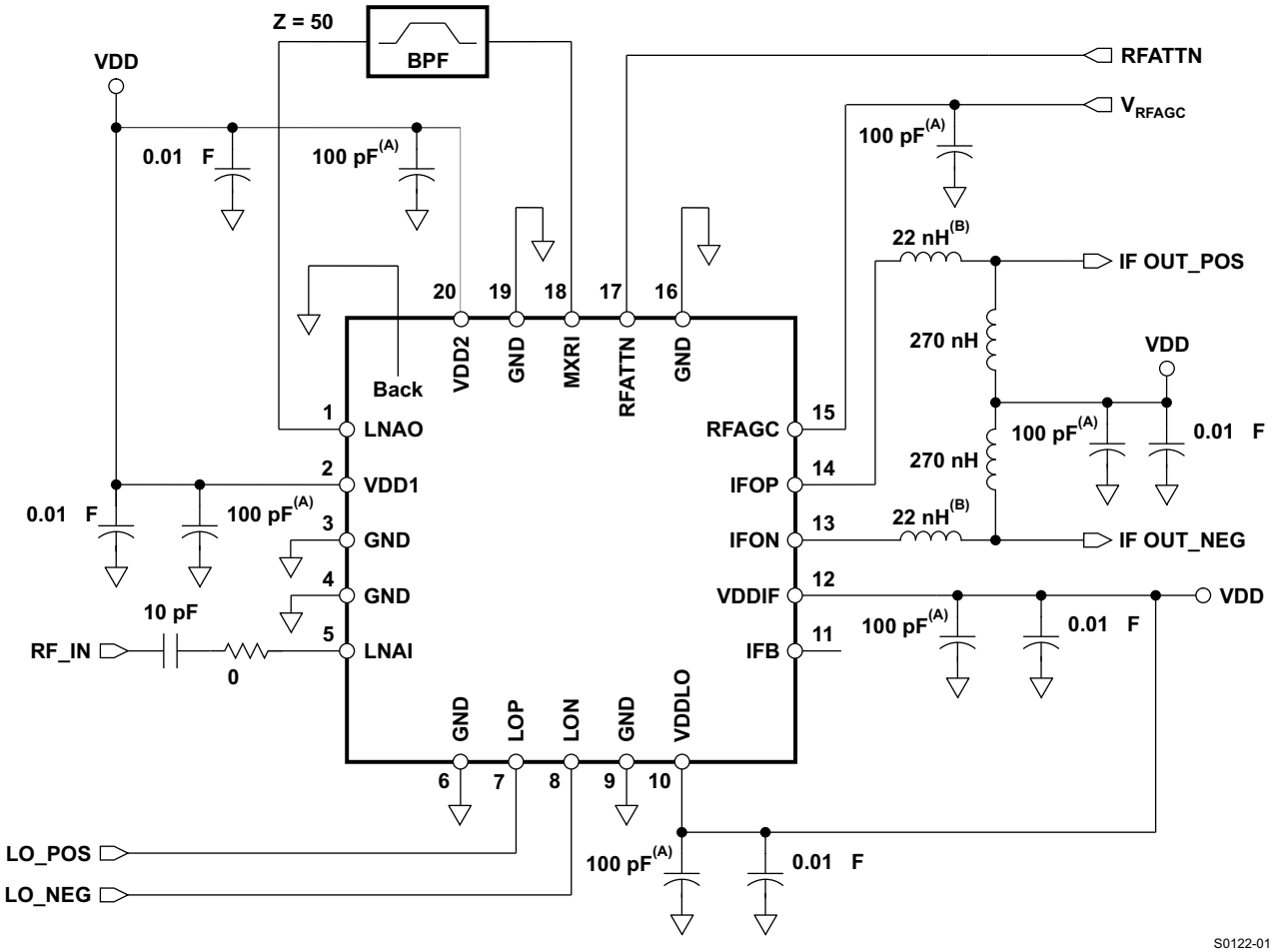
Table 1. PCB Recommendations

Board Material	FR4
Board Material Core Thickness	10 mil
Copper Thickness (starting)	1 oz
Prepreg Thickness	8 mil
Recommended Number of Layers	4
Via Plating Thickness	1/2 oz
Final Plate	White immersion tin
Final Board Thickness	33–37 mil



NOTE: Top and bottom surface finish: copper flash with 50–70 µin white tin immersion.

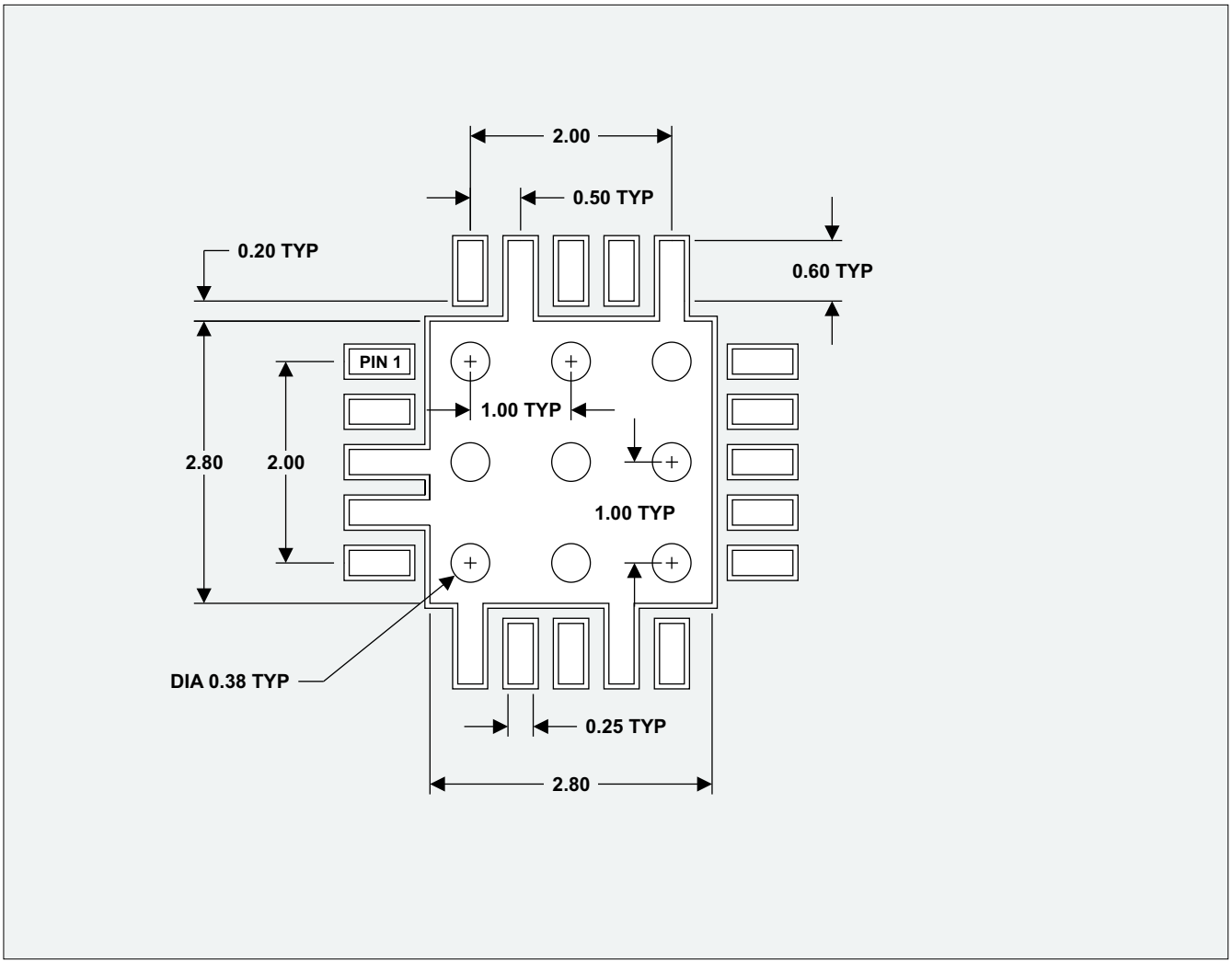
Figure 8. PCB Construction and Via Cross Section



A. Place 100-pF capacitors close to package pins.

B. Place 22-nH inductors close to package pins.

Figure 9. Recommended Application Schematic



Solder Mask. No Solder Mask Under Chip, On Lead Pads or On Ground Connections.

Notes: 9 Via Holes, Each 0.38 mm.
Dimensions in mm

M0022-02

Figure 10. Recommended Pad Layout

PACKAGING INFORMATION

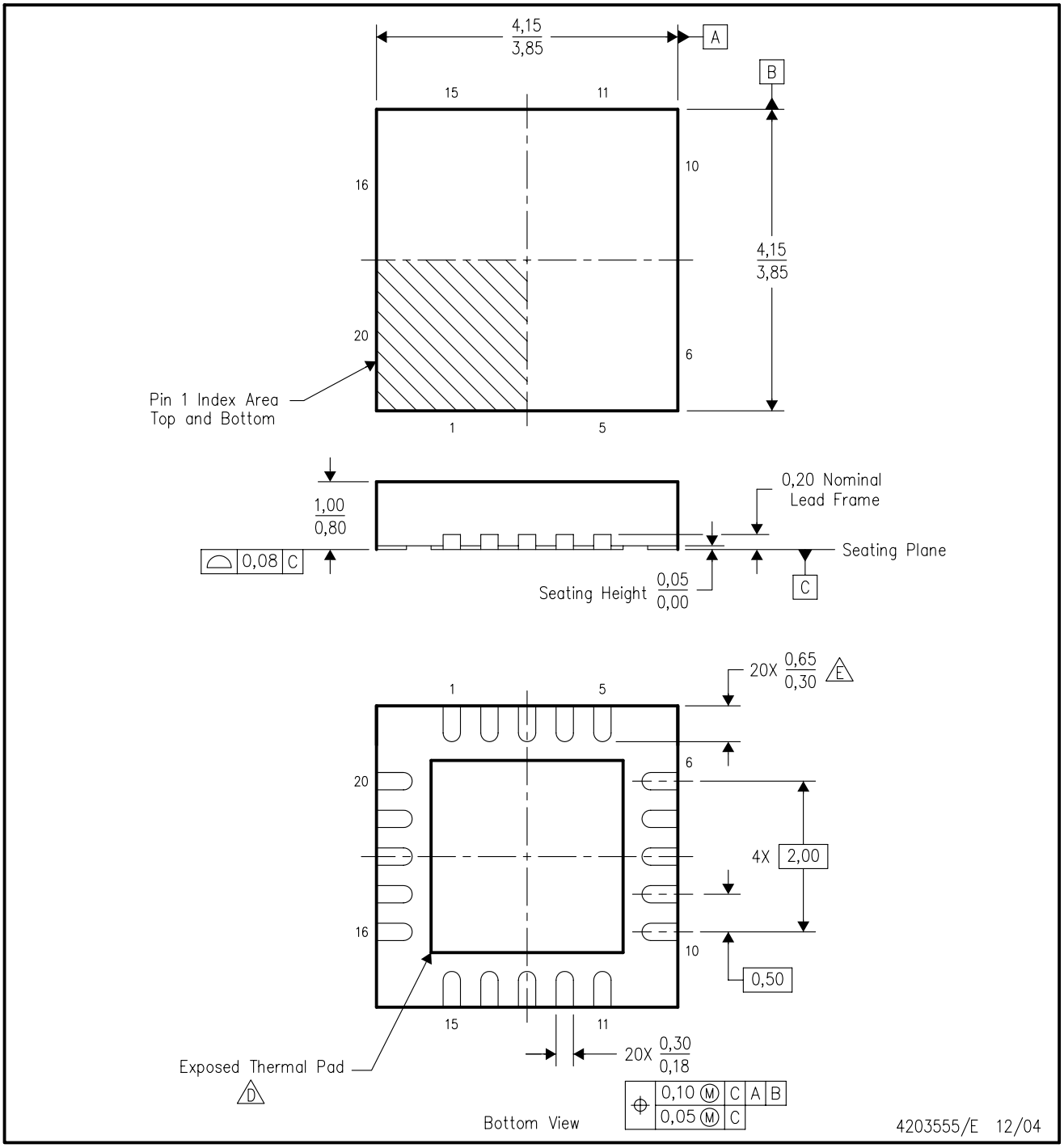
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TRF1216IRGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
TRF1216IRGPRG3	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
TRF1216IRGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
TRF1216IRGPTG3	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGP (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

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