TriTech Microelectronics

TR89101CS

Caller ID Receiver + DTMF

Features

- Single 5V power supply
- Demodulates both V.23 and Bell 202 modes
- Compatible with US Bellcore specification TR-NWT-00030 & SR-TSV-002476 and UK BT SIN 227, SIN 242 and CTA TW/P&E/312
- Built in DTMF transmitter (with single tone option) and call progress detect, for dial back
- High input sensitivity -48dBm
- TTL frequency output for "idle state alert tone" and call progress signals
- Separate power down controls FSK, DTMF, Call Progress
- Low power CMOS
- 28-pin SOIC package

General Description

The TriTech TR89101 Caller ID+ is an integrated Caller ID receiver designed to operate in countries using either the Bellcore system or the British Telecom system for Caller Display Services.

The TR89101 includes receivers for both the US Bellcore specification TR-NWT-00030 & SR-TSV-002476 and the UK SIN 227, SIN 242 and CTA TW/P&E/312 requirements. This device is designed to offer superior flexibility and features over present CID devices. The circuit also includes an industry standard DTMF transmitter for redialing and a Call Progress detector for further system cost savings.

BLOCK DIAGRAM

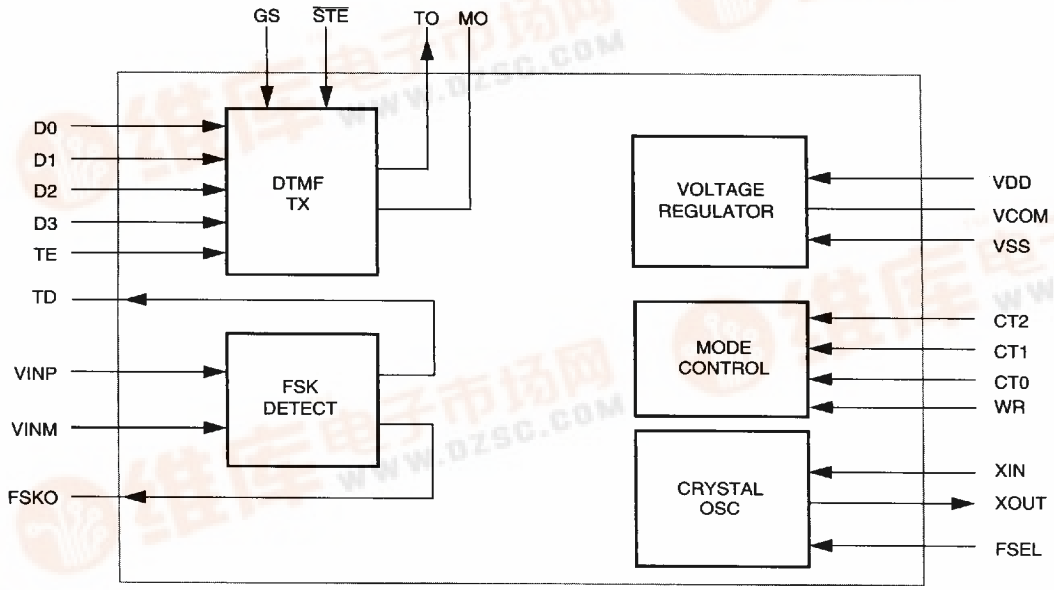
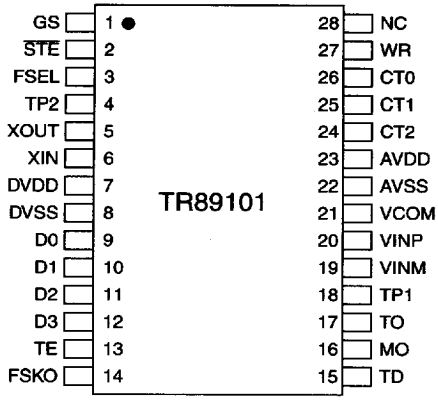


Figure 1 • *Caller ID+*

Pin Configuration



28 - PIN SOP TOP VIEW

Pin Descriptions

Pin No	Pin Name	I/O	Description
1	GS	I	Used to select the high group or low group DTMF frequency when the device is in single tone mode. When pulled to logic 1, the high group frequency will be generated. When pulled to Logic 0, the low group frequency will be generated.
2	$\overline{\text{STE}}$	I	When pulled to Logic 0, only a single DTMF tone is generated. For normal operation tie to Logic 1.
3	FSEL	I	Selects XTAL frequency. 4MHz (High) or 3.58MHz (Low)
4	TP2	-	Factory Test Pin. Do not connect.
5	XOUT	O	Crystal oscillator output pin.
6	XIN	I	Crystal oscillator input pin.
7	DVDD	-	Digital VDD
8	DVSS	-	Digital Ground
9	D0	I	Data for the DTMF generator D0 is the LSB.
10	D1	I	Data is latched on the rising edge of TE.
11	D2	I	
1 2	D3	I	
13	TE	I	Tone enable. When logic low, the tone generation is inhibited. On the low to high transition, the data on the D0...D3 inputs is latched.
14	FSKO	O	FSK demodulator output. Delivers digital data during FSK demodulation. Logic low when inactive. Clipped version of the filtered input signal when in Call Progress Tone Extraction and Alert Tone modes and the signal is in a certain frequency window.
15	TD	O	Tone Detect Output. Logic high when signal amplitude is within limits.
16	MO	O	Mute output. Open drain NMOS output. Sinks current to VSS when TE is high. Requires 100KΩ pull up resistor typically.

Pin Descriptions (continued)

Pin No	Pin Name	I/O	Description
17	TO	O	Analog tone output.
18	TP1	-	Factory test pin. Do not connect.
19	VINM	I	Inverting input of the differential input buffer. Internally biased.
20	VINP	I	Non-inverting input of the differential input buffer. Internally biased.
21	VCOM	-	External bypass for the internal common-mode voltage.
22	AVSS	-	Analog VSS
23	AVDD	-	Analaog VDD
24	CT2	I	Mode selection (see Table 1).
25	CT1	I	
26	CT0	I	
27	WR	I	Write signal for control data latch, Latches CT0-CT2 on rising edge.
28	VSS	-	Ground

Circuit Description

The Caller ID feature is an on-hook capability which provides the user with information about the caller before actually answering the call. The information is transmitted as 1200 bps FSK data during the silent interval between the first two ringing bursts (US standard, and UK CTA scheme) or prior the first burst, but after a line reversal (UK BT scheme).

FSK detector

The FSK detector's main function is to demodulate the incoming 1200 bps FSK signal which carries the CID data and generate a serial TTL data output (FSKO). The detector complies to the two different FSK standards used namely Bell 202 for the US and ITU-T recommendation V.23 in the UK. The detector has internally biased differential inputs (VINP, VINM) and the gain is set to accommodate low-level signals down to -48dBm. The input signal is processed by a filter whose characteristic is dependent on the function in progress. The status of the CT2..CT0 pins determine the behaviour of the circuit (see Table 1). When operating in the CID mode the filtered signal is applied to the FSK demodulator. The demodulated data stream can then be processed by a microcontroller.

Tone detectors

When the FSK function is inactive for CID, a Call Progress Tone Extraction (CPTE) function can be activated. The incoming signal is filtered and, in case the level is between certain limits, a clipped version is delivered to the microcontroller. This tone detection function can also be activated to detect the Idle State Alert Tone as described in BT document SIN 227 issue 1, as 2130 ± 20 Hz. The filtered tone is delivered to the microcontroller for measurement. In the CPTE mode the circuit will recognize a signal with a frequency between 225 Hz and 750 Hz with a power level between -38 dBm and 0 dBm. A logic 1 is flagged on pin TD when a valid Alert Tone or Call Progress Tone is detected to be within respective prescribed level limits.

WR Signal

The TR89101 contains a transparent latch for the CT2..CT0 signals. With WR=0 the latch is in the transparent mode. Data will be latched on the low to high transition of the WR signal.

Crystal Selection

The device uses a crystal oscillator connected to the pins XIN and XIN, that may be one of two set frequencies. Selection of the frequency to be used is controlled by the FSEL pin according to Table 2.

Table 2. *Crystal Selection*

FSEL	Crystal Frequency
0	3.58 MHz
1	4.0 MHz

Table 1. *Mode Selection Settings*

CT2	CT1	CT0	Mode Selection
0	0	0	Call Progress Tone Extraction RX filter scaled to to detect call prgress. Clipped frequency output on FSKO
0	0	1	Caller ID (FSK) detect. Demodulated data on FSKO
0	1	0	DTMF Generator on
0	1	1	Test Mode
1	0	0	Tone Alert Signal Detection. RX filter scaled to detect 2130Hz signal. Clipped waveform on FSKO.
1	0	1	Caller ID (FSK) detect. Demodulated data on FSKO
1	1	0	DTMF generator on
1	1	1	General Power Down.

The DTMF Transmitter

The DTMF transmitter is a tone dialer. It generates eight different sinusoidal audio frequencies which are mixed to provide the 16 tones suitable for Dual-Tone-Multi-Frequency dialing. This block generates high precision DTMF signals at the Tone Output (TO) corresponding to the codes sent by the microcontroller through the 4 data lines (D0...D3). The data bits are latched by the rising edge of the Tone Enable (TE) signal. When TE is high, the open-drain Mute Output (MO) pulls to Ground (VSS) and no tone is generated. This function can be used to mute other devices while dialing. A 100KΩ pull up reistor should be connected to the MO pin for normal operation.

The TO pin is the output of an analog buffer, so there is no swift transition from no-tone to generation. The output is intended to drive an external transistor to modulate the line current rather than driving the line directly. The output impedance of the TO pin is 20kΩ. The low distortion tones are derived from a high stability, crystal-controlled frequency reference.

Table 3. DTMF Selection Table

D0	D1	D2	D3	TE	MO	TO		
LSB			MSB			Low Group Hz	High Group Hz	Digit
X	X	X	X	L	Z	Z	Z	X
X	X	X	X	H	L	Z	Z	X
1	0	0	0	H	L	697	1209	1
0	1	0	0	H	L	697	1336	2
1	1	0	0	H	L	697	1477	3
0	0	1	0	H	L	770	1209	4
1	0	1	0	H	L	770	1336	5
0	1	1	0	H	L	770	1477	6
1	1	1	0	H	L	852	1209	7
0	0	0	1	H	L	852	1336	8
1	0	0	1	H	L	852	1477	9
0	1	0	1	H	L	941	1336	0
1	1	0	1	H	L	941	1209	*
0	0	1	1	H	L	941	1477	#
1	0	1	1	H	L	697	1633	A
0	1	1	1	H	L	770	1633	B
1	1	1	1	H	L	852	1633	C
0	0	0	0	H	L	941	1633	D

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V	AVDD, DVDD Supply Voltage	-0.5	5.5	V
Vi	Input Voltage	-0.3	5.8	V
Vo	Output Voltage	-0.3	5.8	V
Ts	Storage Temperature	-40	125	°C

Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
AVDD	Supply Voltage	4.75	5.0	5.25	V
DVDD	Supply Voltage	4.75	5.0	5.25	V
Ta	Ambient Temperature	0		70	°C
Fxtal	Crystal frequency FSEL=0 FSEL=1		3.58 4.0		MHz

General Specifications

DC Characteristics (AVDD=VDD=5V, Ta=25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
IDD1	Supply Current	FSK on		4.8		mA
IDD2	Supply Current	DTMF on		4.1		mA
IDD3	Supply Current	Alert Tone Detect		4.8		mA
IDD4	Supply Current	Call Progress		4.8		mA
IDDPD	Supply Current	CT2..CT0 = 111		60		µA
Iil	Input Leakage Current		-10		10	µA
Vil	Low Level Input Voltage				0.8	V
Vih	High Level Input Voltage		2.0			V
Vol	Low Level Output Voltage	Iloll<4mA			0.4	V
Voh	High Level Output Voltage	Iloll<20µA	2.4			V

AC Characteristics

FSK Detection (1 dBm= 1mW into a load of 600Ω)

Parameter	Conditions	Min	Typ	Max	Units
Input Sensitivity for FSK Reception		-48		-12	dBm
Logical 1 at FSKO	Bell V.23	1188 1280.5	1200 1300	1212 1319.5	Hz
Logical 0 at FSKO	Bell V.23	2188 2068.5	2200 2100	2222 2131.5	Hz
Tone detect turn on time	From Power Down		7		mS

Call Progress Tone Extraction

Parameter	Conditions	Min	Typ	Max	Units
Signal Extraction Level	225Hz < f < 750Hz	-38		0	dBm
Signal Rejection Level	225Hz < f < 750Hz			-50	dBm

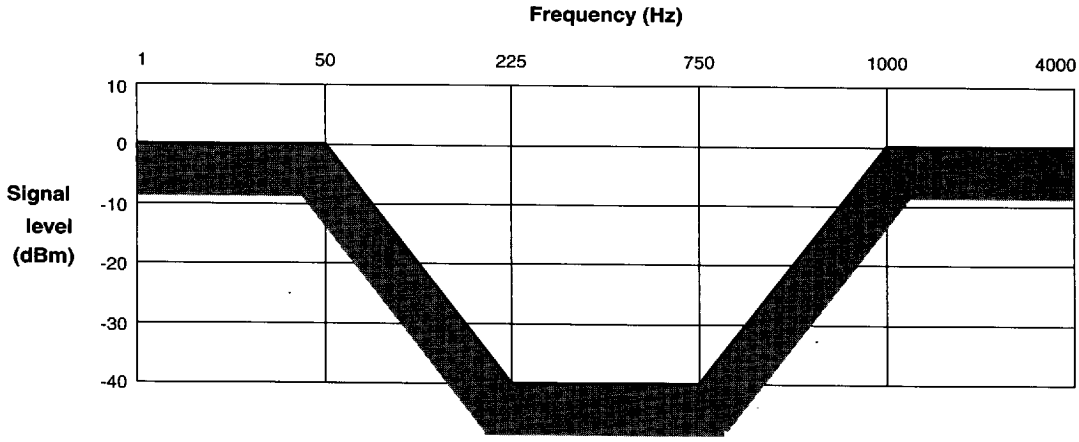


***Figure 2** • CPTE Detection Range*

Idle State Alert Tone Detection (1dBV=1V)

Parameter	Conditions	Min	Typ	Max	Units
Sensitivity	Signal = 2130 ± 20Hz	-40		-2.2	dBV

Tone Detect (TD) Timing

Symbol	Parameter	Min	Typ	Max	Unit
td_1	Delay Time			6	mS
td_2	Delay Time			6	mS

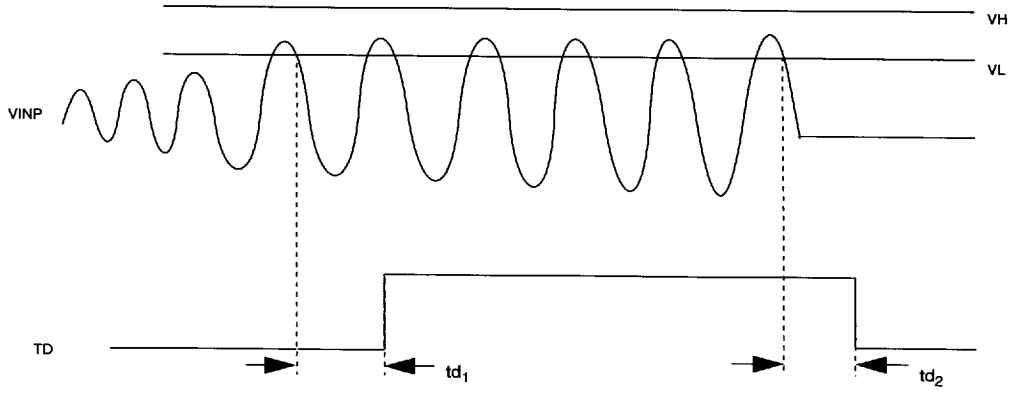


***Figure 3** • Tone Detect (TD pin) Timing Diagram*

Control Timing

Symbol	Parameter	Min.	Max.	Unit
tw	Write Pulse Width	40		nS
tsu	Data Setup Time	20		nS
th	Data Hold Time	20		nS

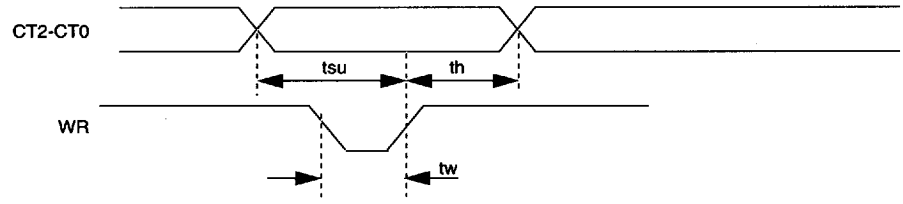


***Figure 4** • Control Timing Diagram*

DTMF Timing

Symbol	Parameter	Min.	Max.	Unit
tstart	Start-up Time	40		µS
tsu	Data Setup Time		20	nS
thd	Data Hold Time		20	nS

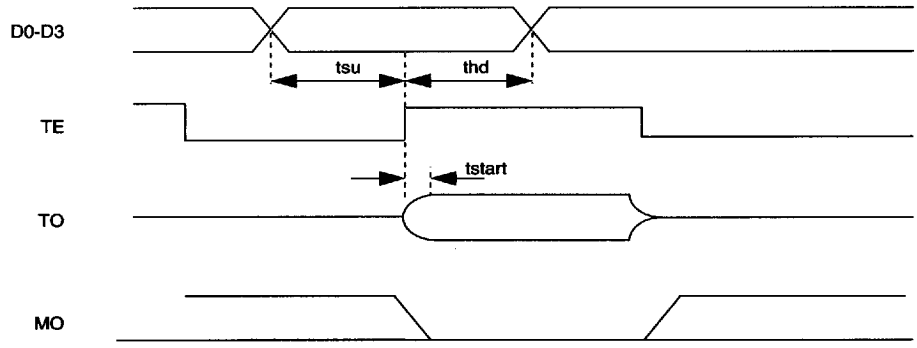


***Figure 5** • DTMF Block Timing Diagram*

DTMF Frequency Tolerance

Table 3a. DTMF Output Frequency Accuracy 4.0MHz

Standard DTMF (Hz)	TO Frequency (Hz)	% deviation
Low Group		
697	698.32	0.19
770	771.60	0.21
852	850.34	-0.19
941	939.85	-0.12
High Group		
1209	1213.59	0.38
1336	1329.79	-0.47
1477	1470.59	-0.43
1633	1644.74	0.72

Table 3b. DTMF Output Frequency Accuracy 3.58MHz

Standard DTMF (Hz)	TO Frequency (Hz)	% deviation
Low Group		
697	699.13	0.30
770	771.45	0.19
852	853.90	0.22
941	940.00	-0.11
High Group		
1209	1202.80	-0.52
1336	1339.65	-0.32
1477	1471.85	-0.35
1633	1633.00	0.00

DTMF Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VHout	High Group Output Level	Rl=10KΩ		1.25		Vp-p
VLout	Low Group Output Level	Rl=10KΩ		1.00		Vp-p
dBp	Pre-emphasis	Rl=10KΩ		2		dB
Rl	Output Load Impedance		10		50	kΩ
Rmo	External pull-up for MO			100		kΩ

Applications Information

The application of the device in a CID system can be explained with reference to the flow charts provided later in this section. However the user is also advised to consult the relevant local specifications for CID. Fig.6 shows a typical connection for TR89101.

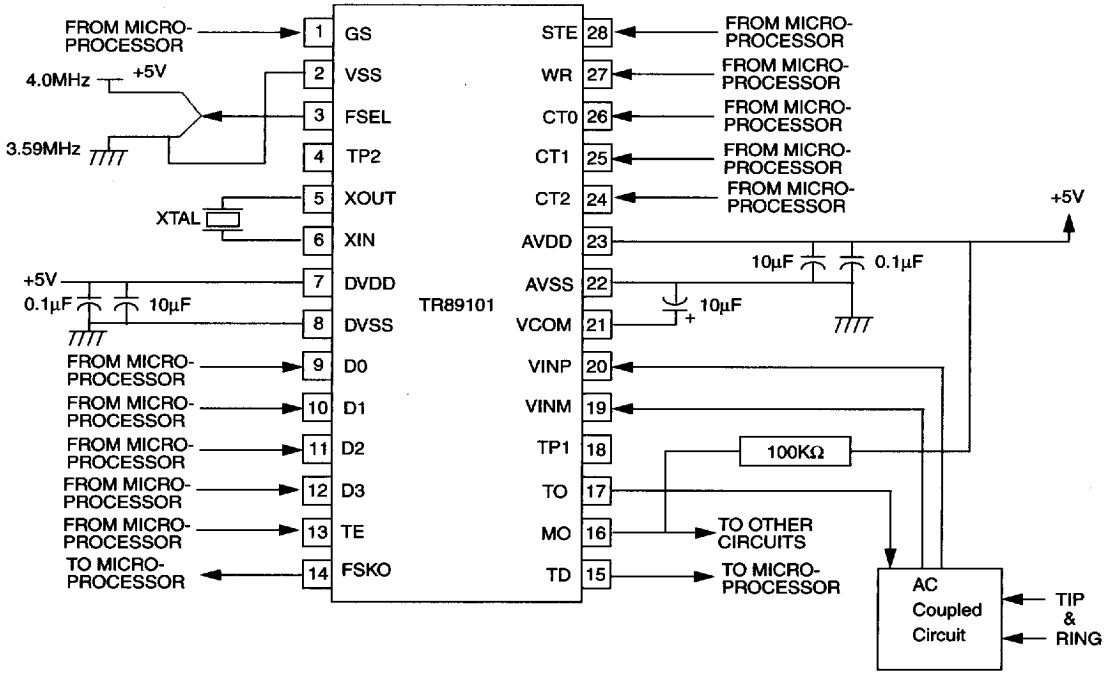


***Figure 6** • Typical Connection Diagram*

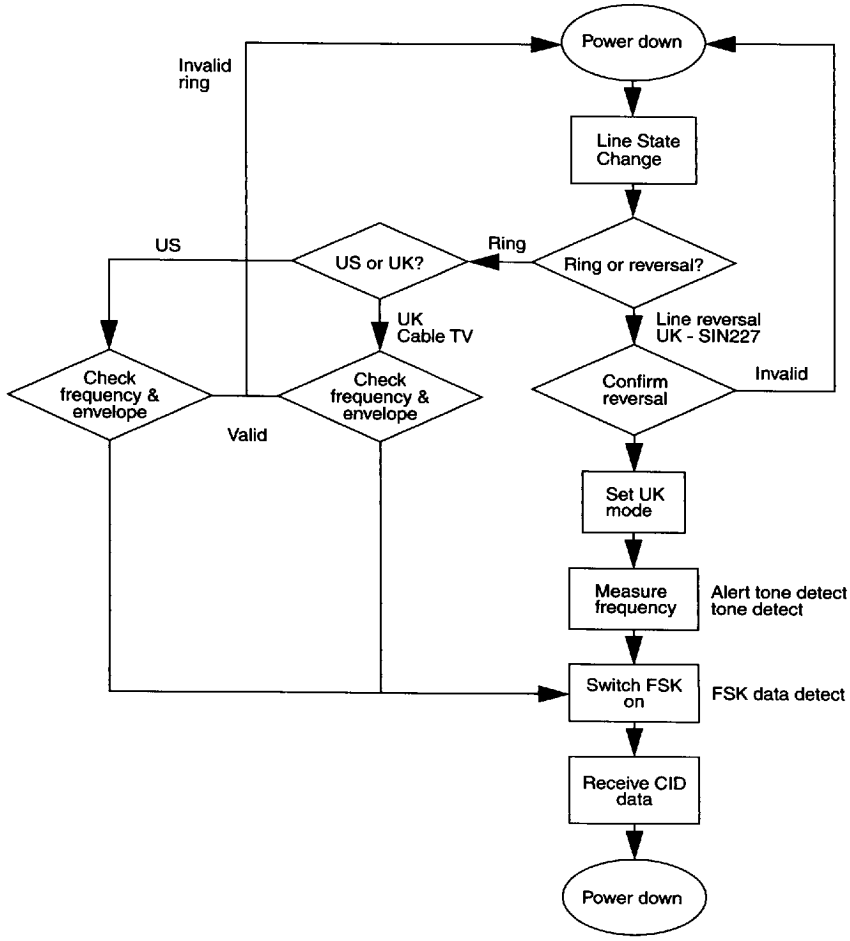
Caller ID Development Kit

Contact TriTech for details of evaluation boards and firmware for Caller ID and Computer Telephony applications

1. Typical Caller ID reception

Assume the initial condition that the device is powered down with the CT2..CT0 pins set to logic 1, as these settings will consume the minimum power. (See Flow Chart 1)

When the PSTN line changes state the first actions are carried out by the microcontroller to determine if the ring (or line reversal) is valid. In the US, ring frequency is between 16-68 Hz (typically 20Hz) with an envelope of two seconds on, four seconds off. The FSK data sent within the four second off period. In the UK, the CTA scheme will provide one burst of ring between 200-450ms in length between 16-25Hz after which the FSK data will be sent. The British Telecom scheme as described in SIN 227 will provide a line reversal to initiate the CID sequence rather than a ring. It is possible for the microcontroller to determine which of these line signals were received and then follow the appropriate sequence for the intended system.



***Flow Chart 1** • CID Reception*

1.1 Bellcore system

Fig.7. shows the Bellcore (US Caller ID) timing diagram. In the Bellcore system the ring signal must be detected within 0.2 to 2.2 seconds. After the two second ring pulse the central office waits 0.5 seconds before starting to send the FSK data. After the ring is accepted as valid by the microcontroller it must turn on the FSK detector (CT0 set to logic 1; CT2, CT1 set to logic 0). This will set the TR89101 ready to receive the FSK data which will be demodulated and output on the FSKO pin in asynchronous format. After the complete message has been received the CT2..0 pins can be set logic 1 to power down the FSK detector.

The data format used is as follows:

All CID messages are preceded with a 250ms preamble (0101010 pattern). This is then followed by a 150ms long carrier signal (1200Hz). The fixed mark is then followed by the message type, 8 bit sequence. After that, a message length or data word count value of 9 through 18 specifies the number of data words that are going to be transmitted following this word. This number does not include the check sum word which follows the data word. The actual CID information is grouped as a series of 8-bit characters bounded by a start bit (logic 0) and a stop bit (logic 1). The data is sent as ASCII characters with no parity. The first eight words contain the date (month - day) and the time (hours - minutes, 24 hour format, two characters each). The ninth word carries the calling party information. This is a 2 - 10 digit number or an ASCII character "P" for privacy or "O" for out of area. The last byte is the checksum which consists of 2's complement of the modulo 256 sum of all the words transmitted, including the message type, message length and data words. The receiver should derive this sum and add it to the received checksum. Any result other than zero indicates that the information was not received correctly.

The alternative multiple message format contains additional information such as the caller's name. In this format each parameter is a series of data words specifying parameter type, parameter length, and parameter data. The check sum is still applied at the end of the complete message.

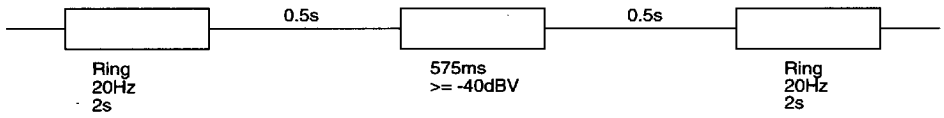


***Figure 7** • US Caller ID Scheme*

1.2 UK CTA system

Fig.8 shows the UK CTA Caller ID timing diagram. After the ring is accepted as valid by the microcontroller the receiver must apply a DC and an AC load for a specified time (>100ms) but this load may not be removed until after the FSK signals have been received. At the same time as the loads are applied, the microcontroller must turn on the FSK detector (CT0 set to logic 1; CT2, CT1 set to logic 0). This will set the TR89101 ready to receive the FSK data which will be demodulated and output on the FSKO pin in asynchronous format. After this load has been applied the central office will begin sending the FSK data.

All CID messages are preceded with an 80-262ms preamble (0101010 pattern at 1200bps). If this preamble is not detected within two seconds then the receiver should assume that this is a non-CID call.

This preamble is followed by a 45-150ms long carrier signal (1300Hz). This fixed mark is then followed by the message type byte. After that, a message length byte specifies the number of data words that is going to be transmitted following this parameter allowing for up to 255 bytes. This number does not include the message type, message length or check sum bytes which follows the data bytes. The actual CID information consists of 0-255 bytes according to the message length. Any 8-bit value may be sent in the message bytes depending on the requirements of the application. Given the large number of bytes they will not be described here, but the user is advised to read SIN 227 Annex A.

After the complete message has been received, the AC and DC loads must be removed and the CT2..0 pins can be set to logic 1 to consume minimum power.

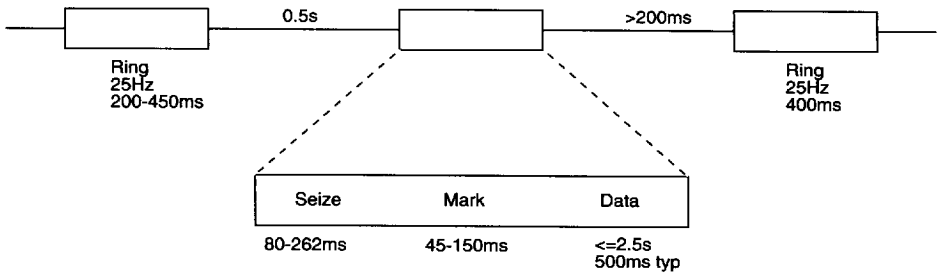


***Figure 8** • UK Cable TV Caller ID Scheme*

1.3 UK British Telecom system

Fig.9. shows the UK British Telecom Caller ID timing diagram. The British Telecom system sends the CID data before a ring signal arrives at the user equipment. The arrival of the CID is indicated by a line reversal which is intended to be detected and qualified by the microcontroller. After the line reversal has been detected there is a period of silence for 100ms. During the silence period the microcontroller should set the TR89101 into alert tone mode (CT2..0 pins set to 100) to enable the idle state alert tone detection circuitry and then monitor the FSKO pin and measure the frequency of the signal that appears on it. The microcontroller will be able to measure a frequency of the range 2130±20Hz. This frequency will be present for between 88-110ms and followed by another silent period of 45ms. In this time the microcontroller must apply a DC wetting pulse for 15±1ms to the line through a load of 240-350Ω within 20±5ms of the start of the silence. The wetting pulse will reduce to a steady state DC load of <0.5mA after its timed period. See figure 1, annex A of SIN 227. An AC load must also be applied at the same time as the wetting pulse and remain constant until the data has finished.

All CID messages are preceded with an 80-262ms preamble (0101010 pattern at 1200bps). If this preamble is not detected within two seconds then the receiver should assume that this is a non-CID call.

The preamble is followed by 45-150ms long carrier signal (1300Hz). The fixed mark is then followed by the message type byte. After that, a message length byte specifies the number of data words that are going to be transmitted following this parameter allowing for up to 255 bytes. This number does not include the message type, message length or check sum bytes which follows the data bytes. The actual CID information consists of 0-255 bytes according to the message length. Any 8-bit value may be sent in the message bytes depending on the requirements of the application. Given the large number of bytes they will not be described here, but the user is advised to read SIN 227 Annex A.

After the complete message has been received the AC and DC loads must be removed and the CT2..0 pins can be set logic 1 to consume minimum power.

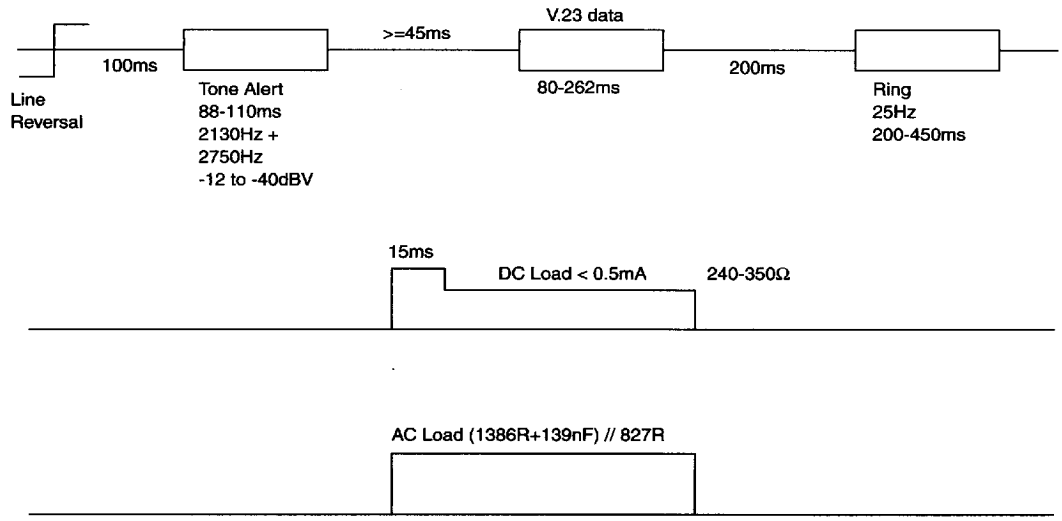
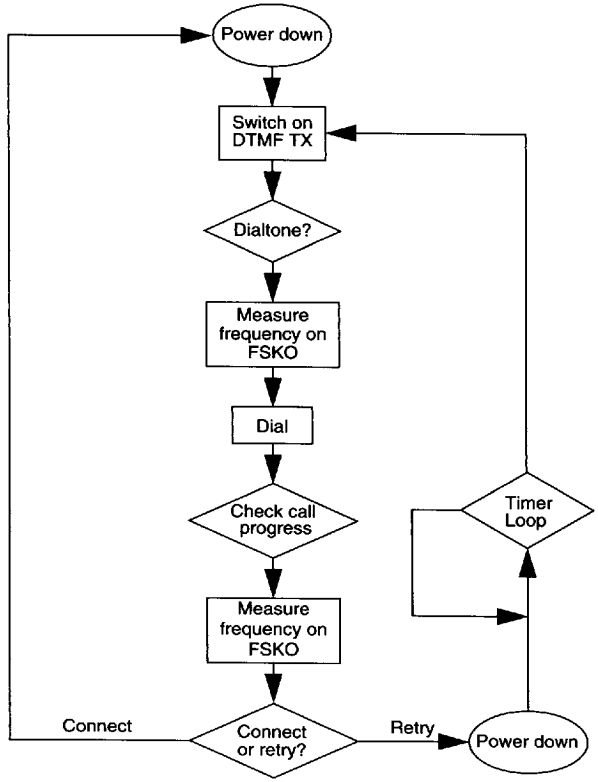


***Figure 9** • BT CID Scheme*

2. Dialing

The TriTech TR89101 contains a DTMF transmitter so that received CID numbers may be redialed by the user. While several PTTs have introduced services that allow redialing the last number that called you, this feature makes it possible to scroll through the stored numbers and choose which one to redial first. The quantity of stored numbers is up to the system designer to define.

To use the TR89101 for dialing refer to Flowchart 2. Firstly switch on the DTMF generator by setting CT2..CT0 to logic 0 and set the TE signal to logic 0. These settings will enable the call progress detection filter into the receive path. The microcontroller can assess which call progress tone has been received by measuring the frequency and duration of the signal on FSKO. In the first instance the presence of dialtone can be detected. If the required dialtone is active, the microcontroller can write the required digit to be dialed by loading the 4-bit latch and setting TE to logic 1 when the input data is stable. A timing diagram is shown in Fig. 5. While TE is high the mute output MO will be pulled to VSS allowing other devices to be muted while dialing takes place. It is a requirement of the microcontroller to time the duration of the DTMF signal as the TR89101 will continue to generate the programmed tone until TE goes low again. This sequence can then be repeated to dial subsequent digits. After dialing is complete the microcontroller can monitor the FSKO signal to detect if a busy signal is present requiring further re-dialing or if the call was successfully connected.



***Flow Chart 2** • DTMF Transmitter*

Mechanical Dimensions

28 Pin SOIC

Dimensions In Inches (mm)