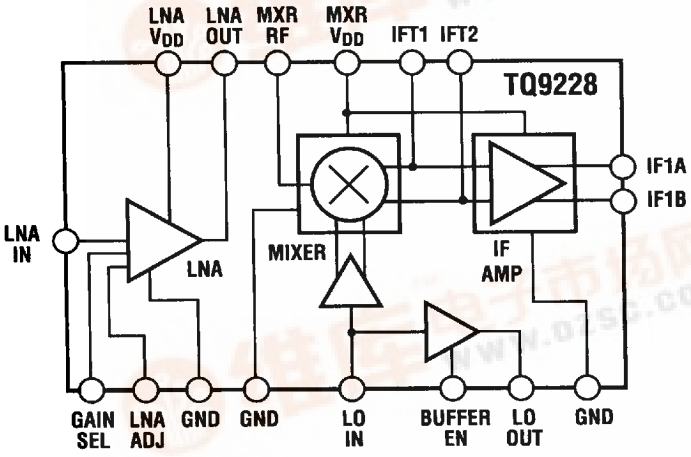


TQ9228

3-V PCS-Band CDMA Downconverter IC

ICs

The TQ9228 is a 3-V, RF receiver IC designed specifically for PCS-band CDMA applications. The performance meets the demanding requirements of IS-95/98 standards-based products; portable or fixed applications. The downconverter architecture maximizes the LNA dynamic range while maintaining excellent overall downconverter performance. The RF frequency range covers the entire PCS band. The high-side LO and 85 MHz IF are compatible with several chip-set frequencies. Enhanced $^1/_2$-IF spurious rejection permits the use of lower IFs. The wide supply voltage range of 2.7 V to 4.0 V permits the use of the part with a variety of battery voltages.

Features

- *Single 3-V operation*
- *Gain select*
- *LO buffer output*
- *Differential IF output*
- *QSOP-24 package*
- *Split LNA architecture*
- *High $^1/_2$ IF rejection*

Applications

- *IS-95/98 mobile phones*
- *Wireless local loop*
- *PCS micro-cells*

Electrical Specifications

Operating Conditions: V_{DD} = 3.0 V, T_A = 25°C, Filter IL = 3 dB, RF = 1930 to 1990 MHz, LO = 2015 to 2075 MHz, LO Level = -4 to +1 dBm, IF = 85 MHz, LNA Adj. = Open; unless otherwise specified

Parameter (1)	Conditions	Min.	Typ.	Max.	Units
Gain	High gain	23.0	26.5	30.0	dB
	Low gain		7		dB
Noise Figure	High gain		2.6	3.7	dB
	Low gain		16.0	17.5	dB
Input IP3	High gain	-12.5	-10.0		dBm
	Low gain	+6.5	+10.0		dBm
Supply Current (2)			51	64	mA

Notes: 1. Min/max values listed are production tested.
2. LO buffer off.

Electrical Specifications (V_{DD} = 3.0 V)

Operating Conditions: V_{DD} = 3.0 V, T_A = 25°C, RF = 1930 to 1990 MHz, LO = 2015 to 2075 MHz, LO Level = -4 to +1 dBm, IF = 85 MHz, LNA Adj. = Open, Filter IL = 3 dB; unless otherwise specified

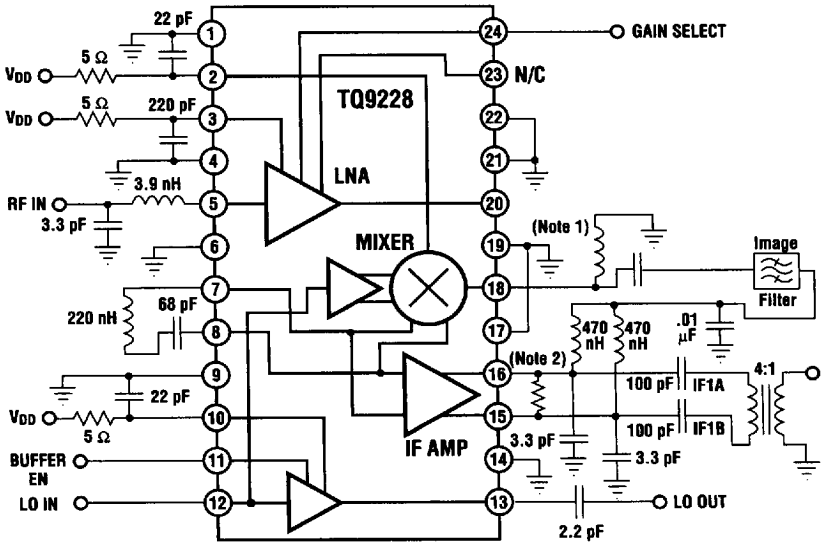
Parameter	Conditions	Min	Typ	Max	Units
Gain	High gain	23.0	26.5	30.0	dB
	Low gain	2.5	6.5	10.5	dB
Noise Figure	High gain		2.6	3.7	dB
	Low gain		16	17.5	dB
Input 3rd-Order Intercept	High gain T_A = 25°C	-12.5	-10.0		dBm
	Low gain	+6.5	+10.0		dBm
LNA Input IP3	LNA only, 50-ohm terminations	+3	+6		dBm
$^1/_2$-IF Suppression	P_{IN} to LNA input = -33 dBm	-50	-57		dBc
Return Loss	LNA In (with external match)	9.5	12		dB
	LNA Out	9.5	15.5		dB
	LNA Out (low-gain mode)	8.5	11.5		dB
	Mixer RF (with external match)	9.5	13		dB
	LO In	9.5	12		dB
	LO Out	8.5	10		dB
Isolation	LNA In to IFA/IFB	20			dB
	LNA In to LO In	20			dB
	LNA In to LO Out	10			dB
	LO In/Out to LNA In	20			dB
	LO In/Out to IFA/IFB	20			dB
	LO Out to LO In	20			dB
	LNA Out pin to Mixer RF pin	25			dB
Supply Current	LNA On, LO Buffer On		54	67	mA
	LNA On, LO Buffer Off		51	64	mA
	LNA Off, LO Buffer On		41	51	mA
	LNA Off, LO Buffer Off		38	48	mA

Parameter	Conditions	Min.	Typ.	Max.	Units
LO Output Power Level	LO Input = -4 dBm	-8.0	-5.5	0	dBm
Output Resistance	Differential mode	475	640	815	ohm
Output Capacitance	Differential mode		0.1	1	pF
LO Buffer Turn-on Time				100	µs
LO Buffer Turn-off Time				100	µs
Input Logic LOW Voltage		0		0.8	V
Input Logic HIGH Voltage		2.3		V_{DD}	V
Input Logic LOW Current				50	µA
Input Logic HIGH Current				200	µA

Note: 1. The value of the $^1/_2$-IF trap components affects the conversion gain and must be selected to optimize conversion gain and $^1/_2$-IF performance. An application circuit which resistively terminates the IF port may be required to center the gain window to achieve the above specification

Test Circuit

(All signal ports are matched to 50 Ω)



Notes: 1. Optional shunt inductance and series capacitance to improve the input matching.
2. Optional resistor to adjust gain.

Receiver Mode Control

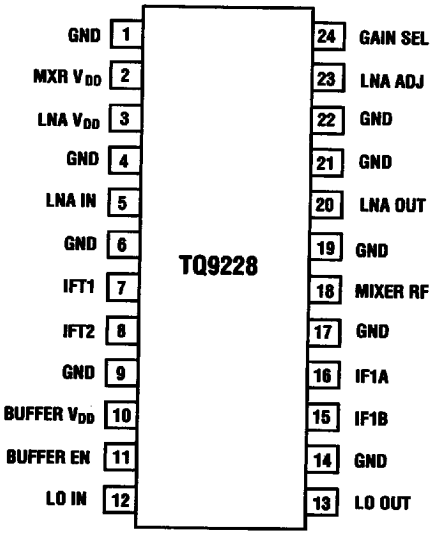
Modes	Gain Select, Buffer En	LNA Gain	Buf Enable
CDMA - TX/RX	1,1	HIGH	On
CDMA - TX/RX Large Signal	0,1	LOW	On
CDMA - Standby	1,0	HIGH	Off
CDMA - Standby Large Signal	0,0	LOW	Off

Pin Descriptions

Pin Name	Pin #	Description
MIXER VDD	2	Mixer supply voltage. Local RF bypass cap required.
LNA VDD	3	LNA supply voltage. Local RF bypass cap required within 0.1" of pin.
LNA IN	5	LNA Input. Internally DC blocked. Requires external noise matching elements.
IFT1	7	Half-IF trap port. Inductor and capacitor IF tuning between pins 7 and 8.
IFT2	8	Half-IF trap port. Inductor and capacitor IF tuning between pins 7 and 8.
BUFFER VDD	10	LO buffer supply voltage. Local bypass cap required within 0.1" of pin.
BUFFER EN	11	On/off control line for LO buffer. HIGH = buffer on, LOW = buffer off.
LO IN	12	Mixer LO input. Internally DC blocked and matched to 50 Ω.
LO OUT	13	LO buffer output port. Requires external capacitor for DC block and LO output tuning.
IF1A	15	Mixer IF output A. Open-drain output. Bias choke and matching to IF filter required.
IF1B	16	Mixer IF output B. Open-drain output. Bias choke and matching to IF filter required.
MIXER RF	18	Mixer RF input port. Internally DC blocked. Requires external match for best return loss.
LNA OUT	20	LNA output. Internally DC blocked and matched to 50 Ω.
LNA ADJ	23	LNA bias current adjust, Series resistor to ground adjusts bias current.
GAIN SEL	24	Gain select control. Logic HIGH = high gain, logic LOW = low gain.
GND	(Note 1)	Ground connection. Use several via holes immediately adjacent to the pins down to backside ground plane. Provides thermal path for heat dissipation and RF grounding. Keep traces physically short. Connect immediately to ground plane.

Notes: 1. GND pins are: 1, 4, 6, 9, 14, 17, 19, 21, 22.
2. Refer to pinout diagram for pin location.

TQ9228 Pinout



General Description

The TQ9228 is a receiver RFIC designed specifically for PCS CDMA applications. It integrates a high-performance LNA+mixer and LO buffer. The RF, LO and IF were designed to support the leading frequency plan in the market. In addition, the part was designeded to support the IS-95/98A standards. The architecture is split in a manner to maximize LNA dynamic range while maintaining excellent downconverter performance

Low Noise Amplifier

The LNA is a single-stage, common-source amplifier designed for low gain (13 dB), very high input intercept (+6 dBm) and low noise (1.5 dB). It is biased on-chip and is first-order, temperature-compensated for stable gain. The LNA contains circuitry to provide a gain step for a downconverter high-input intercept mode. A digital control signal on the gain select line turns the bypass mode on or off. In the low-gain mode, the input signal is routed through a fixed attenuator for the proper gain step.

Mixer and IF Amp

The mixer is a three-stage design comprised of a pre-amplifier, a singly balanced, passive-mixer core and a differential IF amplifier. The mixer itself is a high-input-intercept structure designed for robust operation. Its performance is independent of variations in LO drive and the IF output is decoupled from the mixer core.

Power Supply Connections

The TQ9228 was designed to operate with a single, positive supply voltage over the range of 2.7 V to 4.0 V. The electrical performance variations over this range is described by the typical performance curves. The electrical specifications listed in the specification table apply to a specific, narrower voltage range.

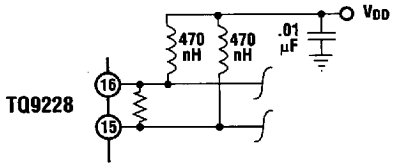
Each of the supply voltage connections must be decoupled to ground with an RF bypass capacitor. A value of 1 nF is recommended for those ports which are internally bypassed. This capacitor should placed within 0.25" of the package. The series 5-ohm resistors shown in the test circuit are optional and are used to provide some additional low-pass filtering on the power supply.

Mixer V_{DD} - The Mixer V_{DD} supply pin is internally bypassed and therefore only needs the standard RF bypass capacitor. Placement is not critical

LNA V_{DD} - The LNA is internally LC matched and brought out through the Vdd connection. Therefore, it is important to place an RF bypass capacitor within 0.1" of the pin.

IF V_{DD} - The IF outputs are biased through chokes connected to V_{DD}. The supply end of the inductors requires a decoupling capacitor.

IF V_{DD} Circuit



Grounding

A low-impedance connection to ground is important for proper RF operation of the TQ9228. It is recommended that multiple via holes to the ground plane be placed at all the ground pins.

LNA Input Match

The TQ9228 LNA was designed for low-noise operation while simultaneously providing a good match to 50 ohms. The LNA requires an external match to achieve the required RF performance. The match is implemented with an external inductor and capacitor configured as shown. The optimal match for noise and return loss is a compromise between gamma optimum noise match and conjugate match.

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LNA Output

The LNA Out port (Pin 20) is internally DC blocked and matched to 50 ohms. It is intended to be connected directly to an image-stripping filter by a printed 50-ohm transmission line. The distance between the LNA out port and the filter is not critical.

Mixer RF Input

The Mixer RF port of the TQ9228 is the input of a common-source feedback amplifier. The input was matched close to 50 ohms. However, in order to properly terminate the image filter with an optimal impedance (e.g. return loss >14 dB), an external tuning network is required. A series capacitor and shunt inductor with the values shown provide the appropriate matching for the mixer RF input.

Mixer LO Input

The LO In port (Pin 12) is internally DC blocked and matched to 50 ohms. It is designed to be connected directly to a VCO output through a 50-ohm transmission line. The LO input provides an excellent match to 50 ohms and requires no external matching components.

LO Buffer Output

The LO Buffer is primarily intended to provide isolation between the buffer output load, the TX upconvert chain, and the input to the buffer, the VCO output. The buffer is internally matched and biased.

Mixer IF Output

The Mixer IF output is a differential "open-drain" configuration. The intent is to permit interfacing to differential IF chain and filtering schemes. The differential output impedance is designed to be close to the required filter termination impedance and is essentially resistive. The "open-drain" outputs require biasing to V_{DD} via an inductor which functions primarily as a choke and secondarily as part of an LC match to the IF filter. A series capacitor is also needed on each of the outputs as part of the impedance matching to the IF filter. The test circuit shows a transformer on the IF output. This is strictly for interfacing to 50 ohms and providing the balun transformer function. Under normal operation, the outputs are designed for direct matching to the IF filter.

Although the TQ9228 was designed with the appropriate nominal gain, it is possible to adjust the value of the nominal gain downward if needed by the system. The gain may be adjusted downward with a shunt resistor across the IF outputs, Pin 15 and Pin 16. This resistor has negligible affect on any of the parameters except gain.

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
DC Power Supply	2.7		5.0	V
Power Dissipation			500	mW
Operating Temperature	-40		85	°C
Storage Temperature	-60		150	°C
Signal Level on Inputs/Outputs			+20	dBm
Voltage to any Non-Supply Pin	-0.3		V_{DD} +.3	V

Notes: 1. Operation or storage in excess of these conditions may result in permanent damage to this device.
2. ESD-sensitive device - Class 1

QSOP-24 Plastic Package

(All dimensions in inches)