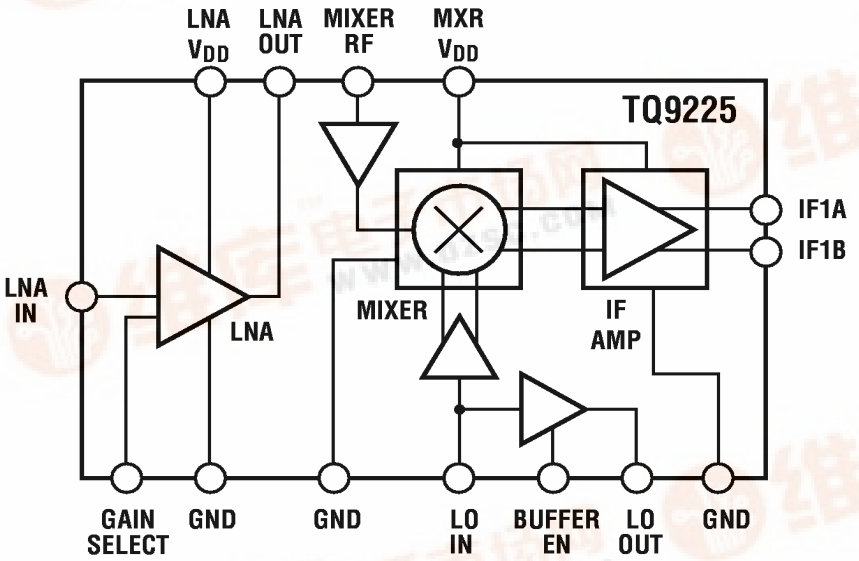
TQ9225

3-V PCS-Band CDMA Downconverter IC



The TQ9225 is a 3-V, RF receiver IC designed specifically for PCS-band CDMA applications. The performance meets the demanding requirements of IS-95/98 standards-based products, both portable and fixed. The downconverter architecture maximizes the LNA dynamic range while maintaining excellent overall downconverter performance. The RF frequency range covers the entire PCS band. The low-side LO and 210 MHz IF are compatible with low-side LO chip-set frequencies. The wide supply voltage range of 2.7 V to 4.0 V permits the use of the part in a variety of supply voltage configurations.

Electrical Specifications

Operating Conditions: V_{DD} = 3.0 V, T_A = 25° C, RF = 1930 to 1990 MHz, LO = 1720 to 1780 MHz, LO Level = -4 to +1 dBm, IF = 210 MHz, Filter IL = 3 dB; unless otherwise specified

Parameter[1]	Conditions	Min.	Typ.	Max.	Units
Gain	High gain	25	28	30.5	dB
	Low gain	4.0	7.5	11.0	dB
Noise Figure	High gain		2.6	3.5	dB
	Low gain		16	17.5	dB
Input IP3	High gain	-12	-10		dBm
	Low gain	+7	+10		dBm
Supply Current [2]	V_{DD} = 3.0 V		50	63	mA

Notes: 1. Min/max values listed are production tested.
2. LO buffer off.

Features

- *Single 3-V operation*
- *Gain select*
- *LO buffer output*
- *Differential IF output*
- *QSOP-24 package*
- *Split LNA architecture*
- *IS 95/98A-compliant performance*

Applications

- *IS-95/98 mobile phones*
- *Wireless local loop*
- *PCS micro-cells*

Electrical Specifications (V_{DD} = 3.0 V)

Operating Conditions: V_{DD} = 3.0 V, T_A = 25° C, Filter IL = 3 dB, RF = 1930 to 1990 MHz, LO = 1720 to 1780 MHz, LO Level = -4 to +1 dBm, IF = 210 MHz; unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Gain	High gain	25.0	28.0	30.5	dB
	Low gain	4.0	7.5	11.0	dB
Noise Figure	High gain		2.6	3.5	dB
	Low gain		16	17.5	dB
Input 3rd-Order Intercept	High gain T_A = 25°C	-12	-10		dBm
	Low gain	+7	+10		dBm
LNA Input IP3	LNA only	+3	+6		dBm
Return Loss	LNA In (with external match)	9.5	12		dB
	LNA Out (high-gain mode)	9.5	15		dB
	LNA Out (low-gain mode)	8.5	11.5		dB
	Mixer RF (with external match)	10	15		dB
	LO In	9.5	16		dB
	LO Out	9.5	14.5		dB
Isolation	LNA In to IFA/IFB	20	50		dB
	LNA In to LO In	20	40		dB
	LNA In to LO Out	10	40		dB
	LO In/Out to LNA In	20	33		dB
	LO In/Out to IFA/IFB	20	50		dB
	LO Out to LO In	17	20		dB
	LNA Out pin to Mixer RF pin	25	45		dB
Supply Current	LNA On, LO Buffer On		53	66	mA
	LNA On, LO Buffer Off		50	63	mA
	LNA Off, LO Buffer On		40	50	mA
	LNA Off, LO Buffer Off		37	47	mA

Parameter	Conditions	Min.	Typ.	Max.	Units
LO Output Power Level	LO Input = -4 dBm	-7.5	-3.5	0	dBm
Output Resistance	Differential mode	475	640	815	ohm
Output Capacitance	Differential mode		0.1	1	pF
LO Buffer Turn-on Time				100	µs
LO Buffer Turn-off Time				100	µs
Input Logic LOW Voltage		0		0.8	V
Input Logic HIGH Voltage		2.3		V_{DD}	V
Input Logic LOW Current				50	µA
Input Logic HIGH Current				200	µA

Electrical Specifications (V_{DD} = 3.6 V)

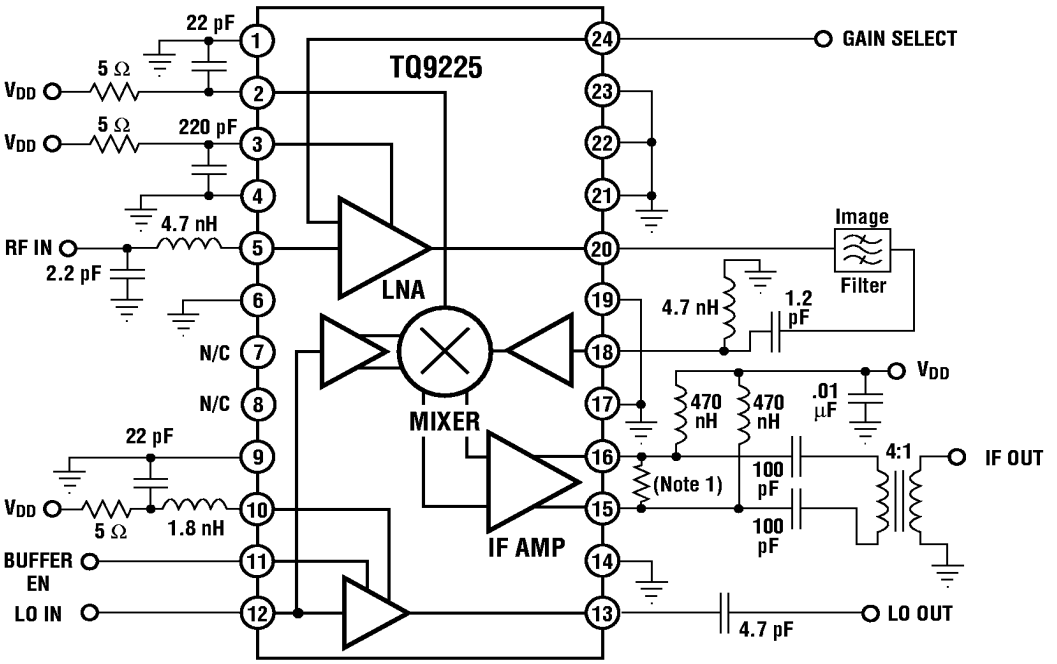
Operating Conditions: V_{DD} = 3.6 V ±5%, T_A = 0 to 70°C, RF = 1930 to 1990 MHz, LO = 1720 to 1780 MHz, LO Level = -4 to +1 dBm, IF = 210 MHz, Filter IL = 3 dB; unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Gain	High gain	24.0	27.5	30.5	dB
	Low gain		7		dB
Noise Figure	High gain		2.4	4.2	dB
	Low gain		16		dB
Input 3rd-Order Intercept	High gain T_A = 25°C	-11			dBm
	Low gain		+11		dBm
LNA Input IP3	LNA only		+7		dBm
Return Loss	LNA In (with external match)	9.5			dB
	LNA Out	9.5			dB
	Mixer RF (with external match)	14.5			dB
	LO In	9.5			dB
	LO Out	9.5			dB
Isolation	LNA In to IFA/IFB	20			dB
	LNA In to LO In	20			dB
	LNA In to LO Out	10			dB
	LO In/Out to LNA In	20			dB
	LO In/Out to IFA/IFB	20			dB
	LNA Out pin to Mixer In pin	25			dB
Supply Current	LNA On, LO Buffer On		65	96	mA
	LNA On, LO Buffer Off		61	92	mA

Parameter	Conditions	Min.	Typ.	Max.	Units
LO Output Power Level	LO Input = -4 dBm	-7.2		0	dBm
Output Resistance	Differential mode	510		875	ohm
Output Capacitance	Differential mode			1	pF
LO Buffer Turn-on Time				100	µs
LO Buffer Turn-off Time				100	µs
Input Logic LOW Voltage	V_{DD} = 2.7 to 4.0	0		0.5	V
Input Logic HIGH Voltage	V_{DD} = 2.7 to 4.0	2.9		V_{DD}	V
Input Logic LOW Current				50	µA
Input Logic HIGH Current				200	µA

Test Circuit

(All signal ports matched to 50 Ω)



Notes: 1. Optional resistor to adjust gain, nominal value.

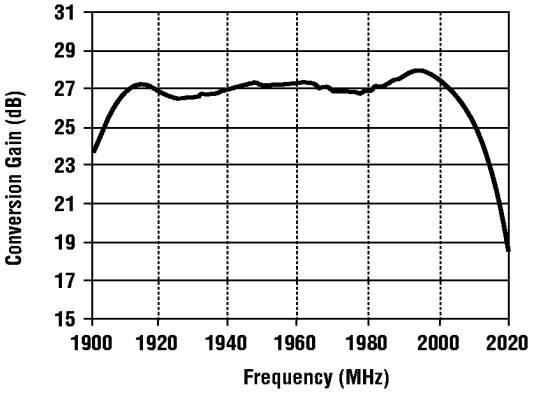
Receiver Mode Control

Modes	Gain Select, Buffer En	LNA Gain	Buf Enable
CDMA - TX/RX	1,1	HIGH	On
CDMA - TX/RX Large Signal	0,1	LOW	On
CDMA - RX	1,0	HIGH	Off
CDMA - RX Large Signal	0,0	LOW	Off

Typical Performance – Downconverter

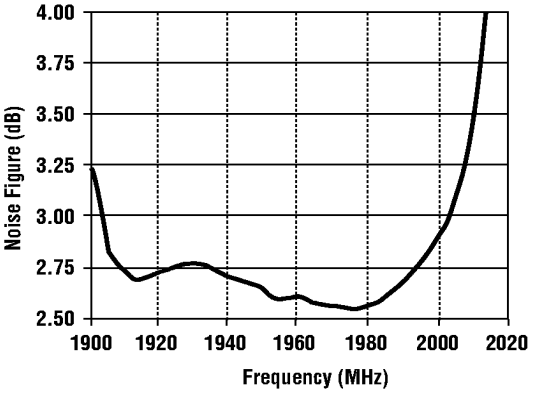
Conversion Gain vs. Frequency

V_{DD} = 3.0 V, T_A = 25° C, P_{LO} = -1 dBm



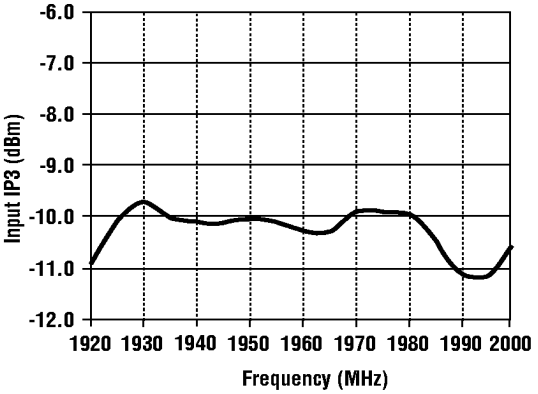
Noise Figure vs. Frequency

V_{DD} = 3.0 V, T_A = 25° C, P_{LO} = -1 dBm



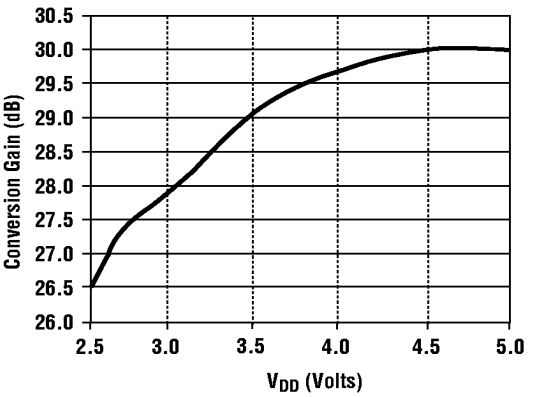
Input IP3 vs. Frequency (P_{LO} = 1 dBm)

V_{DD} = 3.0 V, T_A = 25° C, P_{LO} = -1 dBm



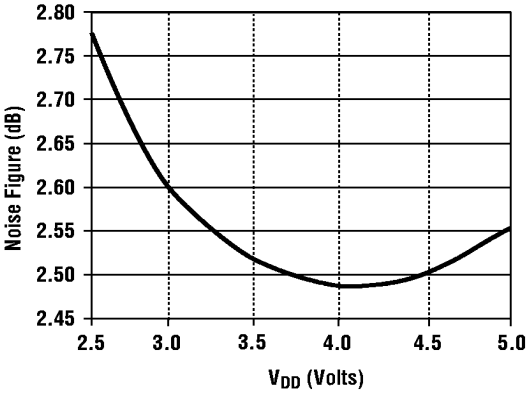
Conversion Gain vs. V_{DD}

T_A = 25° C, RF = 1960 MHz, P_{LO} = -1 dBm



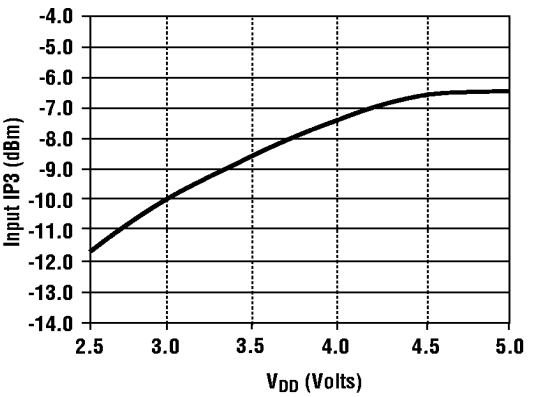
Noise Figure vs. V_{DD}

T_A = 25° C, RF = 1960 MHz, P_{LO} = -1 dBm



Input IP3 vs. V_{DD} (High-gain mode)

T_A = 25° C, RF = 1960 MHz, P_{LO} = -1 dBm



ICs

LNA S-Parameters (High-gain mode)

Freq (GHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
1.800	0.88	-71	2.36	-169	0.016	153	0.31	153
1.820	0.87	-72	2.39	-170	0.017	153	0.31	150
1.840	0.87	-73	2.42	-171	0.017	152	0.30	147
1.860	0.87	-74	2.45	-173	0.017	152	0.30	144
1.880	0.87	-75	2.48	-175	0.018	150	0.29	141
1.900	0.87	-76	2.49	-176	0.019	150	0.28	137
1.920	0.86	-77	2.49	-178	0.019	150	0.28	135
1.930	0.86	-78	2.50	-179	0.020	151	0.28	133
1.940	0.86	-79	2.52	-179	0.021	150	0.28	131
1.950	0.86	-79	2.52	180	0.021	150	0.27	130
1.960	0.86	-80	2.52	179	0.021	148	0.27	128
1.970	0.86	-80	2.52	178	0.021	146	0.26	128
1.980	0.86	-81	2.50	178	0.021	147	0.27	127
1.990	0.86	-81	2.52	177	0.022	148	0.27	125
2.000	0.86	-82	2.54	177	0.023	146	0.27	123
2.020	0.85	-83	2.55	175	0.022	144	0.26	120
2.040	0.85	-84	2.56	174	0.023	145	0.26	118
2.060	0.85	-86	2.58	173	0.024	144	0.26	115
2.080	0.84	-87	2.60	171	0.024	140	0.25	112
2.100	0.84	-88	2.63	170	0.024	142	0.25	110

LNA S-Parameters (Low-gain mode)

Freq (GHz)	|S11|	∠S11	|S21|	∠S21	|S12|	∠S12	|S22|	∠S22
1.920	0.70	-89	0.31	99	0.296	99	0.36	82
1.930	0.70	-90	0.31	98	0.299	98	0.37	80
1.940	0.70	-90	0.31	97	0.303	97	0.37	78
1.950	0.70	-91	0.31	96	0.305	96	0.36	76
1.960	0.69	-91	0.31	95	0.307	95	0.36	75
1.970	0.69	-92	0.31	95	0.309	94	0.36	74
1.980	0.69	-93	0.32	94	0.313	93	0.37	72
1.990	0.69	-93	0.32	94	0.316	92	0.37	70
2.000	0.68	-94	0.32	93	0.316	91	0.37	69

LNA Noise Parameters (typical)

Frequency (GHz)	F_{MIN} (dB)	Γ_{OPT} (Mag)	Γ_{OPT} (Ang)	R_{NOISE} (Ω)
1.900	1.44	0.46	61.4	0.442
1.950	1.29	0.42	56.5	0.404
2.000	1.34	0.38	53.9	0.421

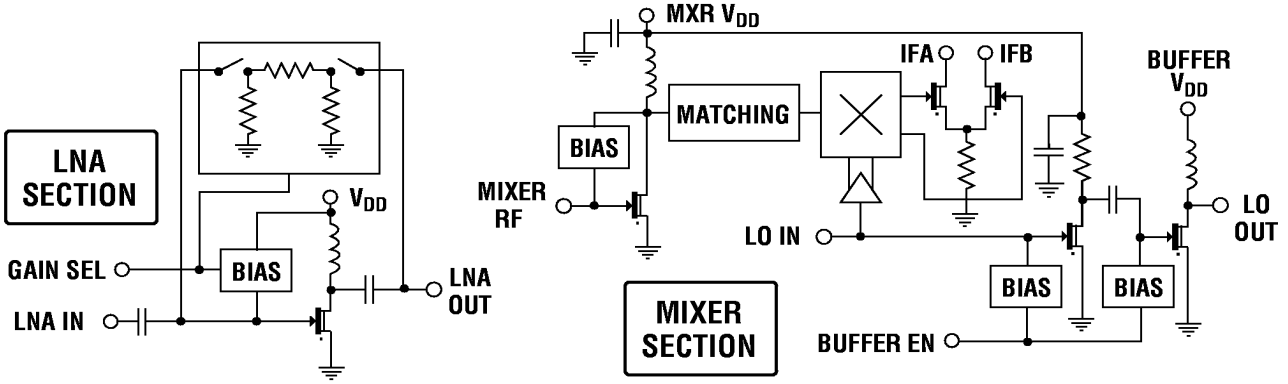
Mixer RF Input Reflection Coefficient

Freq (GHz)	|S11|	∠S11
1.930	0.46	30
1.940	0.47	27
1.950	0.48	24
1.960	0.48	22
1.970	0.50	20
1.980	0.51	19
1.990	0.52	17

Mixer RF Input Reflection Coefficient

Freq (GHz)	|S11|	∠S11
1.720	0.11	91
1.730	0.11	91
1.740	0.11	92
1.750	0.12	92
1.760	0.12	92
1.770	0.13	92
1.780	0.13	92

Simplified Circuit Schematic

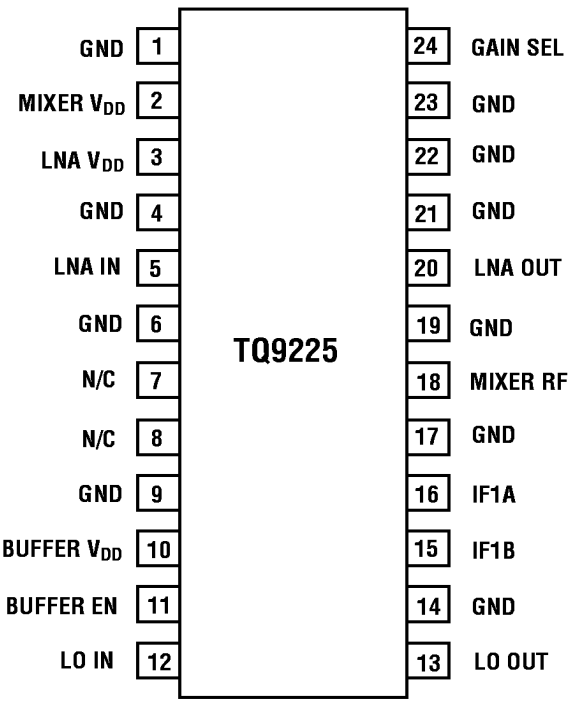


Pin Descriptions

Pin Name	Pin #	Description
MIXER VDD	2	Mixer supply voltage. Local RF bypass cap required.
LNA VDD	3	LNA supply voltage. Local RF bypass cap required within 0.1" of pin.
LNA IN	5	LNA Input. Internally DC blocked. Requires external noise matching elements.
N/C	7,8	No connections.
BUFFER VDD	10	LO buffer supply voltage. Local bypass cap required. Series inductance required for LO output tuning.
BUFFER EN	11	On/off control line for LO buffer. HIGH = buffer on, LOW = buffer off.
LO IN	12	Mixer LO input. Internally DC blocked and matched to 50 Ω.
LO OUT	13	LO buffer output port. Requires external blocking capacitor.
IF1A	15	Mixer IF output A. Open-drain output. Bias choke and matching to IF filter required.
IF1B	16	Mixer IF output B. Open-drain output. Bias choke and matching to IF filter required.
MIXER RF	18	Mixer RF input port. Internally DC blocked. Requires external match for best return loss.
LNA OUT	20	LNA output. Internally DC blocked and matched to 50 Ω.
GAIN SEL	24	Gain select control. Logic HIGH = high gain, logic LOW = low gain.
GND	(Note 1)	Ground connection. Use several via holes immediately adjacent to the pins down to backside ground plane. Provides thermal path for heat dissipation and RF grounding. Keep traces physically short. Connect immediately to ground plane.

Notes: 1. GND pins are: 1, 4, 6, 9, 14, 17, 19, 21, 22, 23.
2. Refer to pinout diagram for pin location.

TQ9225 Pinout



General Description

The TQ9225 is a receiver RFIC designed specifically for PCS CDMA applications. It integrates a high-performance LNA+mixer and LO buffer. The RF, LO and IF were designed to support the leading frequency plan in the market. In addition, the part was designed to support the IS-95/98A standards. The architecture is split in a manner to maximize LNA dynamic range while maintaining excellent downconverter performance

Low Noise Amplifier

The LNA is a single-stage, common-source amplifier designed for low gain (13 dB), very high input intercept (+6 dBm) and low noise (1.5 dB). It is biased on-chip and is first-order, temperature-compensated for stable gain. The LNA contains circuitry to provide a gain step for a downconverter high-input intercept mode. A digital control signal on the gain select line turns the bypass mode on or off. In the low-gain mode, the input signal is routed through a fixed attenuator for the proper gain step.

Mixer and IF Amp

The mixer is a three-stage design comprised of a pre-amplifier, a singly balanced, passive-mixer core and a differential IF amplifier. The mixer itself is a high-input-intercept structure designed for robust operation. Its performance is independent of variations in LO drive and the IF output is decoupled from the mixer core.

Power Supply Connections

The TQ9225 was designed to operate with a single, positive supply voltage over the range of 2.7 V to 4.0 V. The electrical performance variation over this range is described by the typical performance curves.

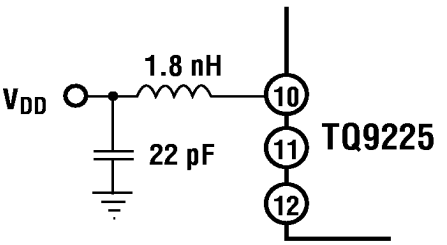
Each of the supply voltage connections must be decoupled to ground with an RF bypass capacitor. A value of 1 nF is recommended for those ports which are internally bypassed. This capacitor should placed within 0.25" of the package. The series 5-ohm resistors shown in the test circuit are optional and are used to provide some additional low-pass filtering on the power supply.

Mixer V_{DD} - The Mixer V_{DD} supply pin is internally bypassed and therefore only needs the standard RF bypass capacitor. Placement is not critical

LNA V_{DD} - The LNA is internally LC matched and brought out through the Vdd connection. Therefore, it is important to place an RF bypass capacitor within 0.1" of the pin.

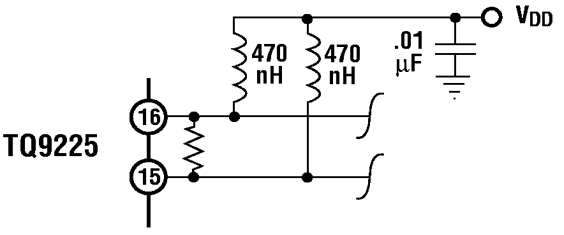
Buffer V_{DD} - The connection to V_{DD} on the port is critical. A series inductance must be added to optimally match the LO buffer. An RF bypass capacitor is needed to decouple the supply end of the inductor.

Buffer V_{DD} Connection



IF V_{DD} - The IF outputs are biased through chokes connected to V_{DD}. The supply end of the inductors requires a decoupling capacitor.

IF V_{DD} Circuit



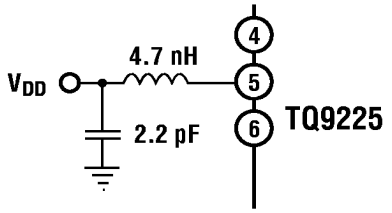
Grounding

A low-impedance connection to ground is important for proper RF operation of the TQ9225. It is recommended that multiple via holes to the ground plane be placed at all the ground pins.

LNA Input Match

The TQ9225 LNA was designed for low-noise operation while simultaneously providing a good match to 50 ohms. The LNA requires an external match to achieve the required RF performance. The match is implemented with an external inductor and capacitor configured as shown. The optimal match for noise and return loss is a compromise between gamma optimum noise match and conjugate match. Both the gamma optimum and conjugate matching impedance values are shown in the table below to permit choice of the appropriate compromise. A recommended set of lumped-element values is shown below. These values provide a noise figure of 1.5 dB and a return loss >10 dB.

LNA Input Match



Optimum Noise Match and Conjugate Match

Frequency (GHz)	Γ_{OPT} (Mag)	Γ_{OPT} (Ang)	Γ_{CONJ} (Mag)	Γ_{CONJ} (Ang)
1.900	0.46	61	0.87	76
1.950	0.42	57	0.86	79
2.000	0.38	54	0.86	821

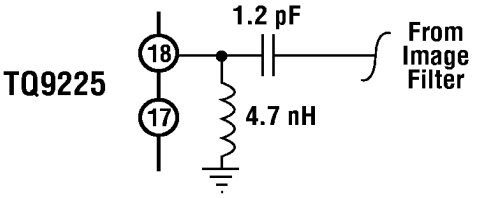
LNA Output

The LNA Out port (Pin 20) is internally DC blocked and matched to 50 ohms. It is intended to be connected directly to an image-stripping filter by a printed 50-ohm transmission line. The distance between the LNA out port and the filter is not critical.

Mixer RF Input

The Mixer RF port of the TQ9225 is the input of a common-source feedback amplifier. The input was matched close to 50 ohms. However, in order to properly terminate the image filter with an optimal impedance (e.g. return loss >14 dB), an external tuning network is required. A series capacitor and shunt inductor with the values shown provide the appropriate matching for the mixer RF input.

Mixer RF Input Match



Mixer LO Input

The LO In port (Pin 12) is internally DC blocked and matched to 50 ohms. It is designed to be connected directly to a VCO output through a 50-ohm transmission line. The LO input provides an excellent match to 50 ohms and requires no external matching.

LO Buffer Output

The LO Buffer is primarily intended to provide isolation between the buffer output load, the TX upconvert chain, and the input to the buffer, the VCO output. The buffer is internally matched and biased, but can be tuned externally for optimizing the frequency response of the buffer. A small-value inductor and capacitor comprise the remaining amount of LC tuning that is needed for the buffer. A series inductance of 1.8 nH on Pin 10 and a series capacitance of 4.7 pF on Pin 13 is necessary to tune the buffer and match the output to 50 ohms.

Mixer IF Output

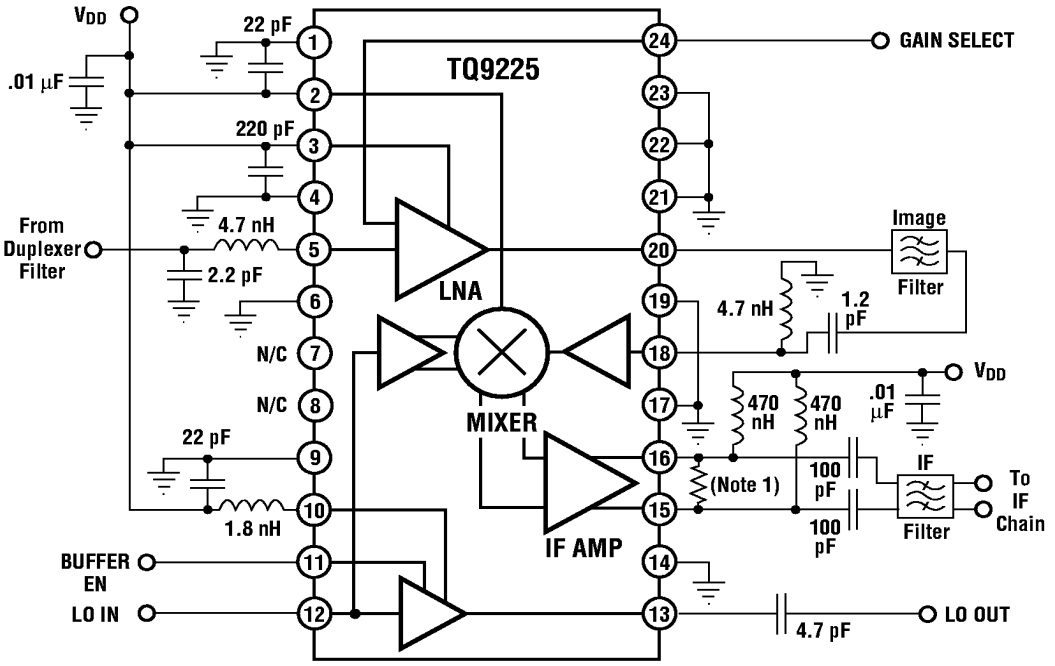
The Mixer IF output is a differential "open-drain" configuration. The intent is to permit interfacing to differential IF chain and filtering schemes. The differential output impedance is designed to be close to the required filter termination impedance and is essentially resistive. The "open-drain" outputs require biasing to V_{DD} via an inductor which functions primarily as a choke and secondarily as part of an LC match to the IF filter. A series capacitor is also needed on each of the outputs as part of the impedance matching to the IF filter. The test circuit shows a transformer on the IF output.

This is strictly for interfacing to 50 ohms and providing the balun transformer function. Under normal operation, the outputs are designed for direct matching to the IF filter.

Although the TQ9225 was designed with the appropriate nominal gain, it is possible to adjust the value of the nominal gain downward if needed by the system. The gain may be adjusted downward with a shunt resistor across the IF outputs, Pin 15 and Pin 16. This resistor has negligible affect on any of the parameters except gain.

Application Circuit

(All signal ports matched to 50 Ω)



Notes: 1. Optional resistor to adjust gain, nominal value.

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
DC Power Supply	2.7		5.0	V
Power Dissipation			500	mW
Operating Temperature	-40		100	°C
Storage Temperature	-60		150	°C
Signal Level on Inputs/Outputs			+20	dBm
Voltage to any Non-Supply Pin	-0.3		V_{DD} +.3	V

Notes: 1. Operation or storage in excess of these conditions may result in permanent damage to this device.

QSOP-24 Plastic Package

(All dimensions in inches)