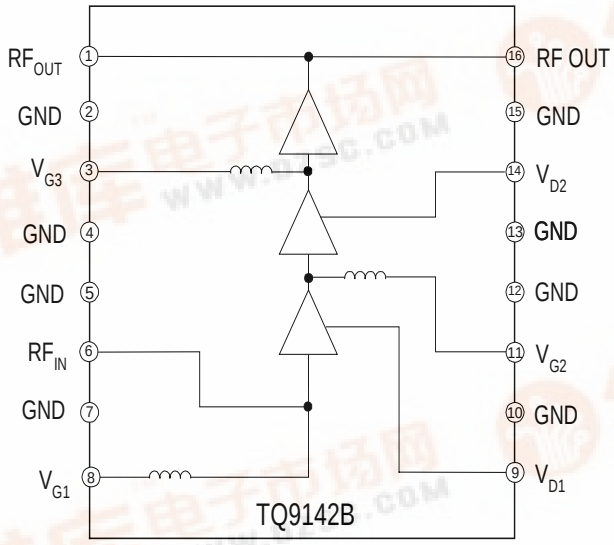
TriQuint SEMICONDUCTOR

WIRELESS COMMUNICATIONS DIVISION

TQ9142B

DATA SHEET

High-Efficiency 3-Stage AMPS Power Amplifier IC



Features

- *60% drain efficiency*
- *+31.0 dBm power output @4.8V*
- *4.8 V to 6.0 V battery operation*
- *S0-16 package*
- *50-ohm matched input*

Applications

- *AMPS Mobile Phones*
- *CDPD Terminals/Modems*

Product Description

The TQ9142B is a highly efficient 3-stage power amplifier developed for handsets and portable terminals operating in the AMPS cellular band (824 to 849 MHz). The part is designed to require minimal external circuitry for matching or bias, simplifying design and keeping board space and cost to a minimum. Access to each stage's gate and drain voltages is provided for maximum flexibility in selection of output power control method, making output power vs. efficiency tradeoffs, or for implementing alternative biasing schemes. The amplifier is packaged in a SOIC-16 plastic package with specially modified central thermal tabs. These tabs provide reliable operation for the 1.4 Watt power output.

Electrical Specifications[1]

Parameter	Min	Typ	Max	Units
Output Power	+30	+31		dBm
Efficiency	55	60		%
Input Return Loss		10		dB

Note 1: Test Conditions: V_{DD} = 4.8 V, V_{GG} = -3.5 V, Freq. = 836 MHz, P_{IN} = 0 dBm, T_C = 25 °C

Note 2: Min/max values 100% production tested.

Electrical Characteristics [1]

Parameter	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Frequency	tuned for cellular band	824		849	MHz
Supply Voltage (V_{DD})		2.7	5.0	7.00	V
Temperature	measured at case	-40	25	+110	°C
P_{OUT}		30.0	31.0		dBm
Efficiency		55	60		%
Input Return Loss			10		dB
Power Control Range			25		dB
Rx Band Noise [2]			-88		dBc
Small Signal Gain	P_{IN} = -10 dBm		40		dB
Harmonics					
2nd Harmonic			-35		dBc
3rd Harmonic			-45		dBc
Negative Supply Current			2	5	mA
Spurious (Stability) [3]	P_{IN} = -40 to +0 dBm		-80		dBc
Ruggedness [4]			No degradation		

Note 1: Test Conditions: V_{DD} = 4.8 V, V_{GG} = -3.5 V, Freq. = 836 MHz, P_{IN} = 0 dBm, BW = 30 kHz, T_C = 25 ° C.

Note 2: Load VSWR set to 7:1 and angle varied 360°. All spurious outputs less than –80 dBc. No large-signal oscillations permitted

Note 2: Noise power measured in 30 kHz bandwidth at the transmit frequency plus 45 MHz.

Note 2: Burnout testing. Load set to 50 ohms, output power measured at nominal test conditions. Load VSWR set to 10:1 and the angle varied 360° over 60 seconds. Load set to 50 ohms; output power is measured again and compared with the first measurement to check for no degradation from first measurement.

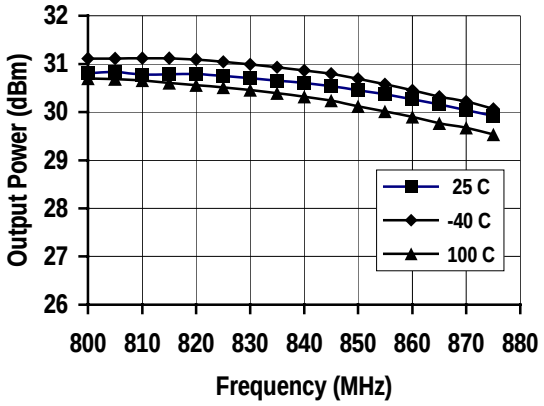
Absolute Maximum Ratings

Parameter	Value	Units
DC Power Supply	8.0	V
DC Gate Voltage	-5.0 to –0.5	V
RF Input Power	+10	dBm
Storage Temperature	-55 to +150	°C
Operating Temperature (case)	-40 to +125	°C
Theta j-c	5	°C/Watt

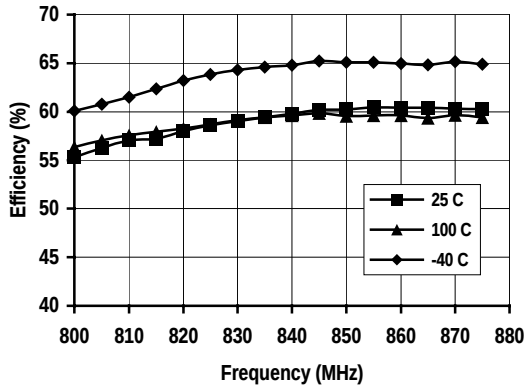
Typical Performance

Test Conditions (Unless Otherwise Specified): V_{DD} = 4.6 V, Freq. = 836 MHz, V_{GG} = -3.5 V, P_{IN} = 0 V, V_{BC} = 2.7 V, T_C = 25°C

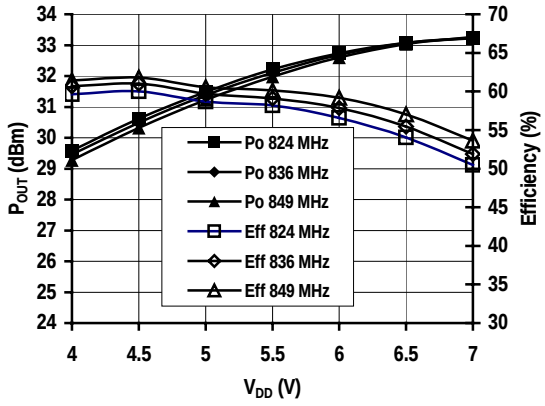
Output Power vs. Frequency vs. Temperature



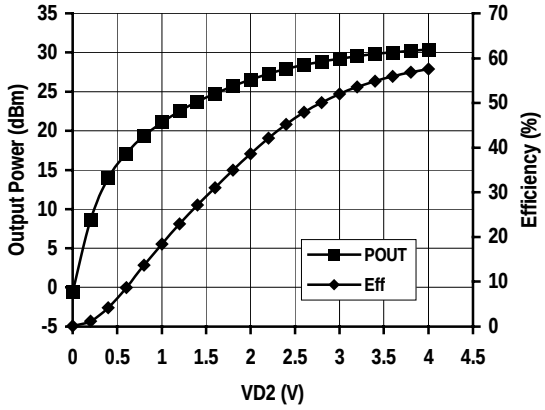
Efficiency vs. Frequency vs. Temperaure



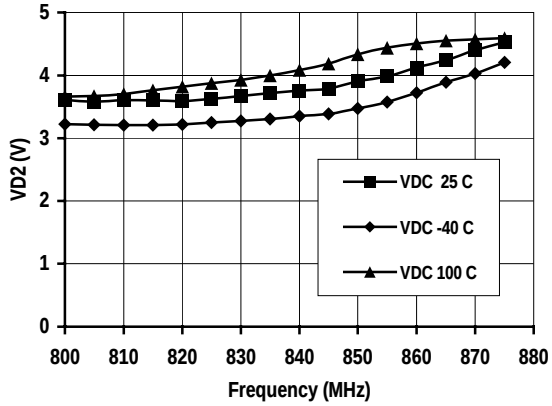
Output Power & Eff. vs. VDD vs. Frequency



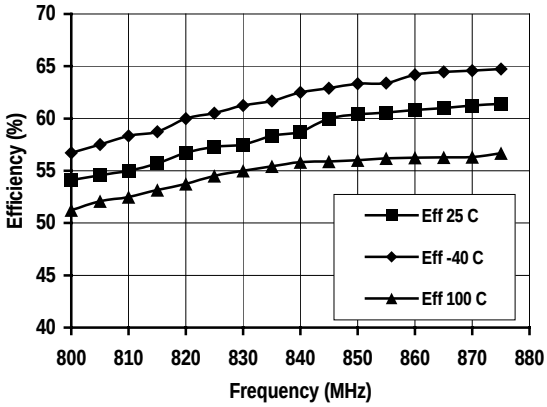
Output Power & Eff vs. VD2



VD2 vs. Frequency vs. Temp (POUT=30 dBm)



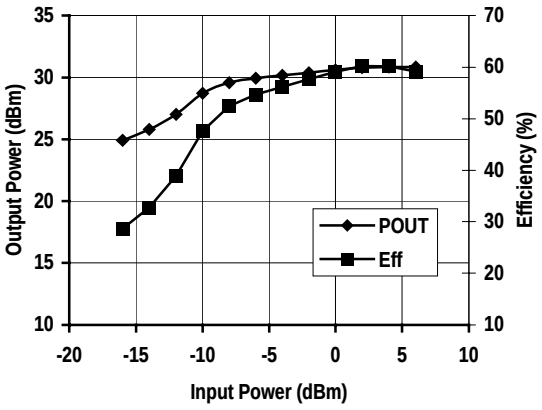
Efficiency vs. Freq. vs. Temp (POUT=30 dBm)



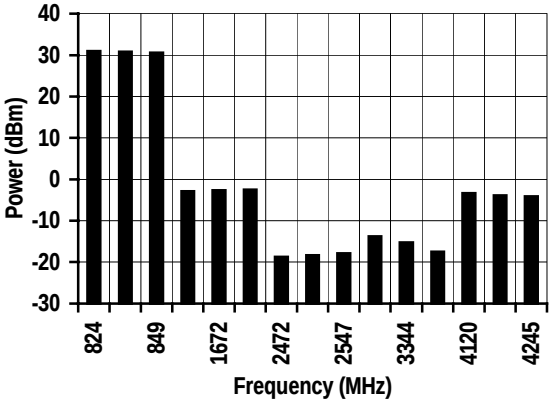
Typical Performance

Test Conditions (Unless Otherwise Specified): V_{DD} = 4.6 V, Freq. = 836 MHz, V_{GG} = -3.5 V, P_{IN} = 0 V, V_{BC} = 2.7 V, T_C = 25°C.

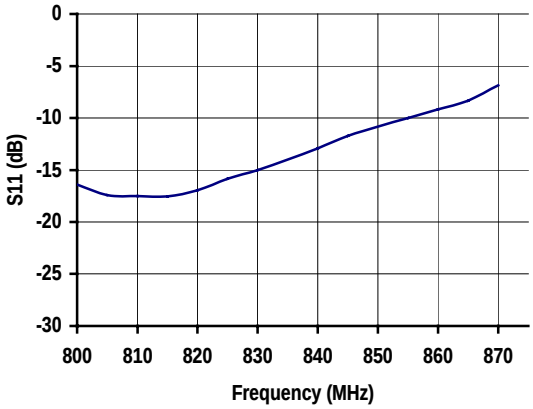
Output Power & Eff. vs. Input Power



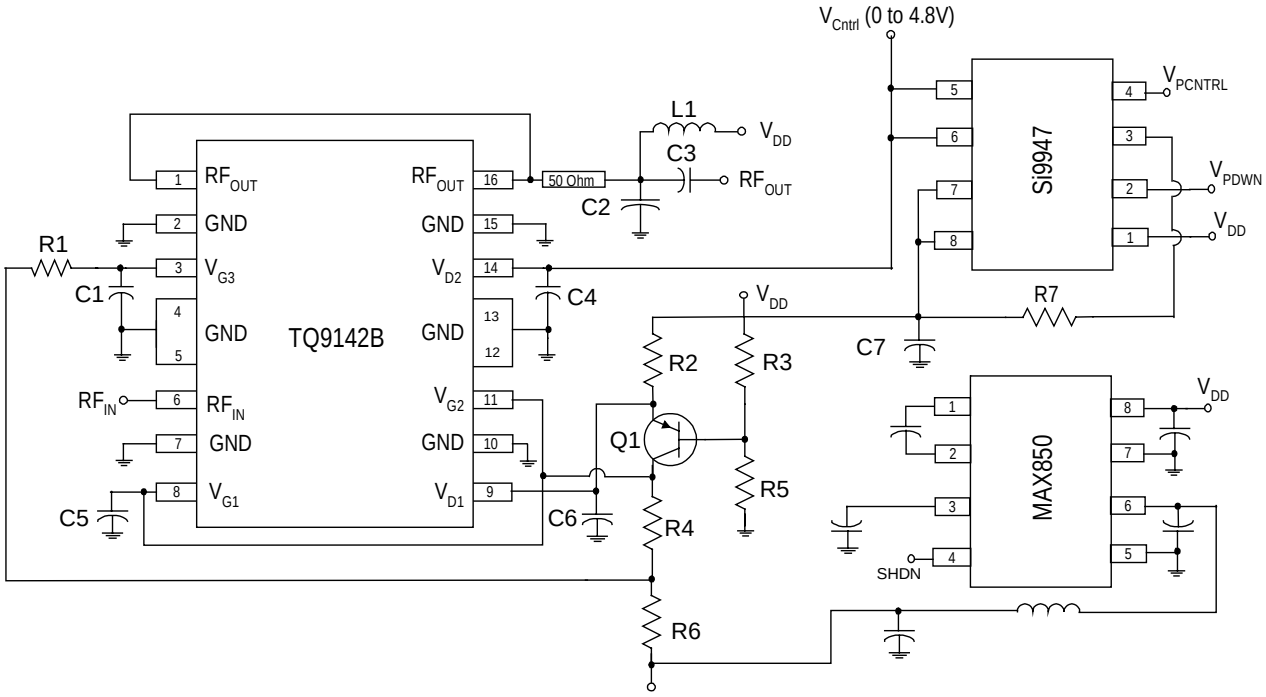
Fundamental & Harmonics vs. Frequency



S11 vs. Frequency



Application/Test Circuit



Bill of Material for TQ9142B Power Amplifier Application/Test Circuit

Component	Reference Designator	Part Number	Value	Size	Manufacturer
Power Amplifier IC		TQ9142B		Power SO-16	TriQuint Semiconductor
PNP Transistor	Q1	2N3906			
Capacitor	C1, C4, C5, C6, C7	MCH155F103ZK	0.1 µF	0402	Rohm
Capacitor	C2	MCH155A8R2CK	8.2 pF	0402	Rohm
Capacitor	C3	MCH155A330JK	33 pF	0402	Rohm
Resistor	R1	MCR01JW100	10 Ω	0402	Rohm
Resistor	R2	MCR01JW240	24 Ω	0402	Rohm
Resistor	R3	MCR01JW1R3	1.3 kΩ	0402	Rohm
Resistor	R4	MCR01JW221	220 Ω	0402	Rohm
Resistor	R5	MCR01JW3R6	3.6 kΩ	0402	Rohm
Resistor	R6	MCR01JW1R3	1.0 kΩ	0402	Rohm
Resistor	R7	MCR01JW510	51 Ω	0402	Rohm
Inductor	L1	KL32TE047J	47 nH	1210	KOA

TQ9142B Operation

The TQ9142B is a gallium arsenide (GaAs) power FET amplifier. It has three stages of gain and features 1 Watt output power at 60% drain efficiency. It can operate at supply voltage from 4.8 to 6.0 V. The device is optimized for operation at frequencies from 824 to 849 MHz. The input is matched to 50 ohms and a simple output match and bypassing complete the minimal external circuitry required for normal operation. The output match and all gate and drain voltages are access8ible, allowing the device to be optimized for supply voltage, output power and efficiency.

The TQ9142B is packaged in a low-cost SOIC-16 package with thermal tabs. It is optimized for use as the transmit amplifier in analog cellular (AMPS) phones and Cellular Digital Packet Data (CDPD) wide-area network (WAN) applications. Its high efficiency, high output power and ease of use make the TQ9142B an excellent solution for RF system designers with tight time to market and cost requirements.

Gate Biasing

A negative voltage is required to bias the TQ9142B Power Amplifier. This is usually generated from the battery voltage with a commercially available charge pump IC such as the Harris 7660 or one of the Maxim 850 series Negative Supply Generator ICs. A simple resistive voltage divider can be used to produce the gate voltages for each stage, but the most consistent operation of the amplifier will be obtained by using the active bias circuit shown in the Application/Test Circuit Schematic. The following table gives the approximate values of gate voltage for the TQ9142B at 4.8 V and at 5.8 V.

Nominal Gate Bias Voltages

V_{DD}	4.8 V	5.8 V
V_{G1}	-1.3 V	-1.0 V
V_{G2}	-1.3 V	-1.4 V
V_{G3}	-1.8 V	-1.7 V

The specific values required for optimum performance vary slightly due to fabrication tolerances in FET pinchoff voltage. The active bias circuit overcomes these small variations and provides the extremely repeatable performance and operation need for high volume production

For a fixed output-matching network, output power increases monotonically but gradually, as gate voltage becomes more positive. Efficiency tends to rise to a peak, then to decrease with more positive gate voltage. See the P_{OUT} and efficiency vs. V_{G2} plots.

Quiescent current, the total drain current flowing with no RF drive, also tends to increase with more positive gate voltage, and must be considered when selecting “optimum” gate bias voltages. The bias stabilization circuit used in the Application /Test Circuit Schematic does an excellent job of controlling quiescent current with variations in FET pinch-off voltage.

As with all GaAs power FETs, it is imperative to ensure that the gate bias is present before applying the drain voltage. Without the gate control, the drain current will rise to full I_{DSS} (-1.5 A), which is potentially destructive to power FETs which are designed to operate at 20% to 50% of I_{DSS}. This is usually more of a problem in a lab test environment, but it is a good idea to provide safeguards in the circuit design to minimize the risk that V_{DD} is applied for any significant length of time without V_{GG} applied.

Output Match

For maximum output power and efficiency, the output matching circuit for the TQ9142B is implemented off-chip with high-Q components. The use of external matching elements allows for some tradeoff adjustments to be made between supply voltage, output power and efficiency. It also allows some flexibility for optimizing the performance in different frequency ranges near the cellular band.

The desired output match impedance for optimum output power should have the impedance for optimum output power should have the impedance shown in the following table.

Output Power Match

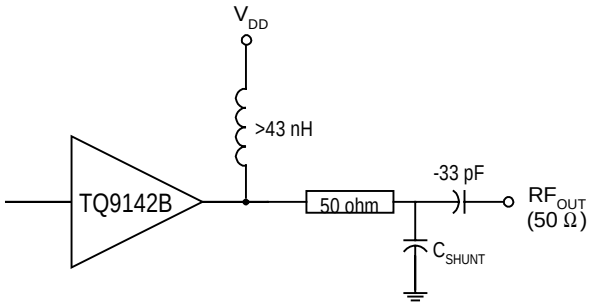
V_{DD}	4.8 V	5.8 V
S11	$.76 \angle -179^{o}$	$.73 \angle -178^{o}$
Impedance	6.77 – j.36 ohm	7.74 + j.74 ohm

The basic output network for the TQ9142B, (and for most GaAs FET power amplifiers), consists of a series inductor followed by a shunt capacitor. An RF choke for bringing the output stage supply voltage and a DC blocking capacitor are also needed.

The series inductance can be realized using a series transmission line or a combination of a series transmission line with a lumped element inductor. The transmission line characteristic impedance should be kept at 50 ohms.

The preferred topology for the output match is shown in the following figures for both the transmission line approach and the combination transmission line/lumped inductor approach.

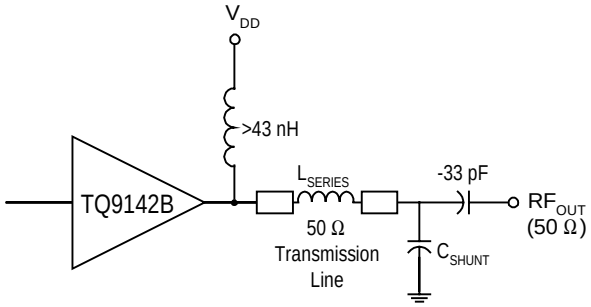
Output Match Topology – Transmission Line



Transmission Line Power Match

V_{DD}	4.8 V	5.8 V
Line Length	338 mils	365 mils
C_{SHUNT}	8.2 pF	6.8 pF

Output Match Topology – Lumped Inductance



Lumped Inductor Power Match

V_{DD}	4.8 V	5.8 V
L_{SERIES}	3.3 nH	3.9 nH
C_{SHUNT}	10 pF	8.2 pF

Please note that the value shown in the table for L_{SERIES} includes the equivalent inductance of any transmission line connecting the power amplifier to the inductor and any transmission line connecting the inductor to the shunt capacitor. Since these lines vary significantly from layout to layout, no attempt has been made here to estimate the approximate value of the physical lumped inductor. The closest standard values of lumped inductors that are lower than the required values are 2.2 nH and 1.8 nH. The connecting transmission lines must be kept fairly short since lumped inductors with values of less than 1.2 nH are not available in most sizes.

Power Control

The best method of power control for the TQ9142B is to vary VD2. It is also possible to vary any of the gate voltages to achieve the same result, but the bias stabilization circuit shown in the Application/Test Schematic works best if VD2 is the control voltage.

Power Down Function

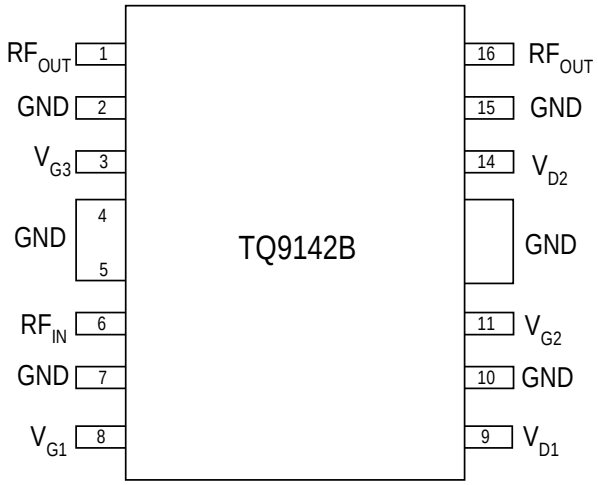
To achieve minimum current leakage in standby mode, a silicon PMOS switching FET (PFET) such as the Siliconix SI9947 can be used in series with the supply voltage. When $V_{STANDBY}$

(active high) is applied to the gate of the PFET, the switch is turned off and only a few microamperes of current will flow. When VSTANDBY = 0, the switch is turned on and VDD is applied to the power amplifier. Typically, the switch will drop the supply voltage by 0.1 to 0.2 V.

Single Supply Operation (Negative Voltage Generators

Depletion-mode GaAs power FETs require a negative gate bias voltage with respect to the grounded source. Several highly efficient negative supply generator ICs are available, such as the Maxim MAX850. The Application Circuit Schematic includes the negative supply. The silicon PFET and the bias circuit to illustrate a complete solution suitable for many cellular telephone designs.

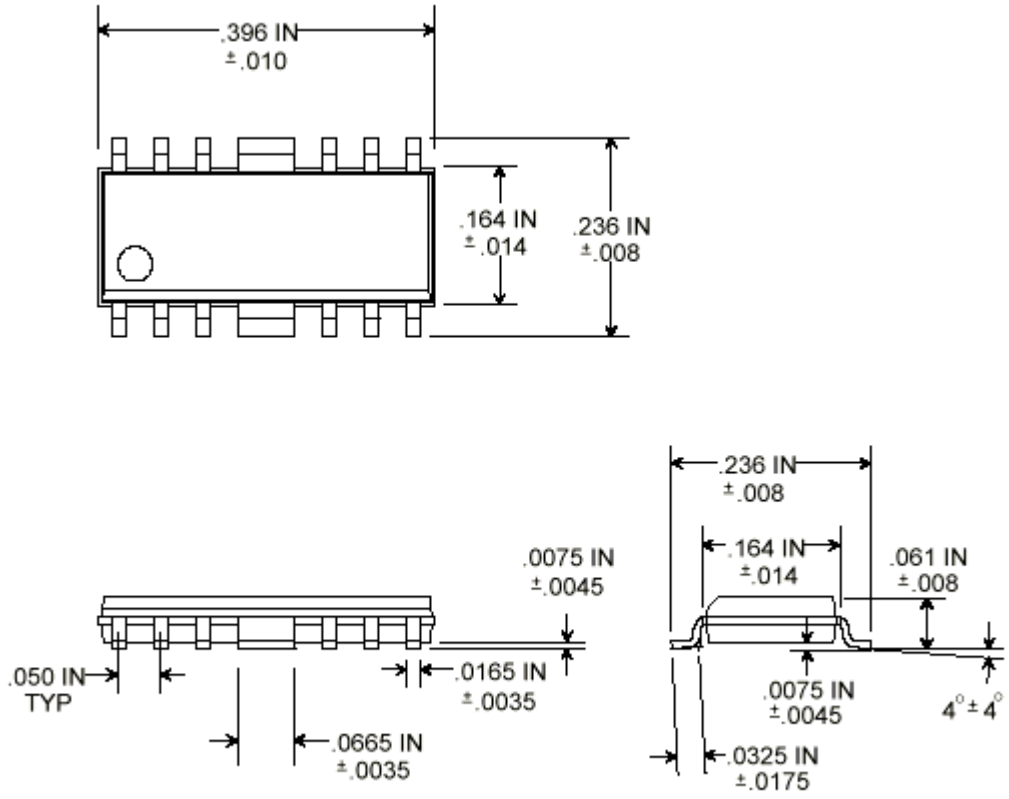
Package Pinout



Pin Descriptions

Pin Name	Pin #	Description and Usage
RF_{OUT}	1, 16	Power amplifier output. Simple bur critical matching circuit required.
V_{G3}	3	Output stage gate voltage. Requires series resistor near device for stability. Local bypass capacitor required.
RF_{IN}	6	Power amplifier input. Matched to 50 ohms. Internal DC block.
V_{G1}	8	First- stage gate voltage. Set V_{G1} = -1.5V or use bias stabilization circuit.
V_{D1}	9	Input stage supply voltage. Local bypass capacitor recommended. Use the same voltage as V_{D3} or use bias stabilization circuit.
V_{G2}	11	Second stage gate voltage. Local bypass capacitor required.
V_{D2}	14	Second stage drain voltage. Local bypass capacitor required. Use the same voltage as V_{D3}
GND	2, 4, 5, 7, 10,12,13,15	Ground connections. Provide thermal path for heat dissipation and RF grounding. Very important to place multiple via holes immediately adjacent to the pins.

Package Type: SOIC-16 Plastic Package with Thermal Tabs



Additional Information

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