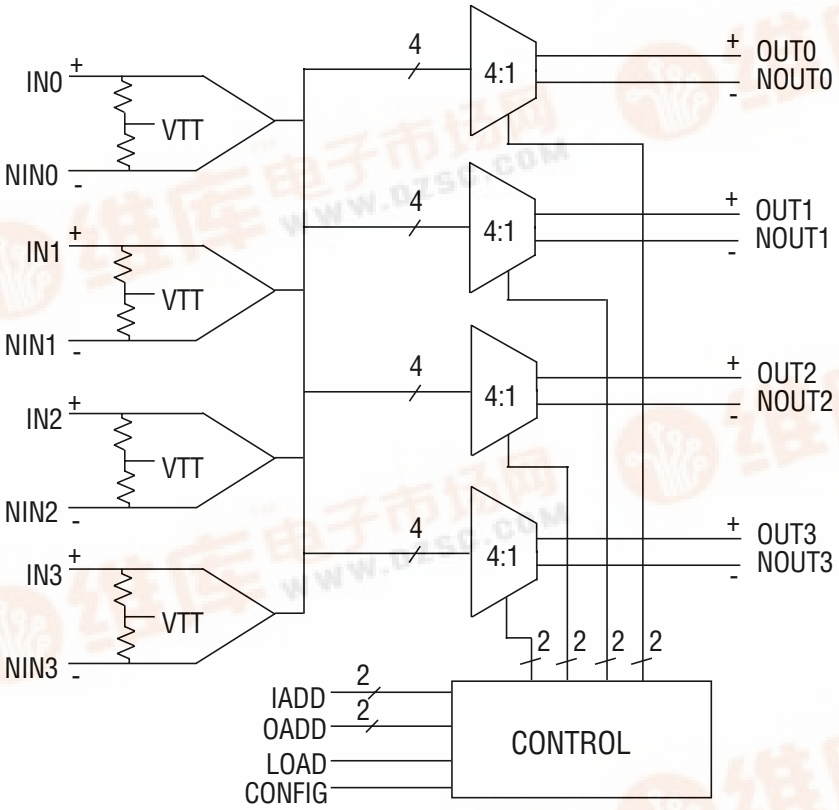
TQ8004

2.7 Gbit/sec 3.3V 4x4 Digital Crosspoint Switch



Features

- 2.7 Gb/s port data bandwidth
- Single 3.3V power supply
- Fully differential data path
- Non-blocking architecture
- Differential PECL I/O TTL control inputs
- On-chip input termination
- Low jitter and channel to channel signal skew
- Double configuration latches
- Small 28-pin TSSOP package

Applications

- Telecom/Datacom/Video switching
- Fanout buffering
- Protection Switching

The TQ8004 is a non-blocking 4 X 4 digital crosspoint switch capable of data rates greater than 2.7 Gigabits per second per port. Utilizing a fully differential data path from input to output, the TQ8004 offers a high data rate with exceptional fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter, low crosstalk and minimum signal skew. The TQ8004 is ideal for high speed data switching applications, as well as high fidelity buffering or protection switching.

The non-blocking architecture uses 4 fully independent 4:1 multiplexers, allowing each input port to be independently programmed to any output port.

SWITCHING PRODUCTS

Circuit Description

Data inputs

The 4 input channels are differential PECL compatible, referenced to VDD = 3.3V power supply (LVPECL). All LVPECL inputs have on-chip 50 Ohm termination to VTT.

For AC coupled designs an internal bias generator can be used to supply the VTT voltage. An on-chip voltage divider generates the VTT voltage at VDD-1.3V with an impedance of 800 Ohms. Due to the high impedance of the internal VTT source it is suited only for AC coupled input schemes.

For DC coupled designs VTT needs to be externally supplied, nominally at VDD-2.0V for LVPECL systems. Note that the external source needs to be able to sink current.

If any inputs are unused, terminate one side of any unused input pair to GND through a 500 Ohm or smaller resistor. This will prevent unwanted oscillations.

Data outputs

The 4 output channels are differential PECL and are designed to be terminated through 50 Ohm to VDD-2.0V. Unused outputs can be left unterminated.

Control inputs

The control inputs are TTL compatible. Unconnected inputs will default to a logic HI level.

Switch configuration

The switch is configured by programming each output to a specific input. Each of the 4 output channels have two sets of program store latches. The first, or program latch, stores a new input configuration prior to application to the switch core. The second, or configuration latch, stores the current input configuration which is applied to the switch core. The use of two sets of program storage latches allows for a new set of input configurations to be loaded simultaneously without disturbing the existing configuration.

The address of the desired output is applied to OADD(0:1). The input address is applied to IADD(0:1). The input address defines which input port connects to the selected output port. The new configuration is loaded into the program latches by asserting the LOAD signal high and is latched when LOAD is de-asserted.

The process is repeated for each new output port configuration. Only the output ports which are to receive a new input port configuration need to be programmed in this manner. The new configurations are not applied to the switch core at this time.

After all of the new configurations have been loaded into the program latches, the CONFIGURE input is asserted high and the data in the program latches is loaded into the configuration latches. The data is latched when CONFIGURE is de-asserted. Data integrity is maintained on output ports not receiving a new configuration

The switch core receives the new configuration immediately following the assertion of CONFIGURE. The integrity of the data on any re-configured output port is unknown for a period t_{dcf} from the time CONFIGURE is asserted.

The LOAD and CONFIGURE inputs can be asserted simultaneously. In this mode, the new configuration will be applied to the switch when LOAD is asserted.

Summary of the IADD(0:1) and OADD(0:1):

IADD1	IADD0	Input
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

OADD1	OADD0	Output
0	0	OUT0
0	1	OUT1
1	0	OUT2
1	1	OUT3

Specifications

Specifications subject to change without notice

Table 1. Absolute Maximum Ratings[4]

Parameter	*Condition*	*Symbol*	*Minimum*	*Nominal*	*Maximum*	*Unit*
Storage Temperature		T_{store}	–65		150	°C
Junction Temperature		T_{CH}	–65		150	°C
Case Temperature w/bias	(1)	T_C	0		100	°C
Supply Voltage	(2)	V_{DD}	0		5.5	V
Voltage to any input	(2)	V_{in}	–0.5		V_{DD} + 0.5	V
Voltage to any output	(2)	V_{out}	–0.5		V_{DD} + 0.5	V
Current to any LVTTL input	(2)	I_{in}	–1.0		1.0	mA
Current to any LVPECL input	(2)	I_{in}	–65		65	mA
Current from any output	(2)	I_{out}			40.0	mA
Power Dissipation of output	(3)	P_{out}			50.0	mW

Notes: 1. Tc is measured at case top.
2. All voltages are measured with respect to GND (0V) and are continuous.
3. Pout = (V_{DD} – V_{out}) x I_{out} .
4. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 2. Recommended Operating Conditions [3]

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_A	Operating Temperature	0	—	85	°C	1
V_{DD}	Supply Voltage	3.14	—	3.47	V	
I_{DD}	Current Positive Supply			300		mA
V_{TT}	Load Termination Supply Voltage		V_{DD} – 2.0		V	2
R_{LOAD}	Output Termination Load Resistance		50		Ω	2
Θ_{JA}	Thermal Resistance Junction to Ambient		40			°C/W

Notes: 1. Package thermal pad to be soldered to PCB.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions. Note that the value shown is for DC coupled LVPECL I/O.
3. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. DC Characteristics—PECL I/O [3]

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input common mode voltage range		V_{ICOM}	V_{DD} – 1500	—	V_{DD} – 1100	mV
Input differential voltage (pk-pk)	(1)	V_{IDIFF}	600	—	2400	mV
Output common mode voltage range		V_{OCOM}	V_{DD}-1500	—	V_{DD} – 1100	mV
Output differential voltage (pk-pk)	(1,2)	V_{ODIFF}	1200	—	2400	mV
Input termination resistance		R_{IN}		50		Ohm
Input capacitance		C_{IN}	—	2.5	—	pF
Output capacitance		C_{OUT}	—	2.5	—	pF
ESD breakdown rating		V_{ESD}	1000	—	—	V

Table 4. DC Characteristics—TTL Inputs[3]

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0	—	V_{DD}	V
Input LOW voltage		V_{IL}	0	—	0.8	V
Input HIGH current	$V_{IH(MAX)}$	I_{IH}	—	—	200	uA
Input LOW current	$V_{IL(MIN)}$	I_{IL}	–400	–200	—	uA
Input capacitance		C_{IN}	—	2.5	—	pF
ESD breakdown rating		V_{ESD}	1000	—	—	V

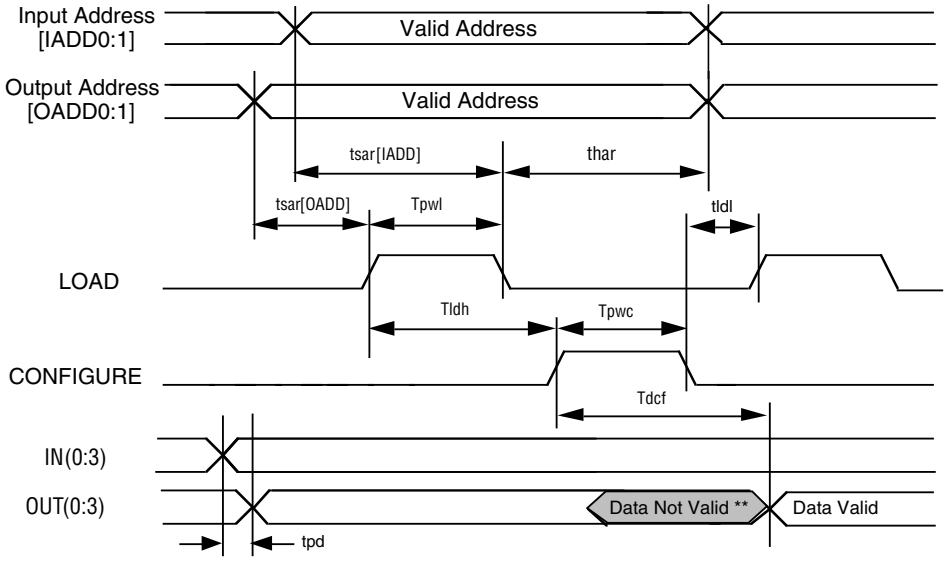
Notes (Tables 3 and 4):
1. Differential Input Peak-Peak = 2| Vin - NVin |
2. R_{LOAD} = 50 ohms to V_{TT} = V_{DD} – 2.0V.
3. Specifications apply over recommended operating ranges.

Table 5. AC Characteristics

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Maximum Data Rate/port			2.7			Gb/s
Minimum Input pulse width	(1)	T_{pw}	370	—	—	ps
Rise/Fall time 20-80%		$T_{r/f}$	—	—	150	ps
Channel Propagation Delay	(1)	T_{pd}	—	—	1.0	ns
Ch-to-Ch Prop. Delay Skew	(1)	T_{skew}		100		ps
Jitter (pk-pk)	(2)	T_{jitter}	—	25	—	ps

Notes: 1. Measured at crossing point of true and complement
2. Crossing of (On) – (NOn) measured with 2^{23} – 1 PRBS, measured over extended time.

Figure 1. Timing Diagram



** Data remains valid on outputs with unchanged configurations

Table 6. Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
t_{sar}	Address to Load Set-up time	2		ns
t_{har}	Address to Load Hold Time	2		ns
t_{pwl}	Min. Load pulse width	5		ns
t_{ldh}	Load to Configure delay	0		ns
t_{ldl}	Configure to Load delay	2		ns
t_{pwc}	Min. Configure pulse width	5		ns
t_{dcf}	Configure to Data Valid		20	ns

Table 7. TQ8004 Pin Descriptions

Signal	Type	Pin Number	Description
Control and Configuration			
CONFIGURE	TTL Input	17	Active High. Enables transfer of data from program latches to configuration latches.
LOAD	TTL Input	16	Active High. Enables program latches to accept new input address based upon which output is selected using OADD inputs. Latches address data on de-assertion.
Input Address Control			
IADD0	TTL Input	27	Input address LSB
IADD1	TTL Input	28	Input address MSB
Output Address Control			
OADD0	TTL Input	14	Output address LSB
OADD1	TTL Input	13	Output address MSB
Output Ports			
OUT0,NOUT0	DPECL Output	19,18	True and Complement Differential PECL Data Out Addressed by OADD(0:1) = 00
OUT1,NOUT1	DPECL Output	21,20	True and Complement DPECL Data Out Addressed by OADD(0:1) = 01
OUT2,NOUT2	DPECL Output	23,22	True and Complement DPECL Data Out Addressed by OADD(0:1) = 10
OUT3,NOUT3	DPECL Output	25,24	True and Complement DPECL Data Out Addressed by OADD(0:1) = 11
Input Ports			
IN0,NIN0	DPECL Input	10,11	True and Complement DPECL Data In. Addressed by IADD(O:1) = 00
IN1,NIN1	DPECL Input	8,9	True and Complement DPECL Data In Addressed by IADD(O:1) = 01
IN2,NIN2	DPECL Input	6,7	True and Complement DPECL Data In Addressed by IADD(O:1) = 10
IN3,NIN3	DPECL Input	4,5	True and Complement DPECL Data In Addressed by IADD(O:1) = 11
Power Pins			
Signal	***Description***		***Pin Number***
VTT	Input Termination Supply		2
VDD	+3.3V Power Supply		1, 15, 26, Package Down Paddle (required)
GND	Ground Supply		3, 12

Figure 2. Typical Output Eye with 2^{23}-1 PRBS data at 2.7 Gb/s

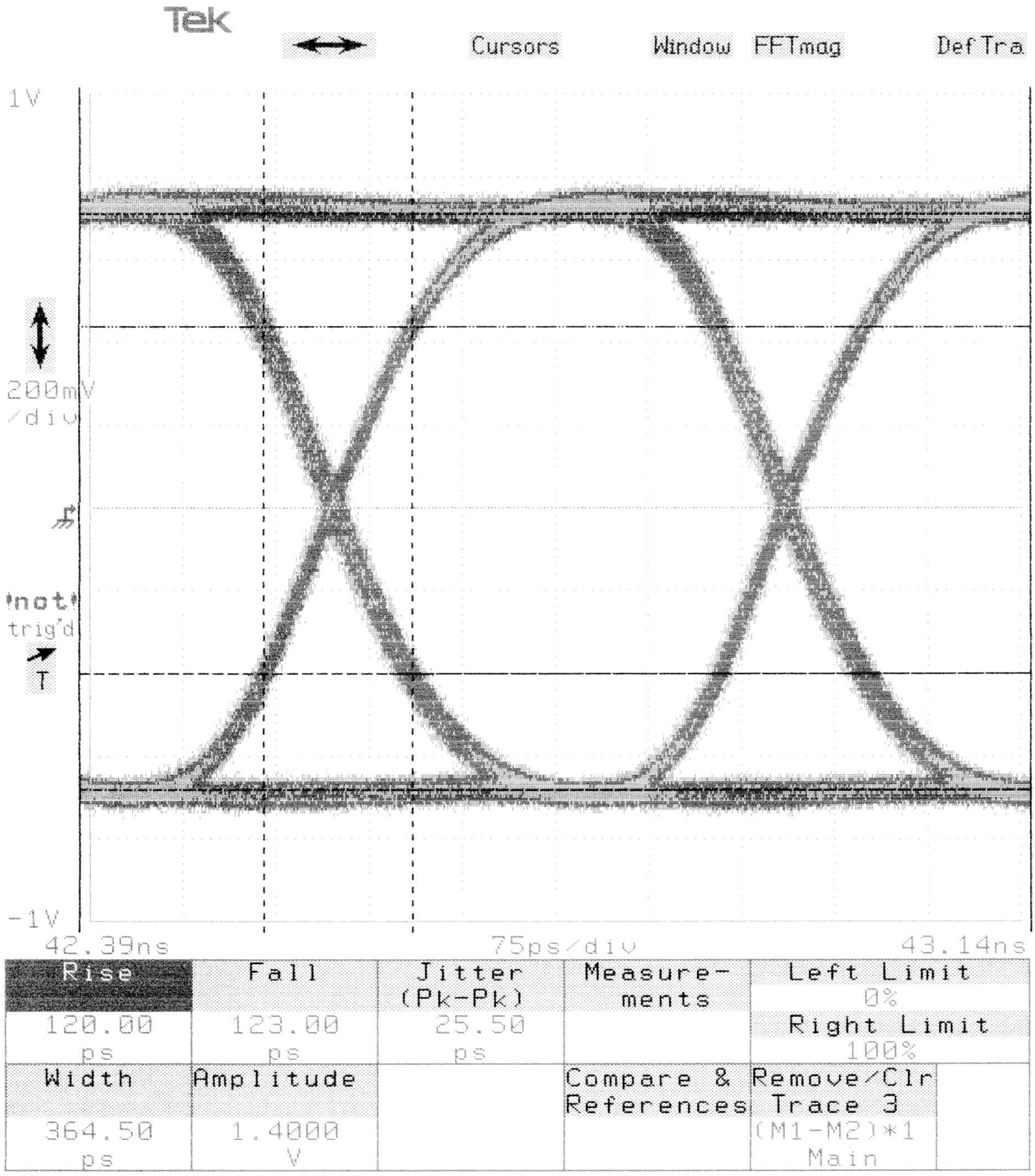
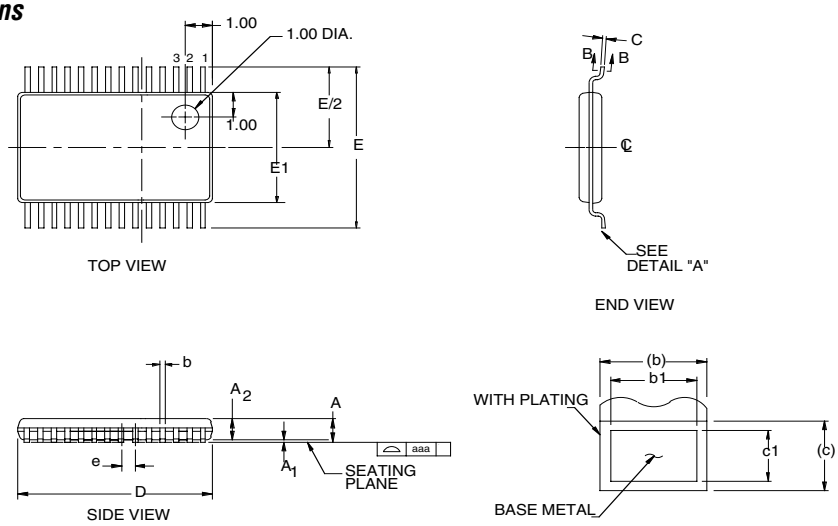


Figure 3. TSSOP Mechanical Dimensions

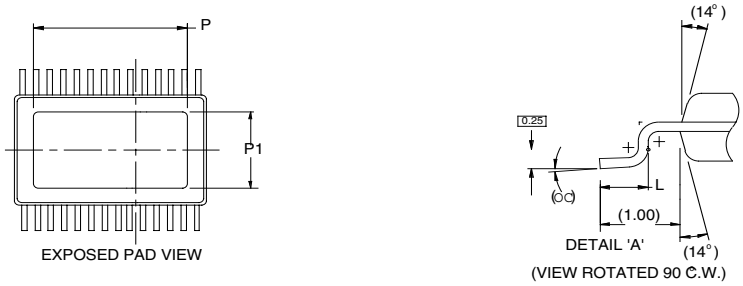
	MIN	NOM	MAX
A			1.10
A1	.0254		.1500
A2	.8500		0.95
b	.1900		.3000
b1	.1900		.2500
c	.0900		.2000
c1	.0900		.1600
D	9.6000		9.8000
E1	4.3000	4.4000	4.5000
e	.6500	.6500	.6500
E		6.4000	
L	.5000	.6000	.7000
N		28	
P		5.00	
P1	3.0000		3.0100

Note: All dimensions in millimeters (mm).



Moisture Level Rating 3 per

JEDEC Standard J-STD-020A



Ordering Information

TQ8004 *2.7Gbit/sec 4x4 Crosspoint Switch*

Additional Information

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