TriQuint SEMICONDUCTOR

WIRELESS COMMUNICATIONS DIVISION

TQ5135
DATA SHEET

3V Cellular CDMA/AMPS LNA/Mixer Receiver IC

Features

- Single +2.8V Operation
- Adjustable Gain/IP3/Current
- Low Current Operation
- Few external components
- QFN 3x3mm, 16 Pin Leadless Plastic Package
- High Input IP3
- Low Noise Figure

Product Description

The TQ5135 is an LNA-Downconverter optimized for use in the Korean, Japanese, and US CDMA Bands. The integrated LNA has the gain step function required for CDMA, and features very low NF and excellent IP3. An external resistor controls LNA bias, making LNA Idd adjustable. The integrated mixer features very high IP3 and provision for external adjustment of gain, IP3, and Idd. Because of the external LO tuning inductor, IF's in the range of 85 to 200Mhz can be used. The excellent RF performance with low current coupled with very small lead-less plastic package is ideally suited for Cellular band mobile phone.

Applications

- CDMA mobile Applications
- Cellular and AMPS mobile applications worldwide
- Wireless data applications

Electrical Specifications[1]

Parameter	Min	Typ	Max	Units
RF Frequency		881.5		MHz
Conversion Gain		25.0		dB
Noise Figure		1.9		dB
Input 3rd Order Intercept		-5.5		dBm
DC supply Current		20		mA

Note 1. Test Conditions: Vdd=+2.8V, T_C=+25C, RF=881.5MHz, RF in =-30dBm LO=966.5MHz, LO input=-4dBm, IF=85MHz

TQ5135
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Absolute Maximum Ratings

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Storage Temperature	T_{store}	-60	25	150	deg. C
Case Temperature w/bias	T_c	-40	25	85	deg. C
Supply Voltage	VDD	0	2.8	4	V
Voltage to any non supply pin		-	-	-	VDD+0.5V

Note 1: All voltages are measured with respect to GND (0V), and they are continuous.

2: Absolute maximum ratings as detailed in this table, are ratings beyond which the device's performance may be impaired and/or permanent damage may occur.

Electrical Characteristics

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
RF Frequency		832		894	MHz
IF Frequency		85		200	MHz
LO input level		-7	-4	-1	dBm
Supply voltage			2.8		V
High Gain Mode	LNA Mode = 0 V				
Conversion Gain [1,3,4]		22.0	25.0		dB
Noise Figure[1,4]			1.9	2.4	dB
Input 3rd Order Intercept[1,3,4]		-7.5	-5.5		dBm
Supply Current			20.0	23.5	mA
Bypass Mode	LNA Mode = Vsup				
Conversion Gain [1,3,4]		5.5	7.5		dB
Noise Figure[1,4]			11.0	12.0	dB
Input 3rd Order Intercept[1,3,4]		10.0	12.0		dBm
Supply Current			10.0	16.0	mA

Note 1.   Test Conditions (devices screened for Conversion Gain, Noise Figure, and IIP3 to the above limits): Vdd = +2.8V, RF = 881.5MHz, LO = 966.5MHz, IF = 85.0MHz, LO input = -4dBm, RF input = -30dBm(High Gain Mode), T_C = +25° C, unless otherwise specified.

2.   Min./Max. limits are at +25° C case temperature unless otherwise specified.

3.   Conversion Gain depends on the values of the two resistors used in the GIC circuit.

4.   Data includes image reject filter (Fujitsu P/N: F5CE-881M50-K206-W) insertion loss of 1.6dB

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Typical Electrical Characteristics – LNA only:

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
RF Frequency		832		894	MHz
High Gain Mode	LNA Mode = 0 V				
Conversion Gain [1,3]			16		dB
Noise Figure[1]			1.5		dB
Input 3rd Order Intercept[1,3]			7.0		dBm
Supply Current			9.5		mA
Bypass Mode	LNA Mode = Vsup				
Conversion Gain [1,3]			-2.5		dB
Noise Figure[1]			2.5		dB
Input 3rd Order Intercept[1,3]			32		dBm
Supply Current			0.7		mA

Note 1.   *Test Conditions: Vdd = +2.8V, RF = 881.5MHz, LO = 966.5MHz, I F= 85MHz, LO input = -4dBm, RF input = -35dBm, T_C = 25° C, unless otherwise specified.*

2.   *Min./Max. limits are at +25° C case temperature unless otherwise specified.*

3.   *Conversion Gain depends on the values of the two resistors used in the GIC circuit.*

Electrical Characteristics – Mixer only:

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
RF Frequency		832		894	MHz
IF Frequency		85		200	MHz
Conversion Gain [1,3,4]			9.0		dB
Noise Figure[1,4]			8.5		dB
Input 3rd Order Intercept[1,3,4]			10.0		dBm
Supply Current			10.0		mA

Note 1:   *Test Conditions: Vdd = +2.8V, RF = 881.5MHz, LO = 966.5MHz, I F= 85MHz, LO input = -4dBm, RF input = -15dBm, T_C = 25° C, unless otherwise specified.*

2.   *Min./Max. limits are at +25° C case temperature unless otherwise specified.*

3.   *Conversion Gain depends on the values of the two resistors used in the GIC circuit.*

4.   *Data includes image reject filter (Fujitsu P/N: F5CE-881M50-K206-W) insertion loss of 1.6dB*

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Typical Test Circuit for CDMA Cellular:

Test Conditions (Unless Otherwise Specified): Vdd=+2.8V, Tc=+25C, RF=881MHz, LO=966MHz, IF=85MHz, PRF=-30dBm, PLO=-4dBm
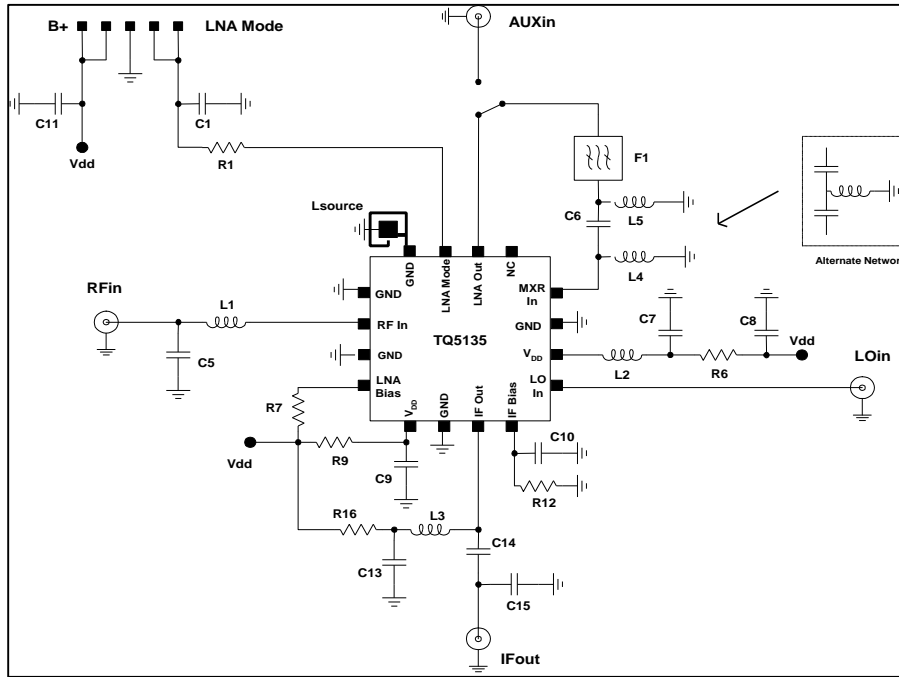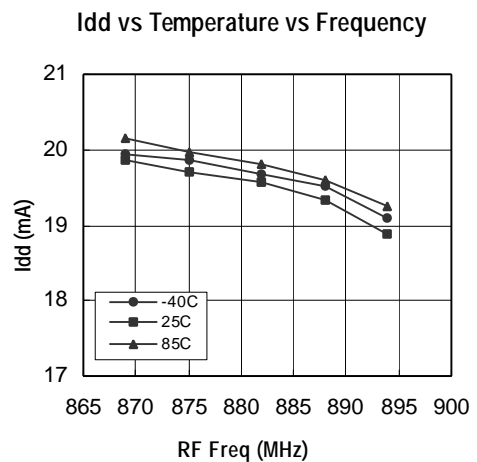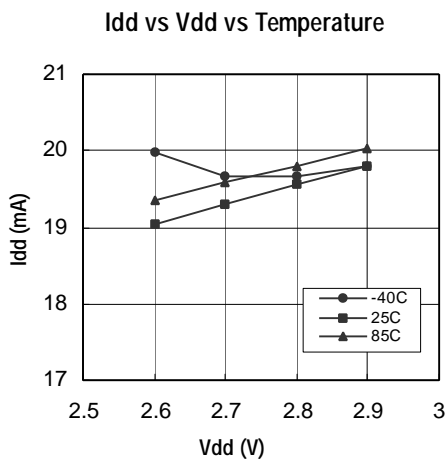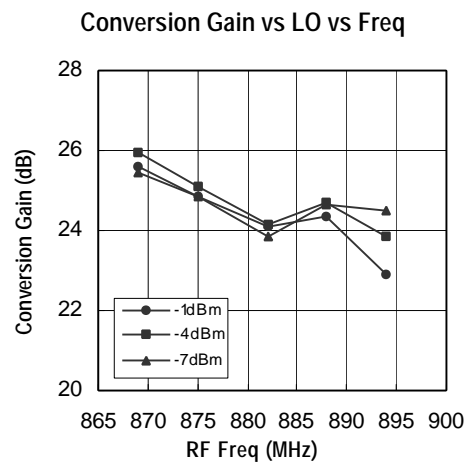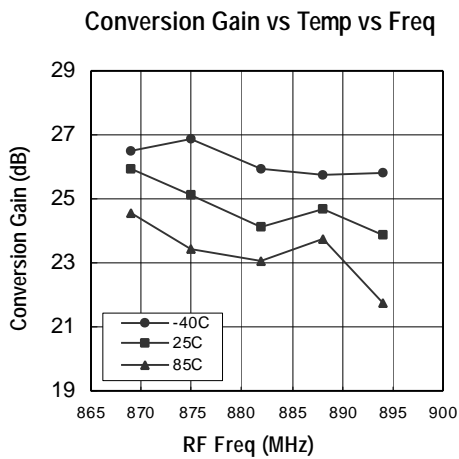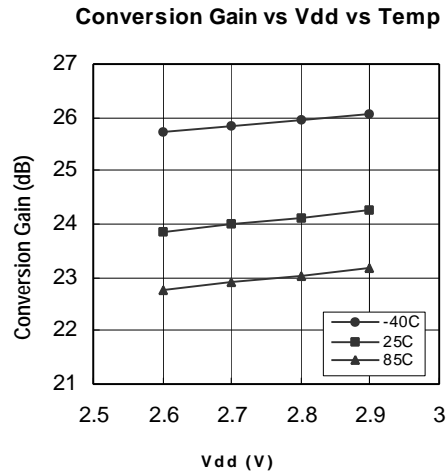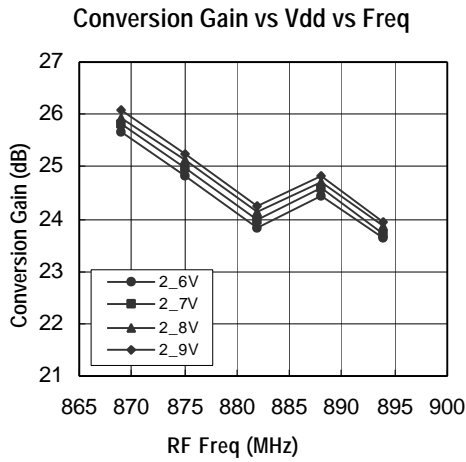

Bill of Material for TQ5135 LNA/Downconverter Mixer for GIC tuning plots

Component	Reference Designator	Part Number	Value	Size	Manufacturer
Receiver IC		TQ5135		3x3mm	TriQuint Semiconductor
Capacitor	C1, C11, C13		0.1uF	0402	
Capacitor	C5		2.7pF	0402	
Capacitor	C6		4.7pF	0402	
Capacitor	C7		22pF	0402	
Capacitor	C8, C9, C10		1000pF	0402	
Capacitor	C14		56pF	0402	
Capacitor	C15		56pF	0402	
Inductor	L1		15nH	0402	TOKO
Inductor	L2		18nH	0402	TOKO
Inductor	L3		100nH	0603	TOKO
Inductor	L4, L5		12nH	0402	TOKO
Resistor	R1, R16		3.3O	0402	
Resistor	R6		20O	0402	
Resistor	R7		4.7KO	0402	
Resistor	R9		1.8O	0402	
Resistor	R12		56O	0402	
RF Saw Filter	F1			3x3mm	SAWTEK

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CDMA Cellular Band Typical Performance – High Gain Mode

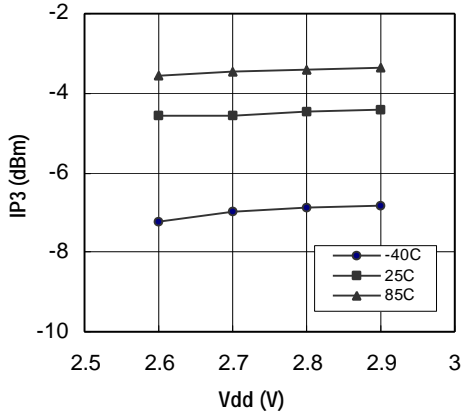*Test Conditions (Unless Otherwise Specified): Vdd=+2.8V, Tc=+25C, RF = 881.5MHz, LO = 966.5MHz, I F= 85MHz*
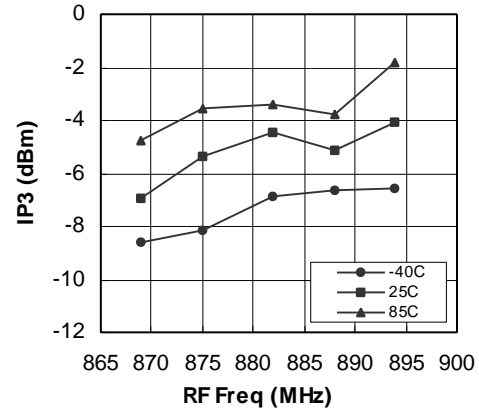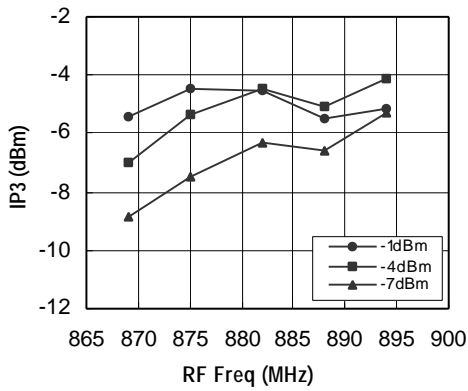
Conversion Gain vs Vdd vs Freq

Conversion Gain vs Vdd vs Temp

Conversion Gain vs Temp vs Freq

Conversion Gain vs LO vs Freq

Idd vs Vdd vs Temperature

Idd vs Temperature vs Frequency

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Input IP3 vs Vdd vs Temperature

Input IP3 vs Temp vs Freq

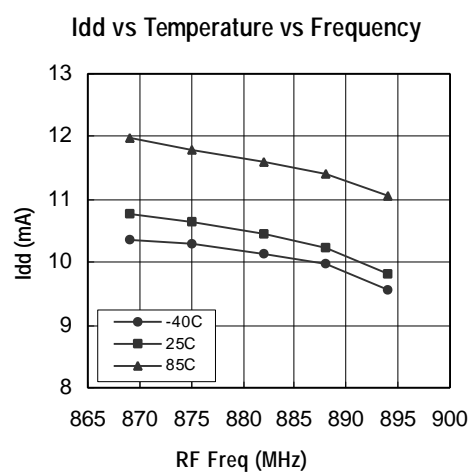## Input IP3 vs LO Drive vs Frequency

Noise Figure vs Temp vs Freq

Noise Figure vs Vdd vs Temp
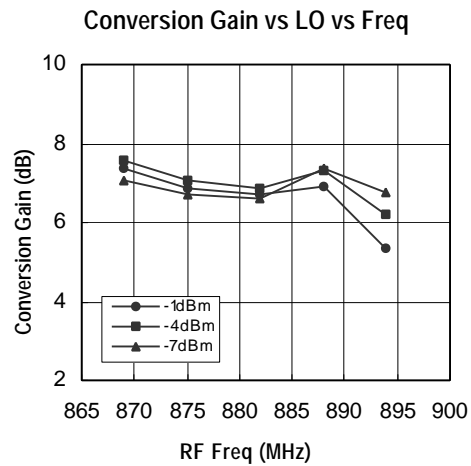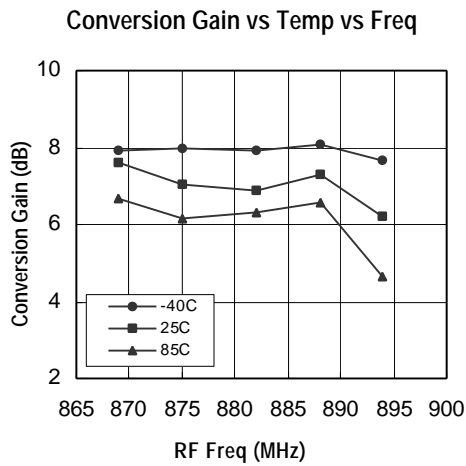
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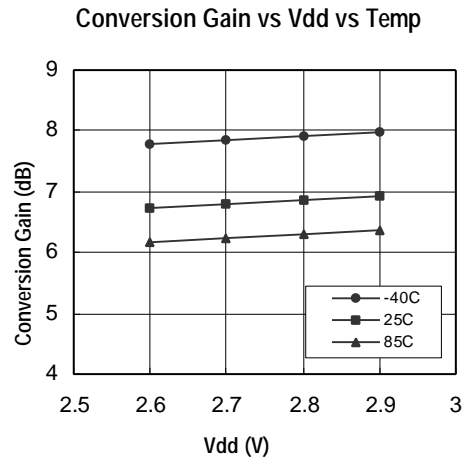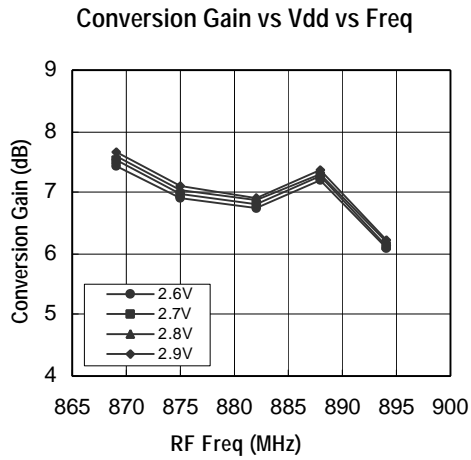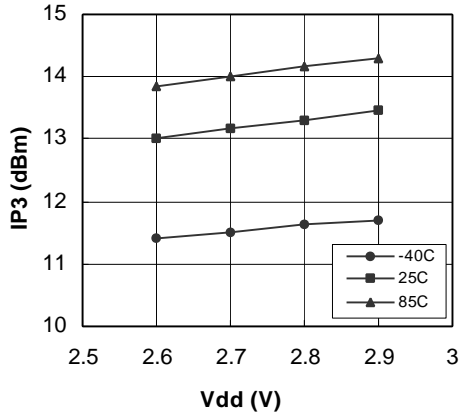
CDMA Cellular Band Typical Performance – Low Gain Mode

Test Conditions (Unless Otherwise Specified): Vdd=+2.8V, Tc=+25C, RF = 881.5MHz, LO = 966.5MHz, I F= 85MHz

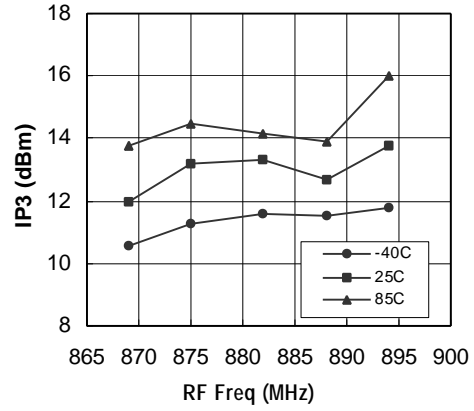**Conversion Gain vs Vdd vs Freq**
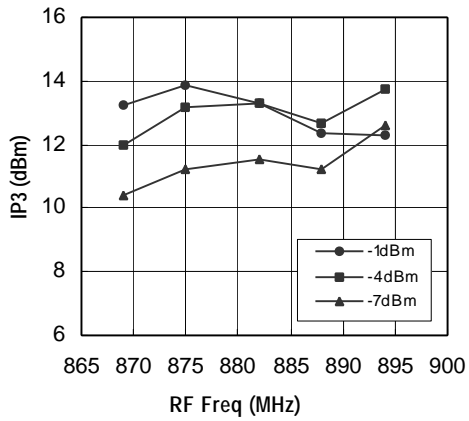

Conversion Gain vs Vdd vs Temp

Conversion Gain vs Temp vs Freq

Conversion Gain vs LO vs Freq

Idd vs Vdd vs Temperature

Idd vs Temperature vs Frequency

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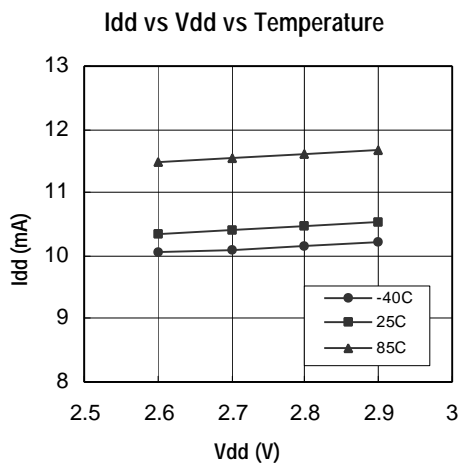
TQ5135
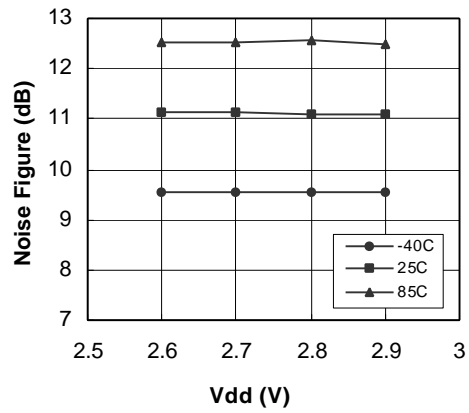## Data Sheet

Input IP3 vs Vdd vs Temperature

Input IP3 vs Temp vs Freq

Input IP3 vs LO Drive vs Frequency

Noise Figure vs Vdd vs Temperature

Noise Figure vs Temp vs Frequency

For additional information and latest specifications, see our website: www.triquint.com
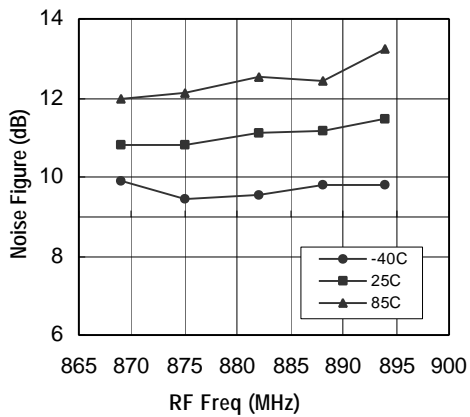
Pinout Description:

The TQ5135 is a complete front-end for a low band CDMA handset receiver. It combines a high IP3 low noise amplifier, a high intercept mixer, and an IF amplifier. The LNA uses an off-chip matching network, which connects to the input at pin 2. The amplifier was designed so that the match for maximum gain also gives very low noise figure. The LNA has two modes, high gain and bypass. Pin 15 is the input to the gain control logic, which drives the switch FETs. In the high gain mode (pin 15=low), the LNA provides around 17dB of gain. In the bypass mode (pin 15=high) it has a loss of about 2dB.

The LNA also provides several ways of setting gain and intercept in the design phase. The LNA FET source is brought out to Pin 16, where a small value of inductance to ground can be added. The inductor can be discrete or simply a small length of pc board trace. Several dB of adjustment is possible. A bias resistor on pin 4 is used to set the LNA supply current. A nominal value of 2.7kohm is recommended, but it can be increased for lower LNA Idd.

The LNA output signal is at Pin 14. It is a 50 ohm line and can be connected directly to a SAW image filter. The image filter output connects to the mixer input at Pin 12. The mixer receives its LO via a buffer which amplifies the signal from Pin 9. The drain of buffer transistor is connected to Pin 10 where it is connected to an external LO tuning inductor.

Figure 1. TQ5135 Block diagram

The IF signal from the mixer is fed to an amplifier. The IF amplifier is an open drain type with output at Pin 7. An external matching circuit is required to match the IF output to a filter. The IF amplifier also has a GIC pin (Gain-Intercept-Current). It is used to set the DC current and gain of the IF stage.

Application Information:

Half IF Spur Rejection Considerations:

The TQ5135 does not contain a balanced mixer so Half-IF spur rejection is completely set by the image filter. Thus we do not recommend using an IF that is less than 2.5 times the image filter.

Grounding:

With good layout techniques there should not be any stability problems. Poor circuit board design can result in a circuit that oscillates. Good grounding is especially important for the TQ5135 since it uses an outboard LO tuning inductor that provides one more potential ground loop path. One could use the evaluation board as an example of proper layout techniques.

It is important to position the LO tuning, GIC, and IF matching components as close to the chip as possible. If the components are far enough away they and their corresponding pc board traces can act as quarter wave resonators in the 5-10Ghz region. If both the IF and the LO paths to ground resonate at the same frequency, oscillation can result.

It is most important that the ground on the GIC bypass cap, the ground on the LO tuning bypass capacitor, and the IF shunt cap ground return back to the chip grounds with minimal inductance (Figure 2).

Also, improving the ground at the LO tuning inductor bypass cap will increase circuit Q. Thus mixer drive is improved with a resultant higher IP3. Improved ground here means minimal inductance between the chip ground pins and the other ground return points.
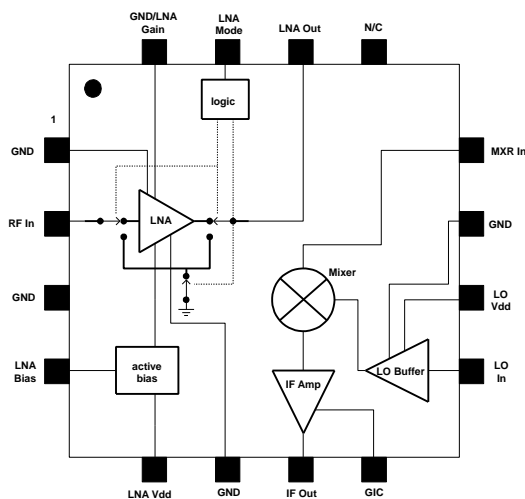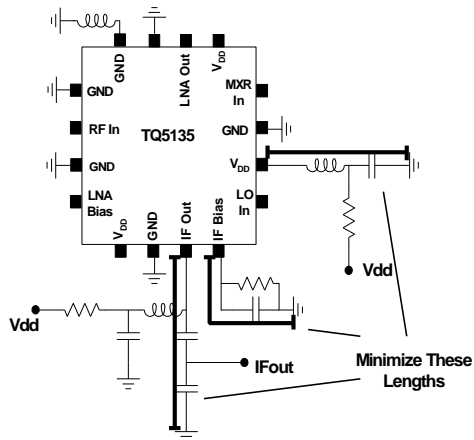
Figure 2. Critical signal Paths

Mixer – Filter Interaction:

Before attempting a new TQ5135 application, it is important to understand the nonlinear interaction between the image filter and the mixer. The device IP3 is a strong function of this interaction. For this reason it is helpful to consider the filter and mixer as one nonlinear block.

Figure 3 shows a much simplified block diagram of the LNA, image filter, and mixer. The RF signal is amplified by the LNA, passes through the image filter, and is converted down to the IF where it is amplified by the IF output FET. The quiescent current in the IF amplifier is set by the GIC network. Both the filter and the mixer terminate the RF signal with 50ohms.

However, the situation is much different with the LO signal. At the LO frequency the image filter looks like a short circuit. Some LO energy leaks out of the mixer input, bounces back off of the image filter and returns back into the mixer with some phase or delay. The delayed LO signal mixes with the normal LO to create a DC offset which is fed into the IF amplifier and changes the quiescent current. Depending on the phase of the reflected LO, the IF stage current may be higher or lower.

The DC offset also affects the passive mixer FET to some degree as well. It has been found empirically that varying the delay between the filter and mixer can have positive or negative consequences on IP3, CG, and NF. It is for this reason that an LC network is useful between the SAW and mixer input, even though the mixer input can have an adequate match at the RF frequency without any external components.
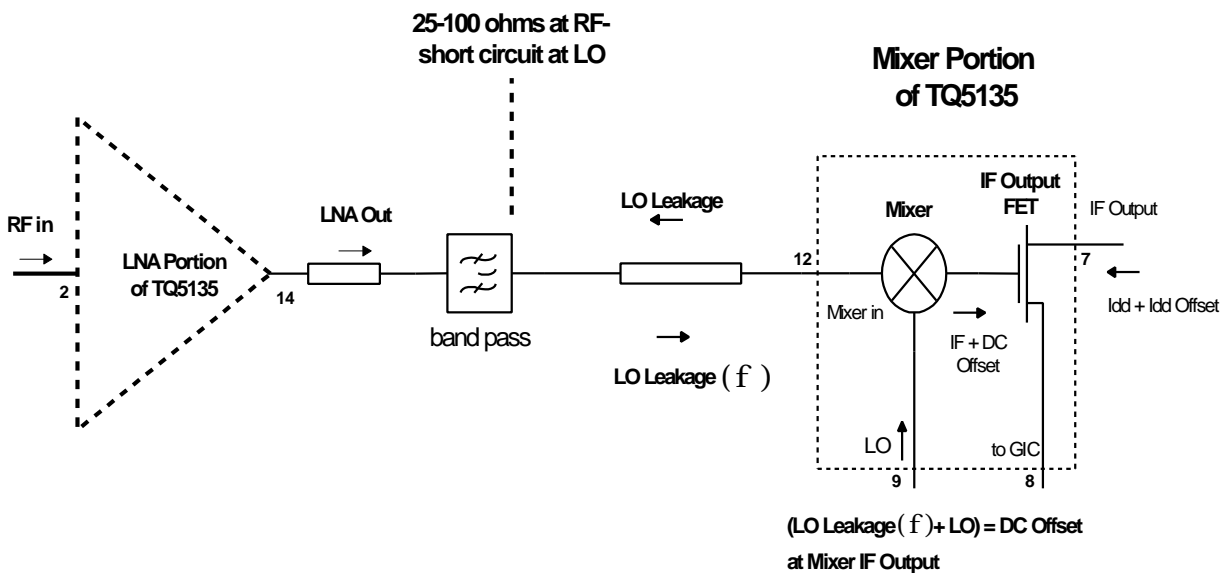

Figure 3. Non-linear filter-Mixer Interaction

LNA S-Parameters :

S-Parameters for the TQ5135 LNA taken in both the high gain and low gain modes. We have not included noise parameters since for this device Gamma-Opt is very close to the conjugate match.
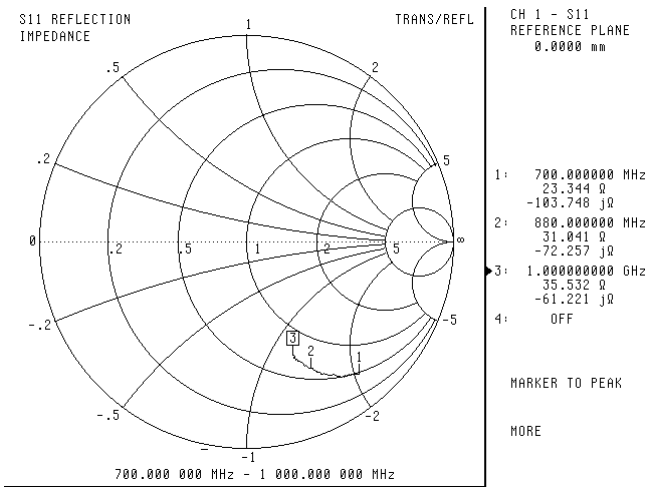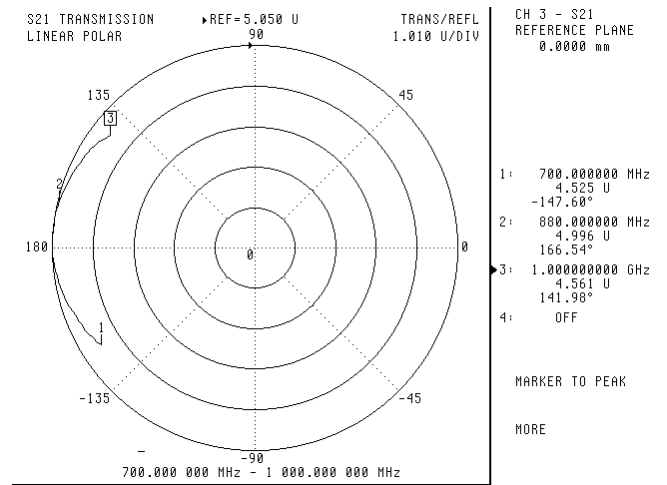

Figure 4: LNA S11 in HG Mode

Figure 6: LNA S21 in HG Mode
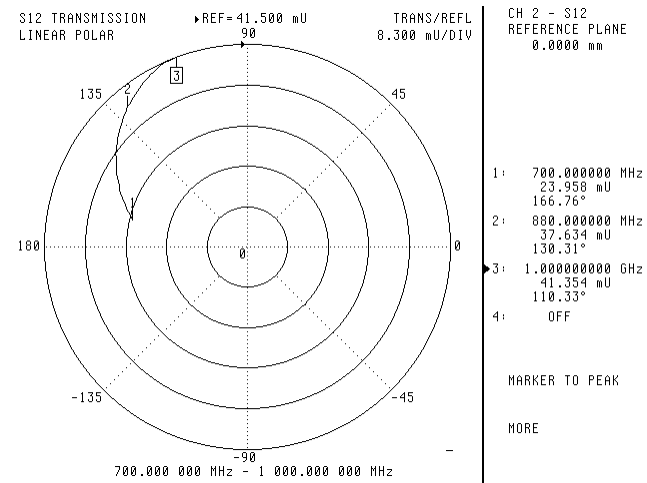

Figure 5: LNA S12 in HG Mode
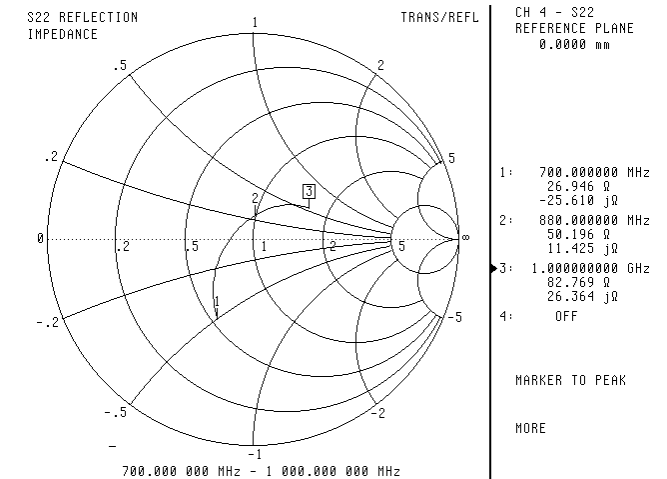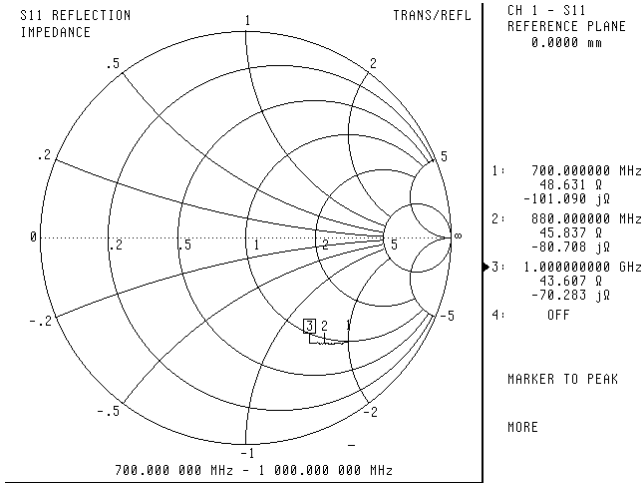

Figure 7: LNA S22 in HG Mode

Figure 8: LNA S11 in LG Mode
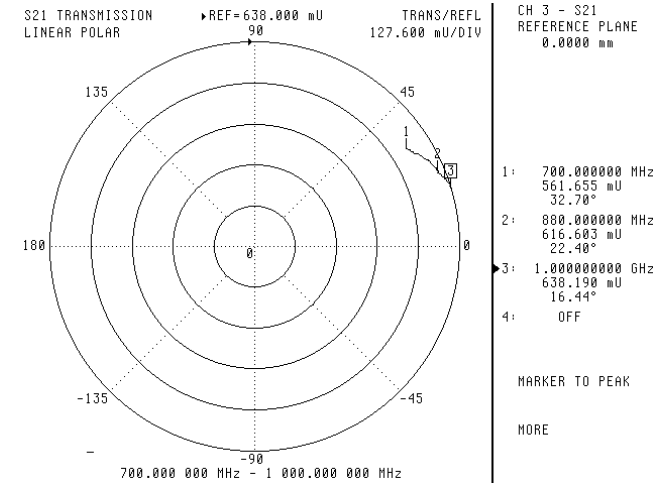
Figure 10: LNA S21 in LG Mode
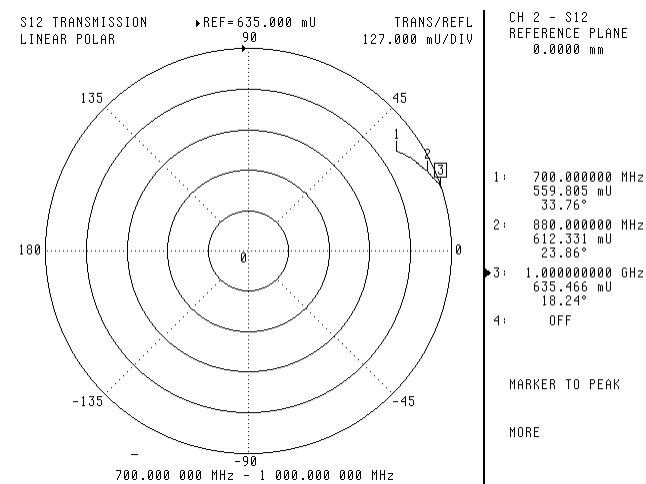
Figure 9: LNA S12 in LG Mode

Figure 11: LNA S22 in LG Mode

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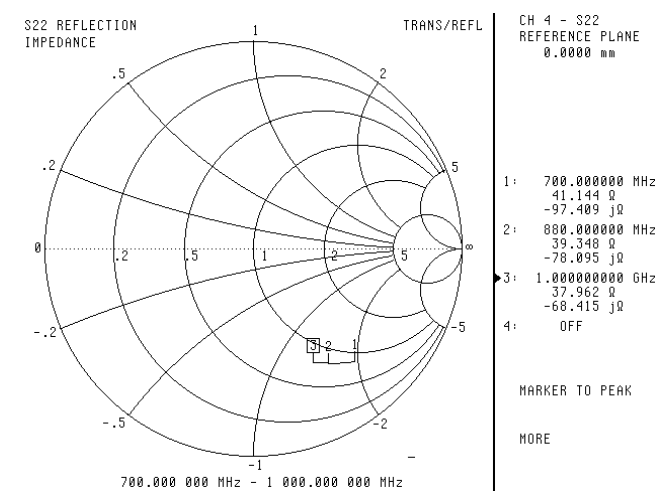## SUGGESTED STEPS FOR TQ5135 TUNING:

The following order of steps is recommended for applying the TQ5135. They are described in detail in the following sections:

Lay out board consistent with the grounding guidelines at the beginning of this note. See section 1 regarding LNA source inductor.

1. Determine the LNA bias resistor value and source inductor value

2. Determine the LNA input matching network component values. Test the LNA by itself.

3. For the mixer, experimentally determine proper LO tuning components. This step needs to be done first since all of the later tuning is affected by it.

4. Determine a tentative GIC network. It will have to be fine-tuned later, since the image filter interaction will affect device current.

5. Synthesize a tentative IF output match. It may have to be fine-tuned later, as the final GIC configuration affects IF stage current. LO is turned ON.

6. Experimentally determine a tentative mixer RF Input match. LO is turned ON. Test the filter-mixer cascade. Verify that the device has adequate IP3. If not, another RF Input matching topology can be tried.

7. Fine tune GIC components for needed Idd. LO is turned ON.

8. Check IF match to see if it still is adequate. LO is turned ON.

9. Test the device as a whole- LNA, filter, mixer

1. Determine LNA Bias Resistor Value and Source Inductor Value

For most designs we recommend an LNA bias resistor of 2.7K ohms. All of the datasheet specs assume that value of resistor. However, if LNA Idd <15mA is desired, then the resistor can be made larger. Refer to Figure 12 for graphs of LNA performance vs. bias resistor.

Please keep in mind that there are implications of reduced LNA bias that are not reflected in IP3. For example, the LNA is normally in front of the image filter so that it may need resistance to blocking or other types of distortion that are not adequately described by the IP3 figure of merit.
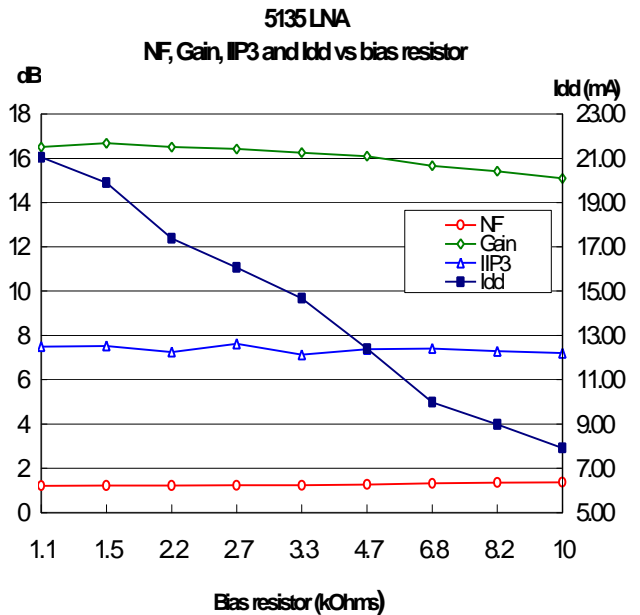

Figure 12: Gain, IIP3, Idd, and NF as a Function of Rbias

A small amount of inductance is needed from pin 16 to ground for proper degeneration of the LNA input stage. Too much inductance at this point will degrade LNA gain, while too little inductance will degrade NF at the conjugate match. Because of stray inductance on the application board layout, it is difficult to give a precise value in nH. Thus we recommend during the prototype stage to use one of the copper patterns in Figure 13.

A short can be placed across the pattern and its position varied until the desired gain is met. Then the unused copper can be removed for the final product.

2. Determine the LNA Matching Network

Matching network design for the TQ5135 LNA is much simpler than designing with discrete transistors. The TQ5135 LNA was designed so that the optimum noise match is very close to the conjugate match. Thus once a match to 50ohms is attained, only a slight adjustment to the L and C values may be needed for optimum noise figure. If the design uses 5-8mil

dielectric FR4 board, then it is likely that the component values on the evaluation board can be used for a starting point. Alternately, a network can be synthesized from the S-parameter values at the end of this note.

3. LO Buffer Tuning

The drain of the LO buffer is brought out to pin 10 where it is fed DC bias via an inductor. The inductor resonates with the internal and external parasitic capacitance associated with that pin. For maximum performance the resonance must be at or near the desired LO frequency. Figure 14 shows a properly tuned LO buffer. Notice that the LO frequency range of interest is to the left of the peak. We recommend that the LO is tuned slightly higher in frequency, so that the desired band is on the lower, more gradual side of the slope. Thus there is less change in performance versus frequency. We have also found empirically that tuning the LO slightly higher in frequency results in much better LO input and RF input matches.
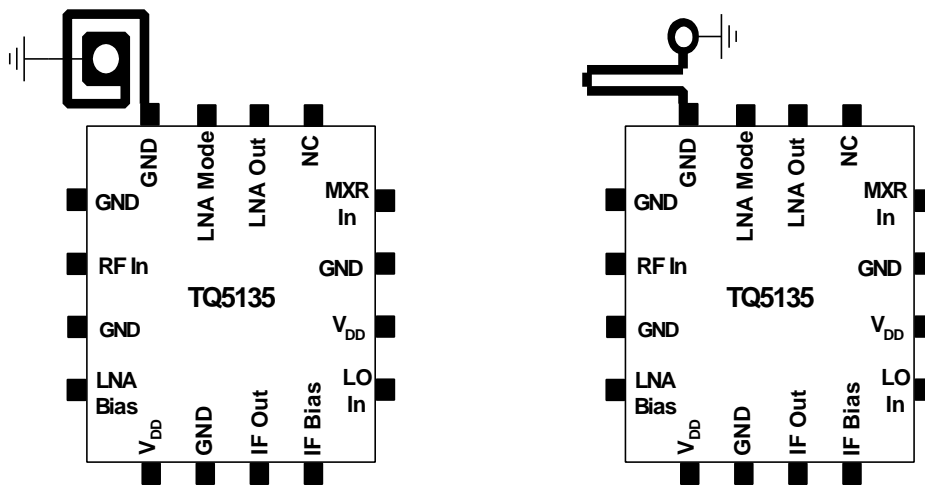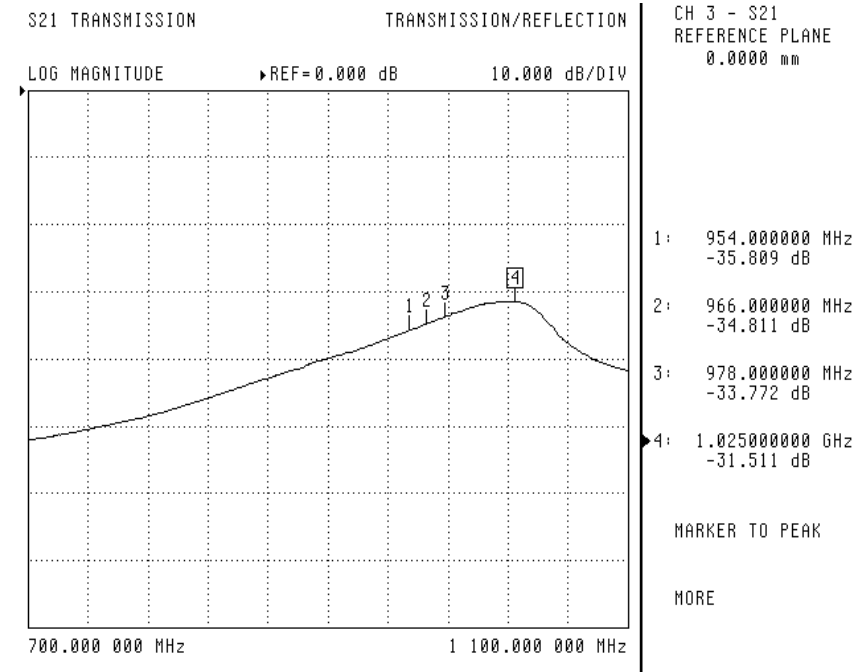

Figure 13: LNA Source Inductor Realization

Figure 14: Suggested LO Tuning Response

A first approximation to the needed inductor can be found by the following equation:

$$L = \frac{1}{C(2\pi F)^2} - 1nH \qquad where\ C=1.5pF$$

It is likely that when the design is prototyped, the needed inductance will fall between two standard inductor values. It is advised to use a slightly larger inductor and then use the bypass capacitor for fine tuning. When using this method it is important to isolate the tuning inductor/bypass cap node from the Vdd bus, since loading on the bus can affect tuning. A resistor of 3.3ohm to 20ohm has been found to work well for this purpose (R2).

Figure 14 shows the recommended test setup for tuning the TQ5135 LO buffer. A network analyzer is set to the center of the LO band +/- 300Mhz, with an output power of –4dBm. It is important to set the frequency range to be quite a bit wider than the LO band, so that the shape of the tuning curve can be seen. A two port calibration is performed and the analyzer is set to monitor S21. Port 1 of the analyzer is connected to the LO port of the TQ5135, while Port 2 is connected via cable to a short length of semi-rigid coaxial probe. The center of the probe should protrude 1 to 2 mm beyond the ground shield. The end of the probe with the exposed center conductor is held close to the LO tuning inductor.
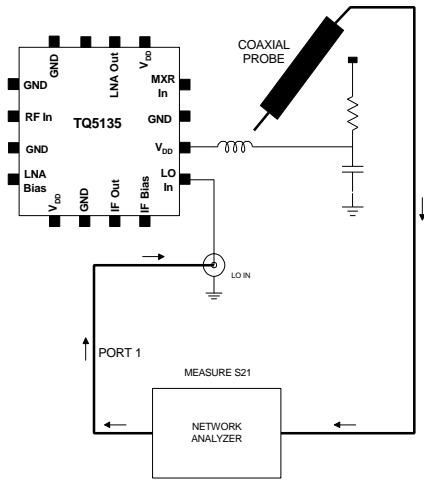
Figure 15: LO Tuning Test Setup

4. GIC Network Design

The GIC pin on the TQ5135 is connected internally to the source of the IF output stage. By adding one or two resistors and a capacitor to this pin, it is possible to vary both the IF stage AC gain, and the IF stage quiescent current. However, there is a limit to the amount of gain increase that is possible,

since there is always some package and bond wire inductance back to the die. Furthermore, although some additional IP3 performance may be gained by increasing the quiescent current, in practice it makes no sense to increase Idd beyond that which provides maximum input intercept. At some point IP3 is limited by the mixer FET, and no further increase in input intercept can be obtained by adjusting the IF stage.

There are two GIC schemes that are recommended for the TQ5135 (Figure 16). The first uses a small resistor (1.0 to 5 ohms) in series with a bypass capacitor to set the AC gain. The IF stage current is then set by the larger resistor (40 to 80 ohms) that connects directly from the GIC pin to ground. The small degeneration resistor lowers the IF stage gain.

The second scheme, which is recommended for maximum gain, uses a resistor in parallel with capacitor. The resistor sets the DC current, while the capacitor bypasses it at the IF frequency. For highest gain, place the capacitor as close to Pin 7 as possible. Try to avoid capacitors which are self-resonant at the IF frequency.

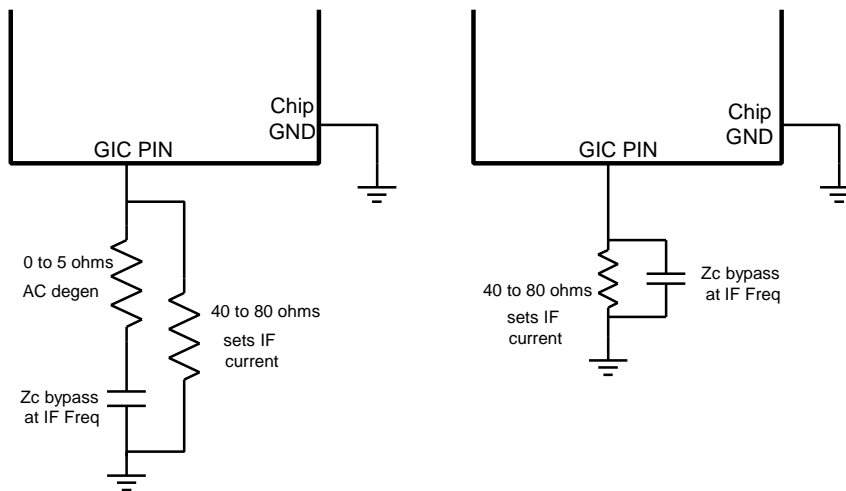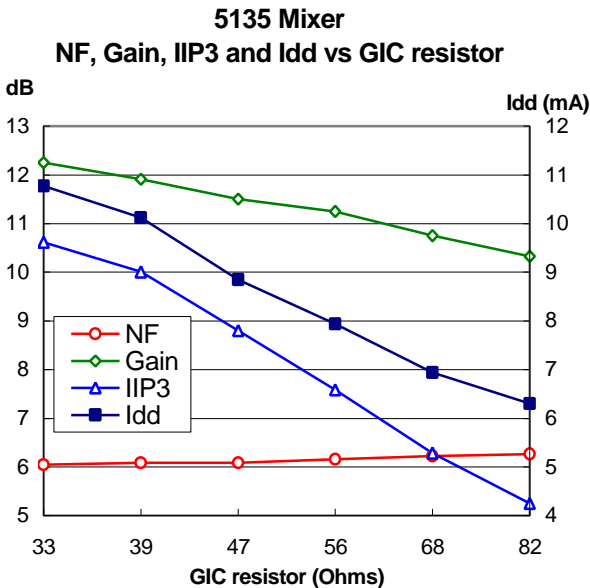Here is an approximate equation for Rgic as a function of IF stage Idd: $\quad Rgic \sim 0.6 / IDD\_IF$

Figure 16: GIC Pin Networks

For additional information and latest specifications, see our website: www.triquint.com

5135 Mixer
NF, Gain, IIP3 and Idd vs GIC resistor

Figure 17: Mixer Performance as a Function of Rgic

5. IF Match Design

The Mixer IF output (Pin 7) is an "open-drain" configuration, allowing for flexibility in efficient matching to various filter types and at various IF frequencies. An optimum lumped-element-matching network must be designed for maximum TQ5135 conversion gain and minimum matching network loss.

When designing the IF output matching circuit, one has to consider the output impedance, which will vary somewhat depending on the quiescent current and the LO drive. The IF frequency can be tuned from 45 to 400 MHz by varying component values of the IF output matching circuit. The IF output pin also provides the DC bias for the output FET.

In the user's application, the IF output is most commonly connected to a narrow band SAW or crystal filter with impedance from 500 -1000Ω with 1 - 2 pF of capacitance. A conjugate match to a higher filter impedance is generally less sensitive than matching to 50Ω. When verifying or adjusting the matching circuit on the prototype circuit board, the LO drive should be injected at the nominal power level (-4 dBm), since the LO level does have an impact on the IF port impedance.

There are several networks that can be used to properly match the IF port to the SAW or crystal IF filter. The IF FET bias is applied through the IF output Pin 7, so the matching circuit topology must contain either a RF choke or shunt inductor.

For purposes of 50 ohm evaluation, the shunt L, series C, shunt C circuit shown in Figure 18 is the simplest and requires the fewest components. DC current can be easily injected through the shunt inductor and the series C provides a DC block, if needed. The shunt C, in particular can be used to improve the return loss and to reduce the LO leakage. The circuit is used on our evaluation board.

For matching into a filter, the circuit of Figure 19 works well. The network provides the needed impedance transformation with a lower loaded Q using reasonable inductor values. Thus matching circuit loss is minimized. The ratio between (L1+L2) and L2 is proportional to the square root of the impedances to be matched, Z1 and Z2. The sum of L1 and L2 must be chosen so that the total inductance resonates with the SAW input capacitance. If this resonant frequency is much higher than the IF frequency, then Copt can be added to lower it. Please note that because of parasitic capacitance and the discrete values of commercial inductors, the formulas of Figure 15 only serve as a starting point for experimentation.

In order to minimize loss, any inductors used should have high Q. Typically 0805 size inductors perform better than the 0603 size. If 0603 inductors must be used for space considerations, make certain to use High-Q types. It is possible to introduce 3dB of additional loss by using low Q inductors. Additionally, it is recommended to place the IF filter very close to the TQ5135. If the two are far apart a transmission line will be needed between them. In that case two matching networks will be needed, one to match down to 50ohms and one to match back up to 1000ohms. Twice the loss can be expected for such a scheme.

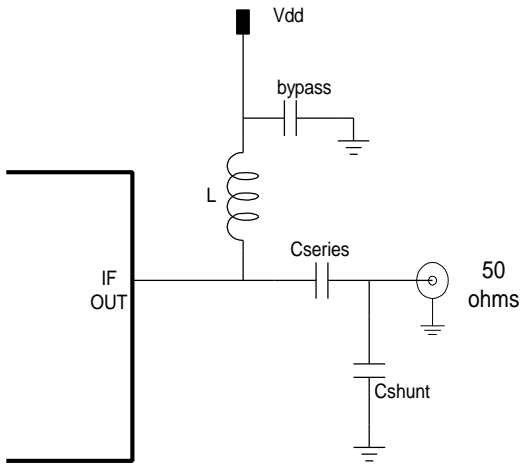**Figure 18: IF Output Match to 50 ohms**

$$L_1 \cong L_2 \sqrt{\frac{Z_2}{Z_1}} - L_2 \qquad\qquad \frac{1}{4p^2 F_{IF}^2 (L_1 + L_2)} \leq C_{SAW}$$
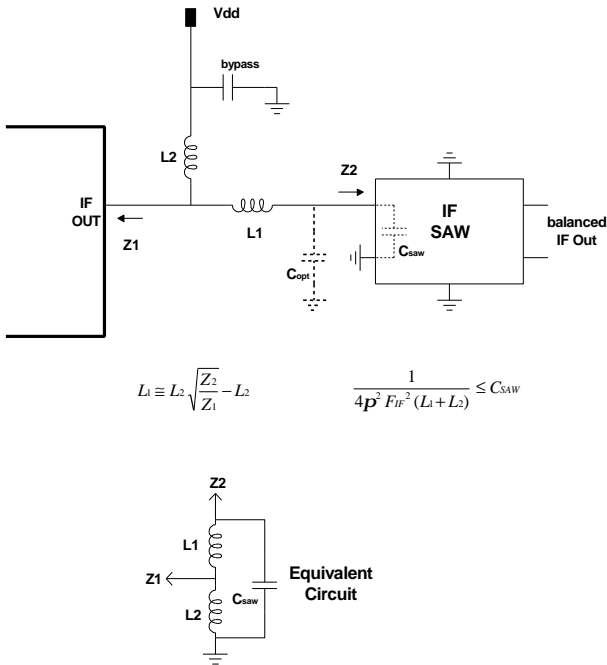

Figure 19: IF Match to a SAW Filter

6. Mixer RF Input Matching Network:

Although the TQ5135 can present <2:1 SWR to the SAW filter without a matching circuit, it is still recommended to use an inter-stage network. We have found that the Mixer-Filter interaction discussed earlier can result in degraded OIP3 at higher LO power levels with no network. Probably more time will be needed for this phase of the design than for any other, since it involves a process of trial-and-error.

It has been found experimentally that maximum IP3 for the TQ5135 evaluation board occurs when the mixer input sees a high impedance at the LO frequency. Since the SAW filter looks like a short circuit at the LO frequency, the network simply needs to add the correct amount of delay to rotate the reflection coefficient around the Smith chart to near "open circuit". Either the circuit of Figure 20-A or 20-B will accomplish this. On the evaluation board, we have found network values that will accomplish this with no degradation at the RF frequency.

Depending upon board layout and LO buffer tuning, it is possible for the mixer RF input to have a poor match. In that case, the circuit of Figure 20-C should be used. The matching and delay can be accomplished with two components.

In either case, it is important that the SAW filter see a 2:1 SWR at the RF frequencies. Otherwise there will be excessive ripple across the band.
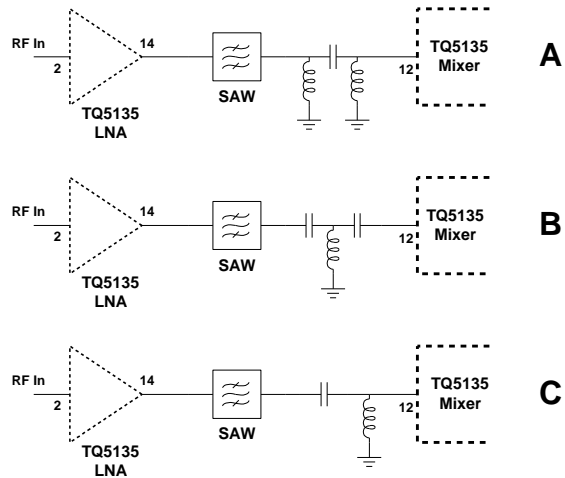

Figure 20: SAW-Mixer Input Networks

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7. Redo GIC Components:

After obtaining the optimum network between the SAW and Mixer RF input, most likely Idd will have changed slightly. Determine a new GIC resistor to bring Idd to the desired value.

8.   Double Check IF Match

After any change which affects IF stage current it is important to recheck the IF output match. This is especially true when matching down to 50ohms, since the match is more sensitive. A match to a 1000ohm filter will not be as sensitive. The LO must be turned ON during the test.

9. Test the TQ5135 Cascade:

Finally after the LNA and Mixer are properly tuned the device performance as a whole should be measured.

### AMPS Mode Application with External Switching:

The TQ5135 is a single IF output low-band CDMA receiver. Because it uses a straightforward design it achieves very high performance for a device drawing 20-25mA.

However, it is possible to add dual IF output (e.g. CDMA/AMPS) capability externally to the device using an inexpensive switch which allows switching between two different IF filters. More information can be found from separate application note.

Package Pinout:
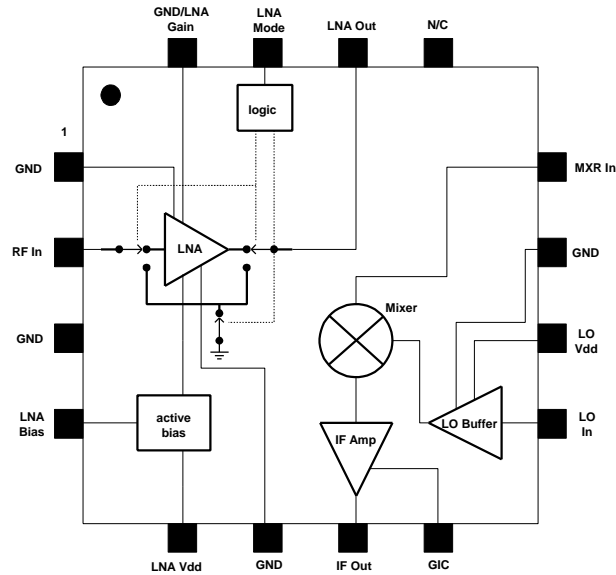
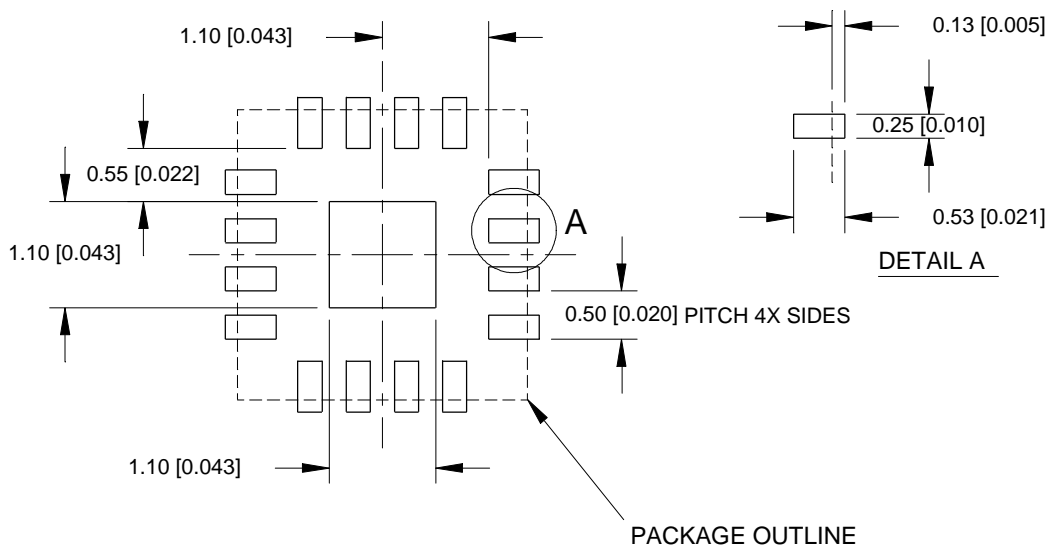*Pin Descriptions:*

Pin #	Pin Name	Description and Usage
1	LNA GND2	Ground connection. Connect as closely as possible to ground or to package paddle ground.
2	LNA IN	Connected to external RF input matching network. Interface is DC blocked.
3	Not Connected	Open connection. No connection is necessary.
4	LNA BIAS	Connected to external LNA bias resistor.
5	LNA VDD	Connected to external LNA supply voltage and RF bypass capacitor. RF bypass capacitor should be as close as possible to IC.
6	LNA GND1	Ground connection. Connect as closely as possible to ground or to package paddle ground.
7	IF	Connected to external IF matching network and IF supply voltage.
8	IF BIAS	Connected to external IF source degeneration resistor and RF bypass capacitor.
9	LO IN	Connected to LO input signal. Interface is DC blocked.
10	LO VDD	Connected to external series LC network for LO drain tuning. Network should be as close to IC as possible with good grounding of capacitor.
11	LO GND	Ground connection. Connect as closely as possible to ground or to package paddle ground.
12	MXR IN	Connected to external mixer matching network. Connect image reject filter as closely to this pin as possible (~0.1in). Interface is DC blocked.
13	Not Connected	Open connection. No connection is necessary.
14	LNA OUT	Connected to external image reject filter. Interface is DC blocked.
15	LNA MODE	Connected to external mode control signal.
16	LNA SOURCE	Connected to LNA's external source degeneration inductance (realized with PCB trace). Inductance can vary between 0 and 1 nH.
Paddle	GND	Ground connection. It is very important to place multiple via holes under the paddle. Provides RF grounding for the part.

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Recommended PC board Layout to Accept 16 Pin Lead-less Plastic Package:

1.10 [0.043]

0.13 [0.005]

0.55 [0.022]

0.25 [0.010]

1.10 [0.043]

0.53 [0.021]

A

DETAIL A

0.50 [0.020] PITCH 4X SIDES

1.10 [0.043]

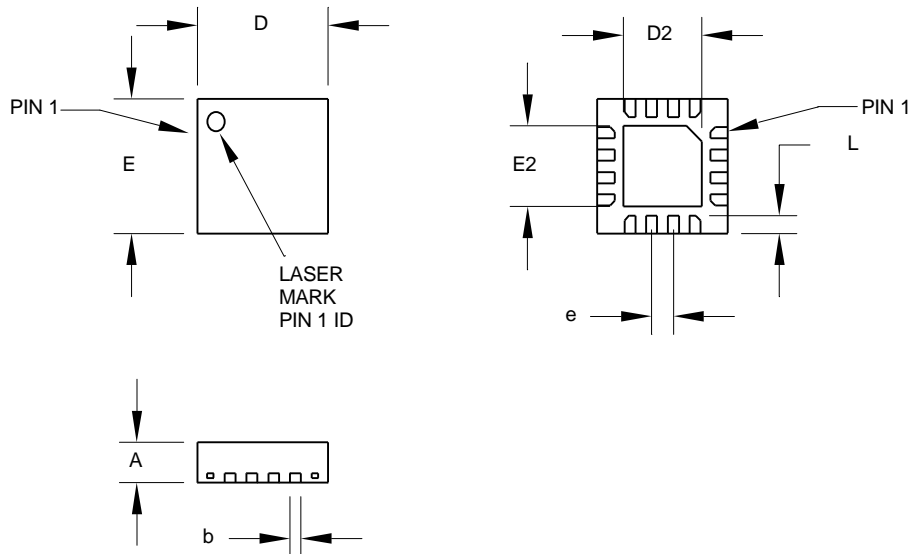PACKAGE OUTLINE

LEAD-LESS 3x3-16 PCB FOOTPRINT

NOTES:
1. ONLY GROUND SIGNAL TRACES ARE ALLOWED DIRECTLY UNDER THE PACKAGE.
2. PRIMARY DIMENSIONS ARE IN MILLIMETERS, ALTERNATE DIMENSIONS ARE IN INCHES.

Package Type: QFN 3x3-16 Lead-less Plastic Package

JEDEC DESIGNATION	DESCRIPTION	METRIC	ENGLISH	Notes
A	OVERALL HEIGHT	0.90 +/-.10 mm	.035 +/-.004 in	1
b	TERMINAL WIDTH	.250 +/-.025 mm	.010 +/-.001 in	1
D	PACKAGE LENGTH	3.00 mm BSC	.118 in	1
D2	EXOPSED PAD LENGTH	1.80 +/-.15 mm	.071 +/-.006 in	1
e	TERMINAL PITCH	.50 mm BSC	.020 in	1
E	PACKAGE WIDTH	3.00 mm BSC	.118 in	1
E2	EXPOSED PAD WIDTH	1.80 +/-.05 mm	.071 +/-.002 in	1
L	TERMINAL LENGTH	.40 +/-.05 mm	.016 +/-.002 in	1

Notes:
1. Primary dimensions are in metric millimeters. The English equivalents are calculated and subject to rounding error.

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info_wireless@tqs.com **Fax: (503) 615-8902**

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