ThunderLAN™ TNETE110PM PCI ETHERNET™ CONTROLLER SINGLE-CHIP 10 BASE-T

SPWS029 – SEPTEMBER 1996

ADVANCE INFORMATION

- Single-Chip Ethernet™ Adapter for the Peripheral Component Interconnect (PCI) Local Bus
  - 32-Bit PCI† Glueless Host Interface
  - Compliant With PCI Local-Bus Specification (Revision 2.1)
  - 33-MHz Operation
  - 3-V or 5-V I/O Operation
  - Adaptive Performance Optimization™ (APO) for Highest Available PCI Bandwidth
  - High-Performance Bus Master Architecture With Byte-Aligning Direct Memory Access (DMA) Controller for Low Host CPU and Bus Utilization
  - Plug-and-Play Compatible
- Supports 32-Bit Data Streaming on PCI Bus
  - Time Division Multiplexed SRAM
  - 2-Gbps Internal Bandwidth
- Driver Compatible With All Previous ThunderLAN Components
- Switched-Ethernet Compatible
- Full-Duplex Compatible
  - Independent Transmit and Receive Channels
  - Two Transmit Channels for Demand Priority
- No On-Board Memory Required
- Auto-Negotiation (N-Way) Compatible
- Supports the Card Bus CIS Pointer Register
- Early-Receive-Interrupt Count Register
- Hardware Statistics Registers for Management-Information Base (MIB)
- Integrated 10 Base-T, and 10 Base-5 Attachment Unit Interface (AUI) Physical Layer Interface
  - Single-Chip IEEE 802.3 and Blue Book Ethernet-Compliant Solution
  - DSP-Based Digital Phase-Locked Loop
  - Smart Squelch Allows for Transparent Link Testing
  - Transmission Waveshaping
  - Autopolarity (Reverse Polarity Correction)
  - External/Internal Loopback Including Twisted Pair and AUI
  - 10 Base-2 Supported Via AUI Interface
- Magic Packet™ Remote Wake-Up Scheme
- Microsoft™ Advanced Power Management
  - PCI Specification Compatible for Low Power/Sleep Mode
  - Advanced Configuration and Power Interface (ACPI)
- Low-Power CMOS Technology
  - Green PC Compatible
- EEPROM Interface Supports Jumperless Design and Autoconfiguration
- DMTF (Desktop Management Task Force) Compatible
- IEEE Standard 1149.1‡ Test-Access Port (JTAG)
- 144-Pin Thin Quad Flat Packages and Quad Flat Packages (PCM and PGE Suffix)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† The PCI Local-Bus Specification, Revision 2.1 should be used as a reference with this document.
‡ IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
ThunderLAN and Adaptive Performance Optimization are trademarks of Texas Instruments Incorporated.
Ethernet is a trademark of Xerox Corporation.
Microsoft is a trademark of Microsoft Corporation.
Magic Packet is a trademark of Advanced Micro Devices Corporation.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

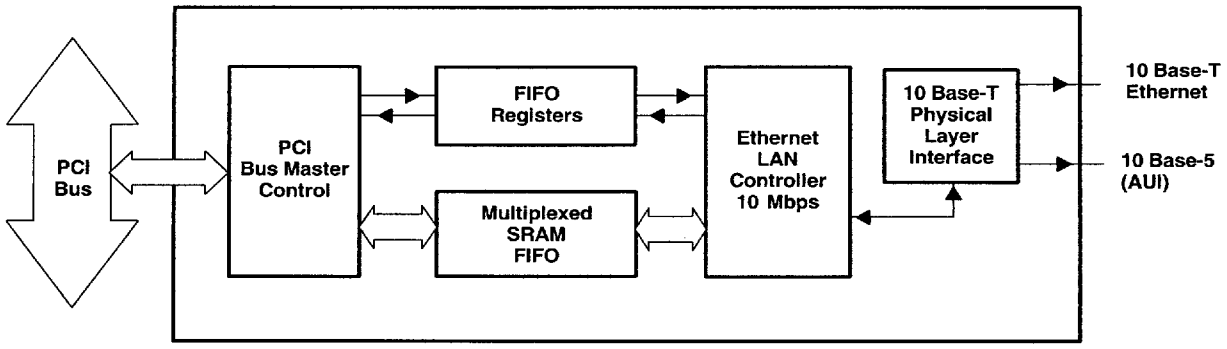


Figure 1. ThunderLAN Architecture

description

ThunderLAN is a high-speed networking architecture that provides a complete PCI-to-10 Base-T/AUI Ethernet solution. The TNETE110PM, one implementation of the ThunderLAN architecture (see Figure 1), is an intelligent-protocol network interface. The ThunderLAN SRAM FIFO-based architecture eliminates the need for external memory and offers a single-chip glueless PCI-to-10 Base-T/AUI (IEEE 802.3) solution with an on-board physical layer interface.

The glueless PCI interface supports 32-bit streaming, operates at speeds up to 33 MHz, and is capable of internal data-transfer rates up to 2 Gbps, taking full advantage of all available PCI bandwidth. The TNETE110PM offers jumperless autoconfiguration using PCI configuration read/write cycles. Customizable configuration registers, which can be autoloaded from an external serial EEPROM, allow designers of TNETE110PM-based systems to give their systems a unique identification code. The TNETE110PM PCI interface, developed in conjunction with other leaders in the semiconductor and computer industries, has been vigorously tested on multiple platforms to ensure compatibility across a wide array of available PCI products. In addition, the ThunderLAN drivers and ThunderLAN architecture use TI's patented Adaptive Performance Optimization (APO) technology to adjust critical parameters for minimum latency dynamically, minimum host CPU utilization, and maximum system performance. This technology ensures that the maximum capabilities of the PCI interface are used by automatically tuning the adapter to the specific system in which it is operating.

An intelligent protocol handler (PH) implements the serial protocols of the network. The PH is designed for minimum overhead related to multiple protocols, using common state machines to implement 95% of the total protocol handler. On transmit, the PH serializes data, adds framing and cyclic redundancy check (CRC) fields, and interfaces to the network physical layer (PHY) chip. On receive, it provides address recognition, CRC and error-checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular-buffer FIFOs in the FIFO SRAM.

Compliant with IEEE Standard 1149.1, the TNETE110PM provides a five-pin test-access port that is used for boundary-scan testing.

The TNETE110PM is available in a 144-pin thin quad flat package (TQFP) and quad flat package (QFP).

differences between TNETE110A and TNETE110PM

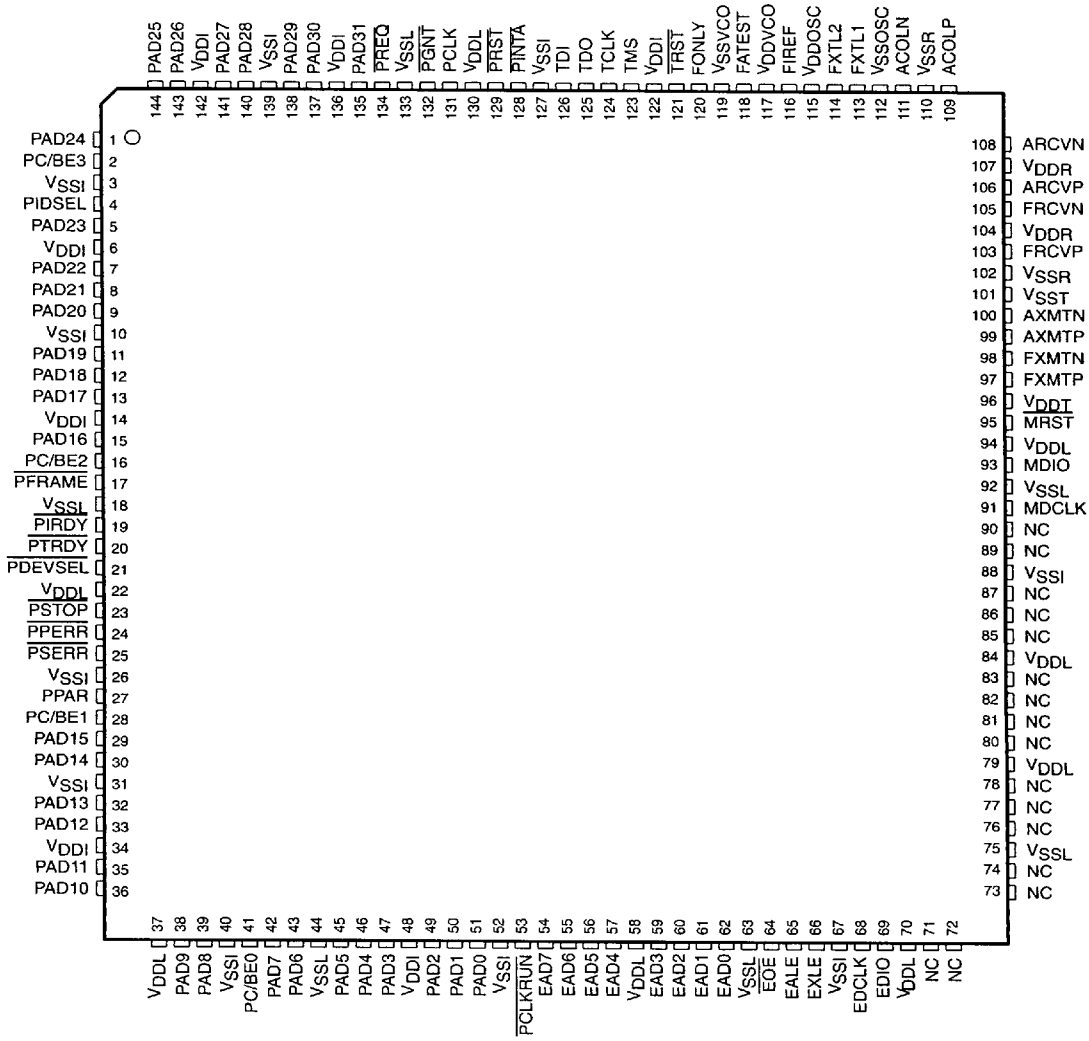
The TNETE110PM implements additional power management features such as Magic Packet and PCI specification 2.1 compatibility for low power/sleep mode, advanced configuration and power interface (ACPI).

ADVANCE INFORMATION

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

pin assignments

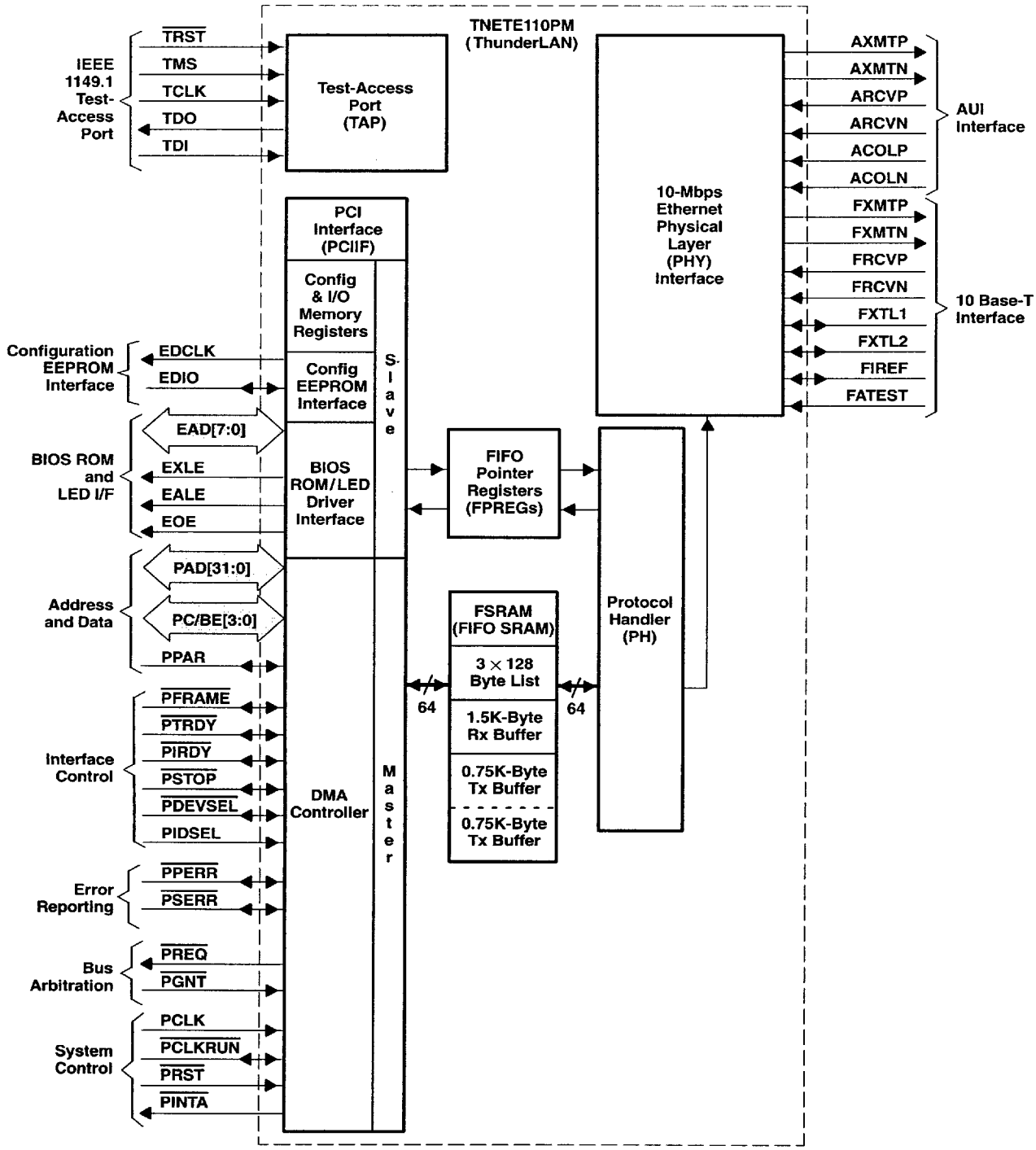
PCM and PGE PACKAGES
(TOP VIEW)



ADVANCE INFORMATION

ADVANCE INFORMATION

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

Pin Functions

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
TEST PORT			
TCLK	124	I	Test clock. TCLK is used to clock state information and test data into and out of the device during operation of the test port.
TDI	126	I	Test data input. TDI is used to shift test data and test instructions serially into the device during operation of the test port.
TDO	125	O	Test data output. TDO is used to shift test data and test instructions serially out of the device during operation of the test port.
TMS	123	I	Test mode select. TMS is used to control the state of the test port controller within TNETE110PM.
$\overline{\text{TRST}}$	121	I	Test reset. $\overline{\text{TRST}}$ is used for asynchronous reset of the test port controller.
PCI INTERFACE			
PAD31	135	I/O	PCI address/data bus. Byte 3 (most significant) of the PCI address/data bus
PAD30	137		
PAD29	138		
PAD28	140		
PAD27	141		
PAD26	143		
PAD25	144		
PAD24	1		
PAD23	5	I/O	PCI address/data bus. Byte 2 of the PCI address/data bus
PAD22	7		
PAD21	8		
PAD20	9		
PAD19	11		
PAD18	12		
PAD17	13		
PAD16	15		
PAD15	29	I/O	PCI address/data bus. Byte 1 of the PCI address/data bus
PAD14	30		
PAD13	32		
PAD12	33		
PAD11	35		
PAD10	36		
PAD9	38		
PAD8	39		

† I = input, O = output, I/O = 3-state input/output

ADVANCE INFORMATION

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
			PCI INTERFACE (CONTINUED)
PAD7	42	I/O	PCI address/data bus. Byte 0 (least significant) of the PCI address/data bus
PAD6	43		
PAD5	45		
PAD4	46		
PAD3	47		
PAD2	49		
PAD1	50		
PAD0	51		
PCLK	131	I	PCI clock. PCLK is the clock reference for all PCI bus operations. All other PCI pins except $\overline{\text{PRST}}$ and $\overline{\text{PINTA}}$ are sampled on the rising edge of PCLK. All PCI bus timing parameters are defined with respect to this edge.
$\overline{\text{PCLKRUN}}$	53	I/O‡	Clock run control (power-down-enable configuration). The $\overline{\text{PCLKRUN}}$ pin should be connected to the $\overline{\text{PRST}}$ signal for the system. This reset is generated by the V_{DDI} supply and, therefore, is used to put the TNETE110PM into D3off mode when SOPD = 1. When the $\overline{\text{PCLKRUN}}$ pin is asserted low, the TNETE110PM performs the following internal functions: – Disables PCLK during sleep state – Puts all PCI outputs in high-impedance mode asynchronously – Disables $\overline{\text{PFRAME}}$ to ensure that the TNETE110PM is signaled as though it is doing a PCI I/O cycle – Resets all TNETE110PM internal state machines – Disables all interrupts – Sets PowerState = 11 b (only if SOPD = 1) – Stops the transmitter and receiver (destructive) Note: Ten PCLK cycles are required for the TNETE110PM to terminate PCI operations and reset all state machines after $\overline{\text{PCLKRUN}}$ goes low. Clock run control (clock-run-enable configuration). The $\overline{\text{PCLKRUN}}$ pin should be connected to the $\overline{\text{PCLKRUN}}$ signal of the system. $\overline{\text{PCLKRUN}}$ is the active-low PCI clock request/grant signal that allows the TNETE110PM to indicate when an active PCI clock is required (this is an open drain).
PC/BE3	2	I/O	PCI bus command and byte enables. PC/BE3 enables byte 3 (MSB) of the PC/BE pins.
PC/BE2	16		PCI bus command and byte enables. PC/BE2 enables byte 2 of PCI address/data bus.
PC/BE1	28		PCI bus command and byte enables. PC/BE1 enables byte 1 of PCI address/data bus.
PC/BE0	41		PCI bus command and byte enables. PC/BE0 enables byte 0 of PCI address/data bus.
$\overline{\text{PDEVSEL}}$	21	I/O	PCI device select. $\overline{\text{PDEVSEL}}$ indicates that the driving device has decoded one of its addresses as the target of the current access. The TNETE110PM drives $\overline{\text{PDEVSEL}}$ when it decodes an access to one of its registers. As a bus master, the TNETE110PM monitors $\overline{\text{PDEVSEL}}$ to detect accesses to illegal memory addresses.
$\overline{\text{PFRAME}}$	17	I/O	PCI cycle frame. $\overline{\text{PFRAME}}$ is driven by the active bus master to indicate the beginning and duration of an access. $\overline{\text{PFRAME}}$ is asserted to indicate the start of a bus transaction and remains asserted during the transaction, only being deasserted in the final data phase.
$\overline{\text{PGNT}}$	132	I	PCI bus grant. $\overline{\text{PGNT}}$ is asserted by the system arbiter to indicate that the TNETE110PM has been granted control of the PCI bus.
PIDSEL	4	I	PCI initialization device select. PIDSEL is the chip select for access to PCI configuration registers.
$\overline{\text{PINTA}}$	128	O/D	PCI interrupt. $\overline{\text{PINTA}}$ is the interrupt request from the TNETE110PM. PCI interrupts are shared, so this is an open-drain (wired-OR) output.

† I = input, I/O = 3-state input/output, O/D = open-drain output
‡ Open drain

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

Pin Functions (Continued)

PIN NAME	NO.	TYPE†	DESCRIPTION
PCI INTERFACE (CONTINUED)			
$\overline{\text{PIRDY}}$	19	I/O	PCI initiator ready. $\overline{\text{PIRDY}}$ is driven by the active bus master to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. When the TNETE110PM is a bus master, it uses $\overline{\text{PIRDY}}$ to align incoming data on reads or outgoing data on writes with its internal RAM-access synchronization (maximum one cycle at the beginning of burst). When the TNETE110PM is a bus slave, it extends the access appropriately until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
$\overline{\text{PTRDY}}$	20	I/O	PCI target ready. $\overline{\text{PTRDY}}$ is driven by the selected device (bus slave or target) to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. ThunderLAN uses $\overline{\text{PTRDY}}$ to ensure every direct I/O (DIO) operation is correctly interlocked.
PPAR	27	I/O	PCI parity. PPAR carries even parity across PAD[31:0] and PC/BE[3:0]. It is driven by the TNETE110PM during all address and write cycles as a bus master and during all read cycles as a bus slave.
$\overline{\text{PPERR}}$	24	I/O	PCI parity error. $\overline{\text{PPERR}}$ indicates a data parity error on all PCI transactions except special cycles.
$\overline{\text{PREQ}}$	134	I/O	PCI bus request. $\overline{\text{PREQ}}$ is asserted by the TNETE110PM to request control of the PCI bus. This is not a shared signal.
$\overline{\text{PRST}}$	129	I	PCI reset signal (power-down enable configuration). The $\overline{\text{PRST}}$ pin should be connected to a reset signal (VAUXGOOD) by the auxiliary power supply. This pin resets the TNETE110PM on initial power up only. When $\overline{\text{PRST}}$ is asserted low, the TNETE110PM performs the following internal functions: – Resets all TNETE110PM registers and state machines – Puts all PCI outputs and IEEE standard (JTAG) pins in high impedance state asynchronously PCI reset signal (clock-run-enable configuration). The $\overline{\text{PRST}}$ pin should be connected to the $\overline{\text{PRST}}$ signal for the system. When $\overline{\text{PRST}}$ is asserted low, the TNETE110PM performs the following internal functions: – Resets all TNETE110PM registers and state machines – Puts all PCI outputs and IEEE standard (JTAG) pins in high impedance state asynchronously
$\overline{\text{PSERR}}$	25	O/D	PCI system error. $\overline{\text{PSERR}}$ indicates parity errors, or special cycle data parity errors.
$\overline{\text{PSTOP}}$	23	I/O	PCI stop. $\overline{\text{PSTOP}}$ indicates the current target is requesting the master to stop the current transaction.
BIOS ROM/LED DRIVER INTERFACE			
EAD7 EAD6 EAD5 EAD4 EAD3 EAD2 EAD1 EAD0	54 55 56 57 59 60 61 62	I/O	EPROM address/data. EAD[7:0] is a multiplexed byte bus that is used to address and read data from an external BIOS ROM. • On the cycle when EXLE is asserted low, EAD[7:0] is driven with the high byte of the address. • On the cycle when EALE is asserted low, EAD[7:0] is driven with the low byte of the address. • When $\overline{\text{EOE}}$ is asserted, BIOS ROM data should be placed on the bus. These pins can also be used to drive external status LEDs. Low-current (2–5 mA) LEDs can be connected directly (through appropriate resistors). High-current LEDs can be driven through buffers or from the BIOS ROM address latches.
EALE	65	O	EPROM address latch enable. EALE is driven low to latch the low (least significant) byte of the BIOS ROM address from EAD[7:0].
$\overline{\text{EOE}}$	64	O	EPROM output enable. When $\overline{\text{EOE}}$ is active (low) EAD[7:0] is in the high-impedance state and the output of the BIOS ROM should be placed on EAD[7:0].
EXLE	66	O	EPROM extended address latch enable. EXLE is driven low to latch the high (most significant) byte of the BIOS ROM address from EAD[7:0].

† I = input, O = output, I/O = 3-state input/output, O/D = open-drain output, A = analog
NOTE 1: This pin should be tied to V_{DD} with a 4.7-kΩ – 10-kΩ pullup resistor.

ADVANCE INFORMATION

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
CONFIGURATION EEPROM INTERFACE			
EDCLK	68	O	EEPROM data clock. EDCLK transfers serial clocked data to the 2K-bit serial EEPROMs (24C02) (see Note 1).
EDIO	69	I/O	EEPROM data I/O. EDIO is the bidirectional serial data/address line to the 2K-bit serial EEPROM (24C02). EDIO requires an external pullup for EEPROM operation. Tying EDIO to ground disables the EEPROM interface and prevents autoconfiguration of the PCI configuration register.
NETWORK INTERFACE (10 Base-T AND AUI)			
ACOLN ACOLP	111 109	A	AUI-receive pair. ACOLN and ACOLP are differential line-receiver inputs and connect to receive pair via transformer isolation, etc.
ARCVN ARCVP	108 106	A	AUI-receive pair. ARCVN and ARCVP are differential line-receiver inputs and connect to receive pair via transformer isolation, etc.
AXMTP AXMTN	99 100	A	AUI-transmit pair. AXMTP and AXMTN are differential line-transmitter outputs.
FATEST	118	A	Analog test pin. FATEST provides access to the filter of the reference PLL. This pin should be left as a no connect.
FIREF	116	A	Current reference. FIREF is used to set a current reference for the analog circuitry.
FONLY	120	A	Front-end only pin. The FONLY pin should be tied low for systems not requiring the power management capabilities of the TNETE110PM.
FRCVN FRCVP	105 103	A	10 Base-T receive pair. FRCVN and FRCVP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
FXTL1 FXTL2	113 114	A	Crystal oscillator pins. Drive FXTL1 from a 20-MHz crystal oscillator module.
FXMTP FXMTN	97 98	A	10 Base-T transmit pair. FXMTP and FXMTN are differential line transmitter outputs.
RESERVED	120	I	Reserved. Tie this pin low.
SERIAL MANAGEMENT INTERFACE			
MDIO	93	I/O	Management data I/O. MDIO is part of the serial management interface.
MRCLK	82	I	Receive clock. MRCLK is the receive clock source.
$\overline{\text{MRST}}$	95	O	MII reset. $\overline{\text{MRST}}$ is the reset signal.
POWER			
V_{DDI}	6, 14, 34, 48, 122, 136, 142	PWR	PCI V_{DD} pins (power-down-enable configuration). V_{DDI} pins provide power for the PCI I/O pin drivers. Connect V_{DDI} pins to a 5-volt power supply when using 5-V signals on the PCI bus. Connect V_{DDI} pins to a 3-volt power supply when using 3-V signals on the PCI bus. Pin #122 should be connected to a power supply that is not powered down during SLEEP mode. This supply must be the same voltage as V_{DDI} when the PCI bus is fully functional. PCI V_{DD} pins (clock-run-enable configuration). V_{DDI} pins provide power for the PCI I/O pin drivers. Connect V_{DDI} pins to a 5-volt power supply when using 5-V signals on the PCI bus. Connect V_{DDI} pins to a 3-volt power supply when using 3-V signals on the PCI bus.
V_{DDL}	22, 37, 58, 70, 79, 84 94, 130	PWR	Logic V_{DD} pins (5 V) (power-down-enable configuration). V_{DDL} pins provide power for internal TNETE110PM logic and should be connected to an auxiliary power source (5 V). Logic V_{DD} pins (5 V) (Clock-run-enable configuration). V_{DDL} pins provide power for internal TNETE110PM logic, and they always must be connected to 5 V.

Pin Functions (Continued)

POWER (CONTINUED)			
V_{DDR}	104 107	PWR	Analog power pin. V_{DDR} is the 5-V power for the receiver circuitry.
V_{DDT}	96	PWR	Analog power pin. V_{DDT} is the 5-V power for the transmitter circuitry.
V_{DDVCO}	117	PWR	Analog power pin. V_{DDVCO} is the 5-V power for the voltage controller oscillator (VCO) and filter input.
V_{DDOSC}	115	PWR	Analog power pin. V_{DDOSC} is the 5-V power for the crystal oscillator circuit.
V_{SSI}	3, 10, 26, 31, 40, 52, 67, 88, 127, 139	PWR	PCI I/O ground pins
V_{SSL}	18, 44, 63, 75, 92, 133	PWR	Logic ground pins
V_{SSOSC}	112	PWR	Analog power pin. Ground for crystal oscillator circuit
V_{SSR}	102 110	PWR	Analog power pin. Ground for receiver circuitry
V_{SST}	101	PWR	Analog power pin. Ground for transmitter circuitry
V_{SSVCO}	119	PWR	Analog power pin. Ground for VCO and filter input

† I = input, A = analog, PWR = power

architecture

The major blocks of the TNETE110PM include the PCI interface (PCIIF), protocol handler (PH), physical layer (PHY), FIFO pointer registers (FPREGS), FIFO SRAM (FSRAM), and a test-access port (TAP). The functionality of these blocks is described in the following sections.

PCI interface (PCIIF)

The TNETE110PM PCIIF contains a byte-aligning DMA controller that allows frames to be fragmented into any byte length and transferred to any byte address while supporting 32-bit data streaming. For multipriority networks it can provide multiple data channels, each with separate lists, commands, and status. Data for the channels is passed to and from the PH by way of circular buffer FIFOs in the SRAM, controlled through FIFO registers. The configuration EEPROM interface (CEI), BIOS ROM/LED driver interface (BRI), configuration and I/O memory registers (CIOREGS), and DMA controller are subblocks of the PCIIF. The features of these subblocks are as follows:

configuration EEPROM interface (CEI)

The CEI provides a means for autoconfiguration of the PCI configuration registers. Certain registers in the PCI configuration space may be loaded using the CEI. Autoconfiguration allows builders of TNETE110PM-based systems to customize the contents of these registers to identify their own system, rather than using the TI defaults. The EEPROM is read at power up and can then be read from, and written to, under program control.

BIOS ROM/LED driver interface (BRI)

The BRI addresses and reads data from an external BIOS ROM via a multiplexed byte-wide bus. The ROM address/data pins also can be multiplexed to drive external status LEDs.

configuration and I/O memory registers (CIOREGS)

The CIOREGS reside in the configuration space, which is 256 bytes in length. The first 64 bytes of the configuration space is the header region, which is explicitly defined by the PCI standard.

ADVANCE INFORMATION

DMA controller (DMAC)

The DMAC is responsible for coordinating TNETE110PM requests for mastership of the PCI bus. The DMAC provides byte-aligning DMA control allowing byte-size fragmented frames to be transferred to any byte address while supporting 32-bit data streaming.

protocol handler (PH)

The PH implements the serial protocols of the network. On transmit, it serializes data, adds framing and CRC fields, and interfaces to the network PHY. On receive, it provides address recognition, CRC and error checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular buffer FIFOs in the FSRAM controlled through FPREGS.

10 Base-T physical layer (PHY)

The PHY acts as an on-chip front-end providing physical layer functions for 10 Base-5 (AUI), 10 Base 2, and 10 Base-T (twisted pair). The PHY provides Manchester encoding/decoding from smart squelch, jabber detection, link pulse detection, autopolarity control, 10 Base-T transmission waveshaping, and antialiasing filtering. Connection to the AUI drop cable for the 10 Base-T twisted pair is made via simple isolation transformers (see Figure 2) and no external filter networks are required. Suitable external termination components allow the use of either shielded or unshielded twisted-pair cable (150 Ω or 100 Ω). Some of the key features of the on-chip PHY are listed as follow:

- Integrated filters
- 10 Base-T transceiver
- AUI transceiver
- 10 Base-2 transceiver
- Autopolarity (reverse polarity correction)
- Loopback for twisted pair and AUI
- Full-duplex mode for simultaneous 10 Base-T transmission and reception
- Low power

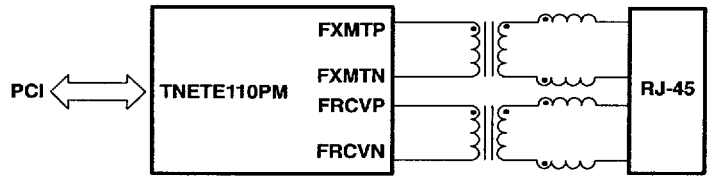


Figure 2. Schematic for 10 Base-T Network Interface Using TNETE110PM

FIFO pointer registers (FPREGS)

The FPREGS are used to implement circular buffer FIFOs in the SRAM. They are a collection of pointer and counter registers used to maintain the FIFO operation. Both the PCIIF and PH use FPREGS to determine where to read or write data in the SRAM and to determine how much data the FIFO contains.

FIFO SRAM (FSRAM)

The FSRAM is a conventional SRAM array accessed synchronously to the PCI bus clock. Access to the RAM is allocated on a time-division multiplexed (TDM) basis, rather than through a conventional shared bus. This removes the need for bus arbitration and provides ensured bandwidth. Half of the RAM accesses (every other cycle) are allocated to the PCI controller. It has a 64-bit access port to the RAM, giving it 1 Gbps of bandwidth, sufficient to support 32-bit data streaming on the PCI bus. The PH has one-quarter of the RAM accesses, and its port may be up to 64 bits wide. A 64-bit port for the PH provides 512 Mbps of bandwidth, more than sufficient for a full-duplex 100-Mbps network. The remaining RAM accesses can be allocated toward providing even more PH bandwidth. The RAM also is accessible (for diagnostic purposes) from the TNETE110PM internal data bus. Host DIO (mapped I/O) accesses are used by the host to access internal TNETE110PM registers and for adapter test.

Features of the FSRAM include:

- 3.375K bytes of FSRAM
- 1.5K-byte FIFO for receive channel
- One 1.5K-byte FIFO for transmit channel
- Three 128-byte lists

Supporting 1.5K bytes of FIFO per channel allows full-frame buffering of Ethernet frames.

test-access port (TAP)

Compliant with IEEE Standard 1149.1, the TAP is composed of five pins that are used to interface serially with the device and the board on which it is installed for boundary-scan testing.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 2) . . . . . – 0.5 V to 7 V
Input voltage range (see Note 2) . . . . . – 0.5 V to 7 V
Output voltage range . . . . . – 0.5 V to 7 V
Power dissipation . . . . . TBD
Operating case temperature range, T_C . . . . . 0°C to 95°C
Storage temperature range, T_{stg} . . . . . – 65 C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: Voltage values are with respect to V_{SS}, and all V_{SS} pins should be routed so as to minimize inductance to system ground.

The recommended operating conditions and the electrical characteristics tables are divided into groups, depending on pin function:

- PCI-interface pins
- Logic pins
- Physical layer pins

The PCI signal pins are operated in one of two modes shown in the PCI tables.

- 5-V signal mode
- 3-V signal mode

recommended operating conditions (PCI-interface pins) (see Note 3)

			3-V SIGNALING OPERATION			5-V SIGNALING OPERATION			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage (PCI)		3	3.3	3.6	4.75	5	5.25	V
V_{IH}	High-level input voltage		0.5 × V_{DD}		V_{DD}+0.5	2.0		V_{DD}+0.5	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 4)		–0.5		0.3 × V_{DD}	–0.5		0.8	V
I_{OH}	High-level output current	TTL outputs			–0.5			–2	mA
I_{OL}	Low-level output current (see Note 5)	TTL outputs			1.5			6	mA
T_C	Operating case temperature		0		95	0		95	°C
T_{stg}	Storage temperature		– 65		150	– 65		6	°C

NOTES: 3. PCI interface pins include V_{DDI}, PCLKRUN, PFRAME, PTRDY, PIRDY, PSTOP, PDEVSEL, PIDSEL, PPERR, PSERR, PREQ, PGNT, PCLK, PPAR, PRST, PINTA, PAD[31:0], PC/BE[3:0], TRST, TMS, TCLK, TDO, TDI.
4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (PCI-interface pins)

PARAMETER		TEST CONDITIONS†		3-V SIGNALING OPERATION		5-V SIGNALING OPERATION		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage, TTL-level signal (see Note 6)	V_{DD} = MIN,	I_{OH} = MAX	0.9 × V_{DD}		2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MAX,	I_{OL} = MAX		0.1 × V_{DD}		0.5	V
I_{OZ}	High-impedance output current	V_{DD} = MAX,	V_O = 0 V		10		10	µA
		V_{DD} = MAX,	V_O = V_{DD}		−10		− 10	
I_I	Input current, any input or input/output	V_I = V_{SS} to V_{DD}			± 10		± 70	µA
I_{DD}	Supply current	V_{DD} = MAX			50		60	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		10		10	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V		10		10	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.
NOTE 6: The following signals require an external pullup resistor: $\overline{\text{PSERR}}$ $\overline{\text{PINTA}}$.

recommended operating conditions (logic pins) (see Note 7)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (5 V only)		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		V_{DD}+0.3	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 4)		−0.3		0.8	V
I_{OH}	High-level output current	TTL outputs			−4	mA
I_{OL}	Low-level output current (see Note 5)	TTL outputs			4	mA

NOTES: 4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).
7. Logic pins include V_{DDL}, EAD[7:0], EXLE, EALE, $\overline{\text{EOE}}$, EDCLK, EDIO.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (logic pins)

PARAMETER		TEST CONDITIONS†		MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MAX,	I_{OL} = MAX			0.5	V
I_O	High-impedance output current	V_{DD} = MIN,	V_O = V_{DD}			10	µA
		V_{DD} = MIN,	V_O = 0 V			−10	
I_I	Input current	V_I = V_{SS} to V_{DD}				±10	µA
I_{DD}	Supply current 33 MHz (PCLK) (see Note 8)	V_{DD} = NOM			243		mA
I_{DD} (RESET)	Device reset (Idle)				178		mA
I_{DD} (SLEEP)	Sleep mode				51‡		mA
I_{DD} (RWAKE)	Remote Wake-up				186§		mA
I_{DD} (PWRDN)	Power-down				51		mA
C_i	Input capacitance, any input¶	f = 1 MHz,	Others at 0 V			10	pF
C_o	Output capacitance, any output or input/output¶	f = 1 MHz,	Others at 0 V			10	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.
‡ PCLK stopped
§ MTCLK stopped
¶ Assured by design
NOTE 8: More information on access to modes is available in the ThunderLAN Power Management and Remote Wake up specification.

recommended operating conditions (physical-layer pins) (see Note 9)

PARAMETER		JEDEC SYMBOL	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V

NOTE 9: Physical-layer pins include V_{DDOSC}, V_{DDR}, V_{DDT}, V_{DDVCO}, ACOLN, ACOLP, ARCVN, ARCVP, AXMTP, AXMTN, FATEST, FIREF, FRCVN, FRCVP, FXTL1, FXTL2, FXMTP, and FXMTN.

electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (physical-interface pins)

10 Base-T receiver input (FRCVP, FRCVN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
$V_{I(DIFF)}$	Differential input voltage†	V_{ID}			0.6	2.8	V
$I_{(CM)}$	Common-mode current†	I_{IC}				4	mA
V_{SQ+}	Rising input pair squelch threshold (see Note 10)		V_{CM} = V_{SB},	See Note 11		270	mV
V_{SQ-}	Falling input pair squelch threshold (see Note 11)		V_{CM} = V_{SB},	See Note 11	−270		mV

† See recommended operating conditions
NOTES: 10. V_{SQ} is the voltage level at which input is assured to be seen as data.
11. V_{SB} is the self-bias of the input FRCVP and FRCVN.

electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (physical-interface pins) (continued)

10 Base-T transmitter drive characteristics (FXMTP, FXMTN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
V_{SLW}	Differential voltage at specified slew rate	$V_{OD(SLEW)}$		±2.2	±2.8	V
$V_{O(CM)}$	Common-mode output voltage	V_{OC}	See Figure 3d	0	4	V
$V_{O(DIFF)}$	Differential output voltage	V_{OD}	Into open circuit		5.25	V
$V_{O(I)}$	Output idle differential voltage	$V_{OD(IDLE)}$			±50	mV
$I_{O(FC)}$	Output current, fault condition†	$I_{O(FC)}$			300	mA

† Specified by design

AUI receiver input (ARCVP, ARCVN, ACOLP, ACOLN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{I(DIFF)1}$	Differential input voltage 1‡	$V_{ID(1)}$	See Note 12	0	3	V
$V_{I(DIFF)2}$	Differential input voltage 2‡	$V_{ID(2)}$	See Note 13	0	100	mV
$V_{(SQ)}$	Falling input pair squelch threshold			−325		mV

‡ See recommended operating conditions

NOTES: 12. Common-mode frequency range – 10 Hz to 40 kHz
13. Common-mode frequency range – 40 kHz to 10 MHz

AUI-transmitter drive characteristics (AXMTP, AXMTN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{O(DIFF)1}$	Differential output voltage	$V_{OD(1)}$	See Note 14	±500	±1315	mV
$V_{OI(DIFF)}$	Output idle differential voltage‡	$V_{OD(IDLE)}$			±40	mV
$V_{OI(DIFF)U}$	Output differential undershoot‡	$V_{OD(IDLE)U}$			100	mV
$I_{O(FC)}$	Output current, fault condition§	$I_{O(FC)}$			150	mA

‡ See recommended operating conditions

§ Characterized but not tested

NOTE 14: The differential voltage is measured as per Figure 3b.

crystal-oscillator characteristics

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{SB(FXTL1)}$	Input self-bias voltage	V_{IB}		1.7	2.8	V
$I_{OH(FXTL2)}$	High-level output current	I_{OH}	$V_{(FXTL2)} = V_{SB(FXTL1)}$ $V_{(FXTL1)} = V_{SB(FXTL1)} + 0.5\,V$	−1.3	−5.0	mA
$I_{OL(FXTL2)}$	Low-level output current	I_{OL}	$V_{(FXTL2)} = V_{SB(FXTL1)}$ $V_{(FXTL1)} = V_{SB(FXTL1)} - 0.5\,V$	−0.4	1.3	mA

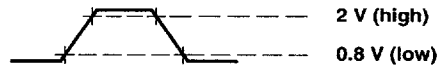
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

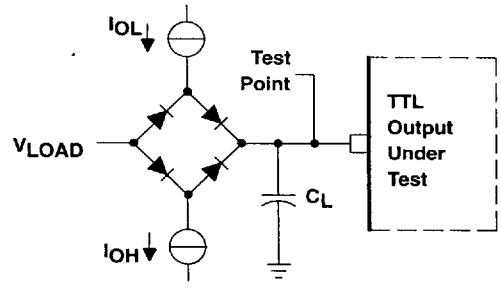
The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.



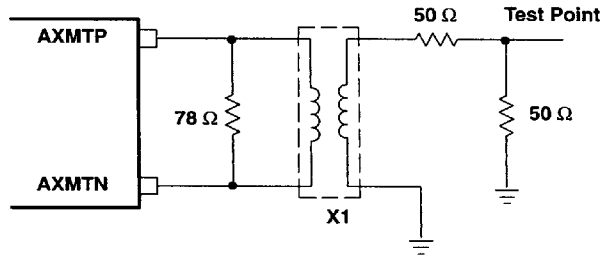
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

test measurement

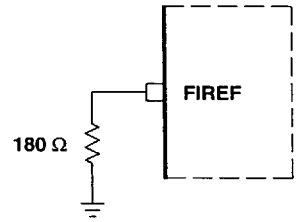
The test-load circuit shown in Figure 3 represents the programmable load of the tester pin electronics that are used to verify timing parameters of the TNETE110PM output signals.



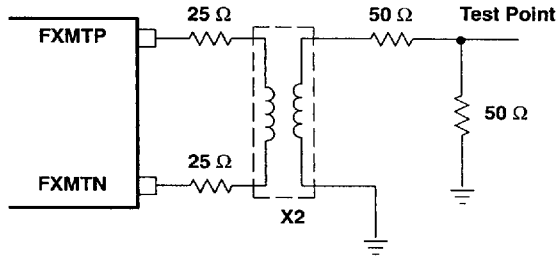
(a) TTL OUTPUT TEST LOAD



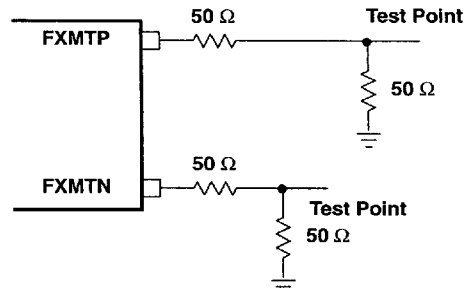
(b) AXMTP AND AXMTN TEST LOAD (AC TESTING)
X1–FII–Mag 23Z90(1:1)



(c) FIREF TEST CIRCUIT



(d) FXMTP AND FXMTN TEST LOAD (AC TESTING)
X2–FII–Mag 23Z128(1:$\sqrt{2}$)



(e) FXMTP and FXMTN TEST LOAD (DC TESTING)

Where: I_{OL} = Refer to I_{OL} in recommended operating conditions
I_{OH} = Refer to I_{OH} in recommended operating conditions
V_{LOAD} = 1.5 V, typical dc-level verification or 0.7 V, typical timing verification
C_L = 18 pF, typical load-circuit capacitance

Figure 3. Test and Load Circuit

switching characteristics for 5-V and 3.3-V PCI (see Note 15 and Figure 4)

	PARAMETER	MIN	MAX	UNIT
t_{VAL}	Delay time, PCLK to bused signals valid (see Notes 16 and 17)	2	11	ns
$t_{VAL(PTP)}$	Delay time, PCLK to bused signals valid point-to-point (see Notes 16 and 17)	2	12	ns
t_{on}	Float to active delay	2		ns
t_{off}	Active to float delay		28	ns

NOTES: 15. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.
16. Minimum times are measured with a 0-pF equivalent load; maximum times are measured with a 50-pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications.
17. $\overline{\text{PREQ}}$ and $\overline{\text{PGNT}}$ are point-to-point signals, and have different output-valid delay and input-setup times than do bused signals. $\overline{\text{PGNT}}$ has a setup time of 10 ns; $\overline{\text{PREQ}}$has a setup time of 12 ns. All other signals are bused.

timing requirements for 5-V and 3.3-V PCI (see Note 16 and Figure 4)

	PARAMETER	MIN	MAX	UNIT
t_{su}	Setup time, bused signals valid to PCLK (see Note 17)	7		ns
$t_{su(PTP)}$	Setup time to PCLK—point-to-point (see Note 17)	10, 12		ns
t_h	Input hold time from PCLK	0		ns
t_c	Cycle time, PCLK (see Note 18)	30	500	ns
$t_{w(H)}$	Pulse duration, PCLK high	11		ns
$t_{w(L)}$	Pulse duration, PCLK low	11		ns
t_{slew}	Slew rate, PCLK (see Note 19)	1	4	V/ns

NOTES: 16. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.
17. $\overline{\text{PREQ}}$ and $\overline{\text{PGNT}}$ are point-to-point signals, and have different output-valid delay and input-setup times than do bused signals. $\overline{\text{PGNT}}$ has a setup time of 10 ns; $\overline{\text{PREQ}}$has a setup time of 12 ns. All other signals are bused.
18. As a requirement for frame transmission/reception, the minimum PCLK frequency varies with network speed. The clock may be stopped only in a low state.
19. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.

timing requirements for PCI 5-V and 3.3-V (see Note 16 and Figure 4) (continued)

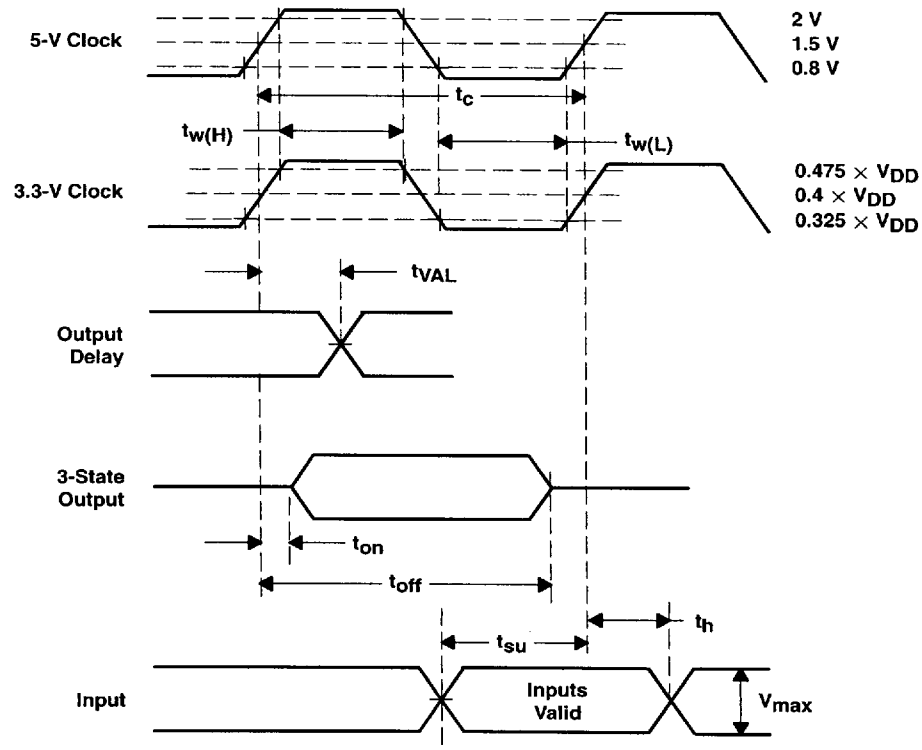


Figure 4. 5-V and 3.3-V PCI Timing

ADVANCE INFORMATION

timing requirements for management data I/O (MDIO) (see Figure 5)

		MIN	MAX	UNIT
$t_{a(MDCLKH-MDIOV)}$	Access time, MDIO valid from MDCLK high (see Note 20)	0	300	ns

NOTE 20: When the MDIO signal is sourced by the PMI/PHY, it is sampled by TNETE110PM synchronous to the rising edge of MDCLK.

switching characteristics for management data I/O (MDIO) (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$t_{su(MDIOV-MDCLKH)}$	Setup time, MDIO valid to MDCLK high (see Note 21)	10		ns
$t_{h(MDCLKH-MDIOX)}$	Hold time, MDCLK high to MDIO changing (see Note 21)	10		ns

NOTE 21: MDIO is a bidirectional signal that can be sourced by TNETE110PM or the PMI/PHY. When TNETE110PM sources the MDIO signal, TNETE110PM asserts MDIO synchronous to the rising edge of MDCLK.

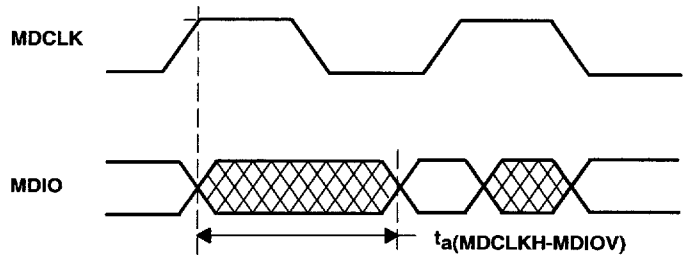


Figure 5. Management Data I/O Timing (Sourced by PHY)

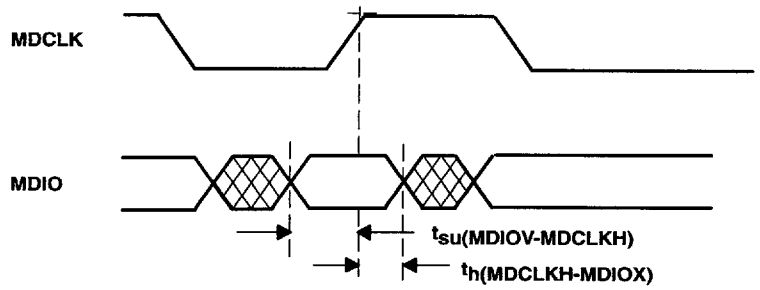


Figure 6. Management Data I/O Timing (Sourced by TNETE110PM)

ADVANCE INFORMATION

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

timing requirements for BIOS ROM and LED interface (see Figure 7)†

		MIN	MAX	UNIT
t_{su}	Setup time, data		250	ns
t_h	Hold time, data	0		ns

† The EPROM interface, consisting of 11 pins, requires only two TTL '373 latches to latch the high and low addresses.

switching characteristics for BIOS ROM and LED interface (see Figure 7)†

PARAMETER		MIN	MAX	UNIT
$t_{d(EADV-EXLEL)}$	Delay time, address high byte valid to EXLE low (address high byte setup time for external latch)	0		ns
$t_{d(EXLEL-EADZ)}$	Delay time, EXLE low to address high byte invalid (address high byte hold time for external latch)	10		ns
$t_{d(EADV-EALEL)}$	Delay time, address low byte valid to EALE low (address low byte setup time for external latch)	0		ns
$t_{d(EALEL-EADZ)}$	Delay time, EALE low to address low byte invalid (address low byte hold time for external latch)	10		ns
t_a	Access time, address	288		ns

† The EPROM interface, consisting of 11 pins, requires only two TTL '373 latches to latch the high and low addresses.

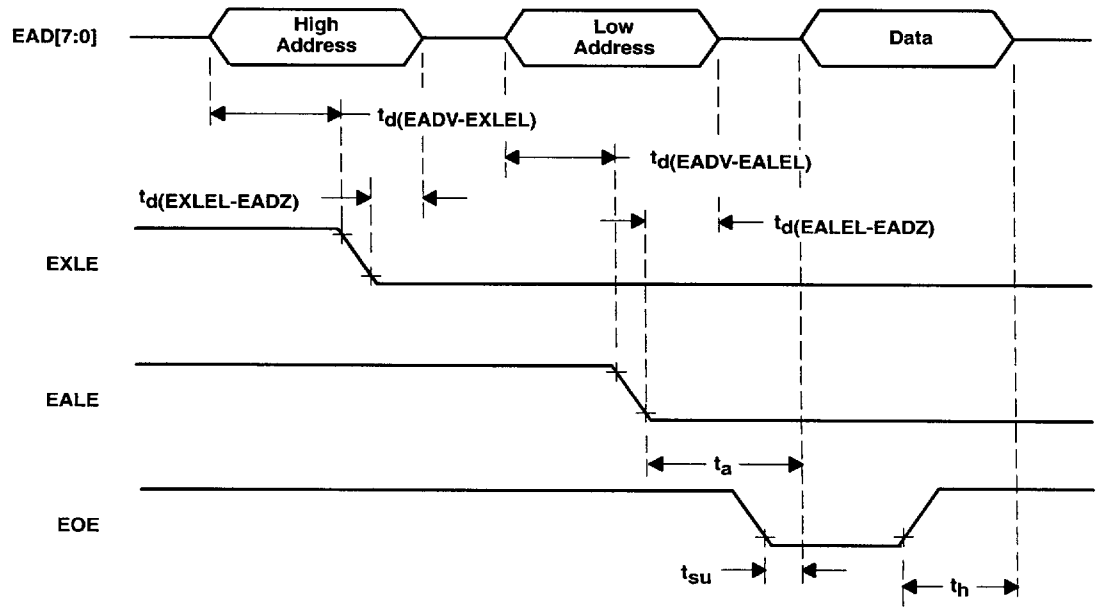


Figure 7. BIOS ROM and LED Interface Timing

ADVANCE INFORMATION

switching characteristics for configuration EEPROM interface (see Figure 8)

PARAMETER		MIN	MAX	UNIT
$f_{CLK(EDCLK)}$	Clock frequency, EDCLK	0	100	kHz
$t_{d(EDCLKL-EDIOV)}$	EDCLK low to EDIO data in valid	0.3	3.5	µs
$t_{d(EDIO\ free)}$	Time the bus must be free before a new transmission can start	4.7		µs
$t_{d(EDIOV-EDCLKL)}$	Delay time, EDIO valid after EDCLK low (start condition hold time for EEPROM)	4		µs
$t_{w(L)}$	Low period, clock	4.7		µs
$t_{w(H)}$	High period, clock	4		µs
$t_{d(EDCLKH-EDIOV)}$	Delay time, EDCLK high to EDIO valid (start condition setup time)	4.7		µs
$t_{d(EDCLKL-EDIOX)}$	Delay time, EDCLK low to EDIO changing (data out hold time)	0		µs
$t_{d(EDIOV-EDCLKH)}$	Delay time, EDIO valid to EDCLK high (data out setup time)	250		ns
t_r	Rise time, EDIO and EDCLK		1	µs
t_f	Fall time, EDIO and EDCLK		300	ns
$t_{d(EDCLKH-EDIOH)}$	Delay time, EDCLK high to EDIO high (stop condition setup time)	4.7		µs
$t_{d(EDCLKL-EDIOX)}$	Delay time, EDCLK low to EDIO changing (data in hold time)	300		ns

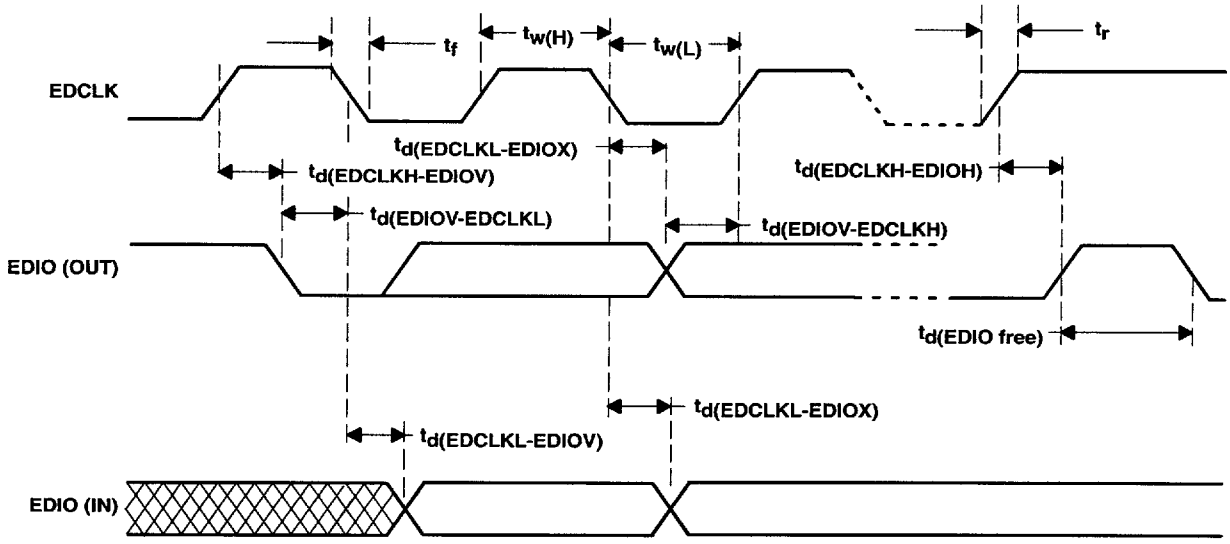


Figure 8. Configuration EEPROM Interface Timing

timing requirements for crystal oscillator (see Figure 9)†

		MIN	TYP	MAX	UNIT
$t_{d(VDDH-FXTL1V)}$	Delay time from minimum V_{DD} high level to first valid FXTL1V full swing period (see Note 22)			100	ms
$t_{w(H)}$	Pulse duration at FXTL1 high	13			ns
$t_{w(L)}$	Pulse duration at FXTL1 low	13			ns
t_t	Transition time of FXTL1		7		ns
t_c	Cycle time, FXTL1		50		ns
	Tolerance of FXTL1 input frequency		±0.01		%

† The FXTL signal may be implemented either by connecting a 20-MHz crystal across the FXTL1 and FXTL2 pins or by driving the FXTL1 from a 20-MHz crystal-oscillator module.

NOTE 22: This specification is provided as an aid to board design. This specification is not qualified during manufacturing testing.

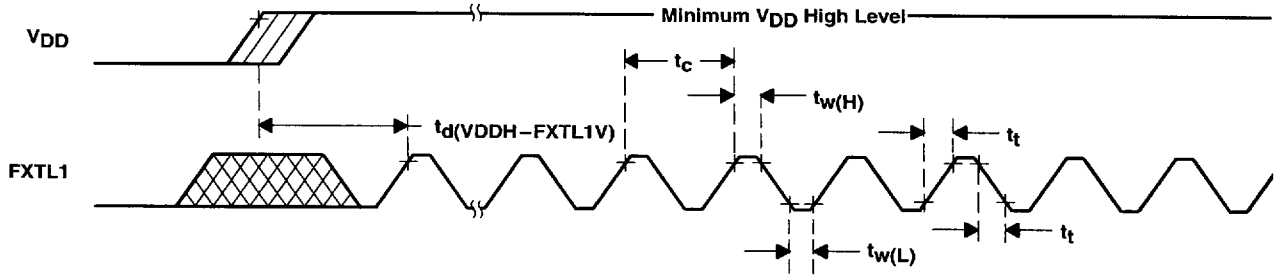


Figure 9. Crystal-Oscillator Timing

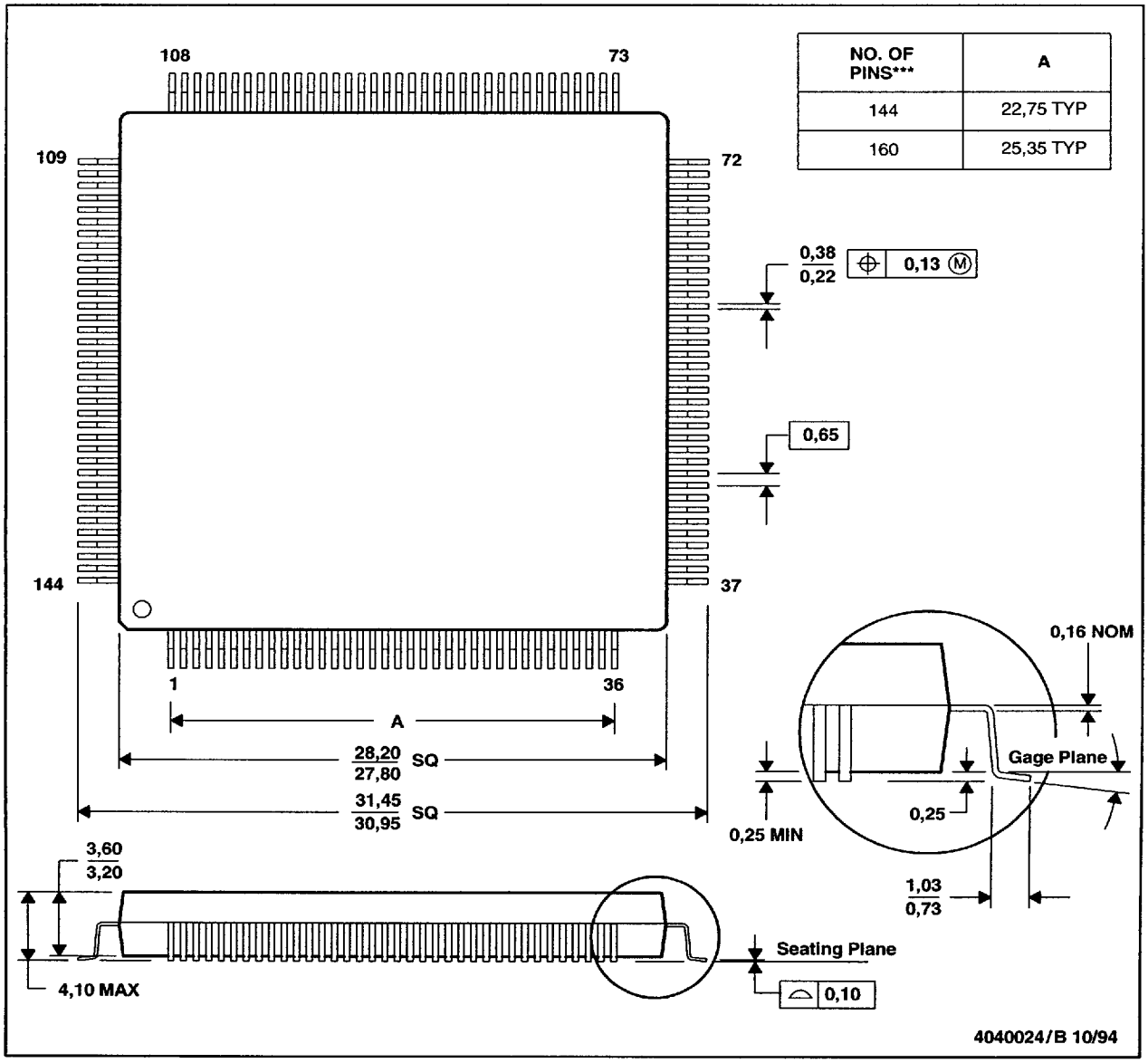
ADVANCE INFORMATION

ADVANCE INFORMATION

MECHANICAL DATA

PCM (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

144 PIN SHOWN



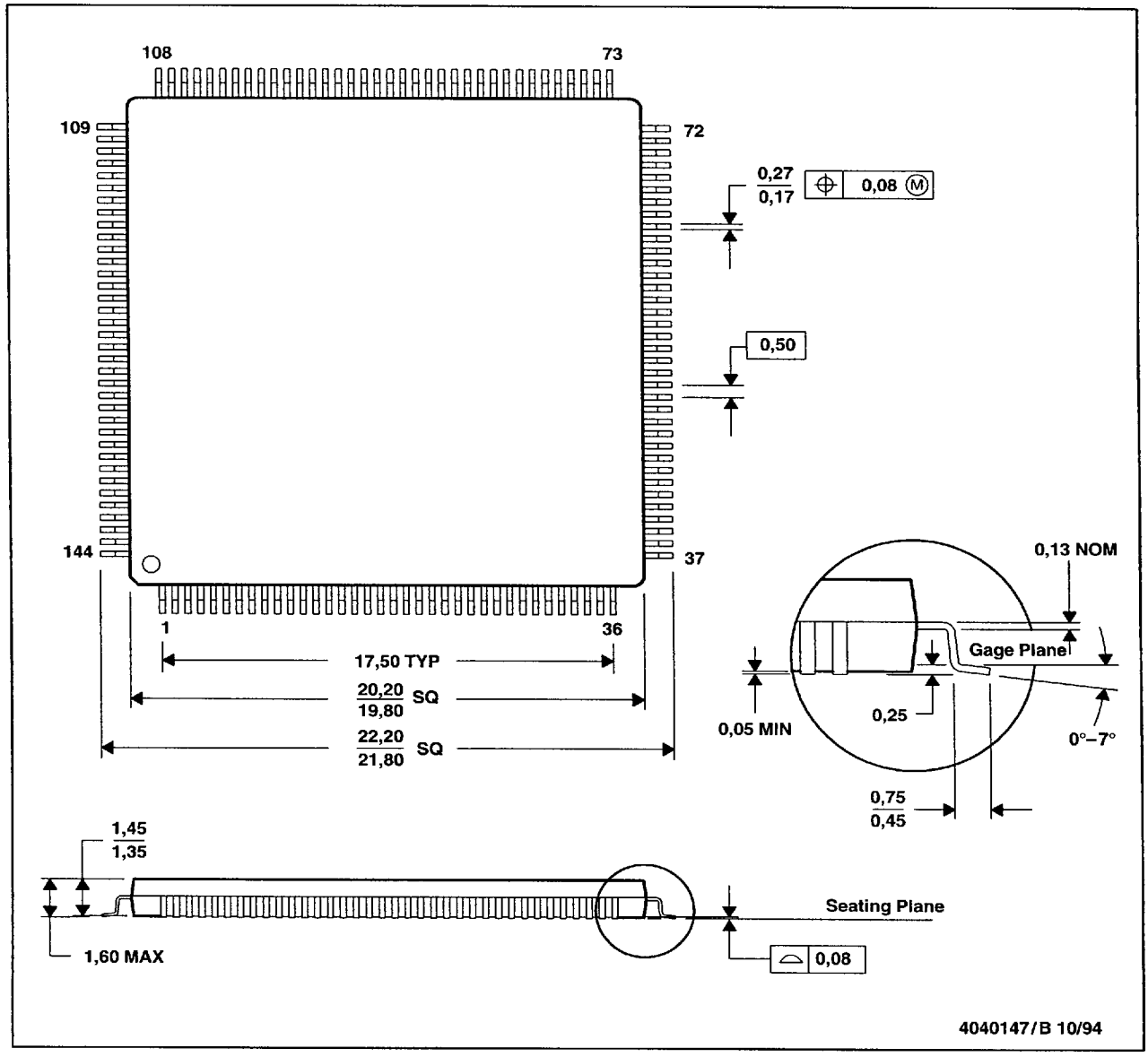
NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022
D. The 144 PCM is identical to the 160 PCM except that four leads per corner are removed.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

MECHANICAL DATA

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

ADVANCE INFORMATION