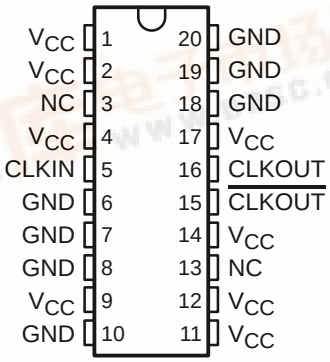
TNETA1630
622.08-MHz CLOCK-GENERATION DEVICE

SDNS029C – OCTOBER 1994 – REVISED DECEMBER 1995

- **Generates a 622.08-MHz Clock From a 19.44-MHz TTL Clock**
- **Provides Differential Pseudo-ECL (PECL) Outputs**
- **Operates From a SIngle 5-V Power Supply**
- **Packaged in 20-Pin Plastic Small-Outline (DW) Package**

DW PACKAGE
(TOP VIEW)

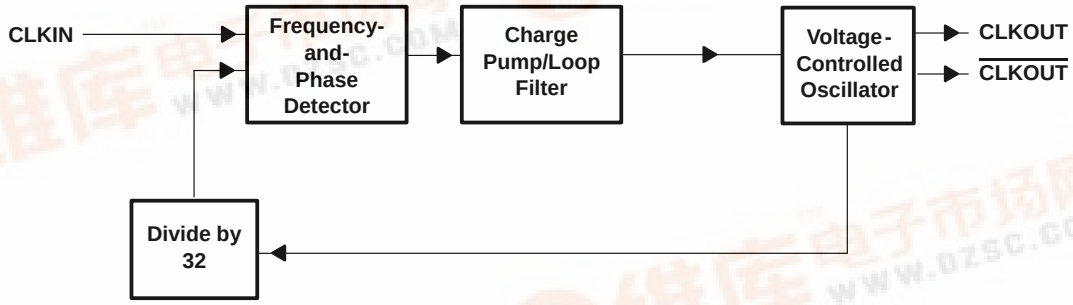


NC – No internal connection

description

The TNETA1630 is a 622.08-MHz clock-generation device that utilizes a TTL-clock input at 19.44 MHz. The 622.08-MHz clock is provided on differential pseudo-ECL (PECL) outputs. The device operates from a single 5-V power supply. An internal second-order low-pass filter is used to reduce jitter.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	5	I	19.44-MHz TTL-input clock
CLKOUT	16	O	622.08-MHz PECL-output clock true
$\overline{\text{CLKOUT}}$	15	O	622.08-MHz PECL-output clock complement
GND	6, 7, 8, 10, 18, 19, 20		Ground (0-V reference)
V_{CC}	1, 2, 4, 9, 11, 12, 14, 17		Supply voltage
NC	3, 13		No connection. Leave floating.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –1.2 V to 7 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	TTL (see Note 2)	2			V
V_{IL}	Low-level input voltage	TTL (see Note 2)			0.8	V
I_{IK}	Input clamp current	TTL			–18	mA
T_A	Operating free-air temperature		–40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 5 V		V_{CC} – 0.975			V
V_{OL}	Low-level output voltage	V_{CC} = 5 V			V_{CC} – 1.525		V
$V_{O(PP)}$	Output voltage swing, PECL	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	400			mV
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_L = –18 mA			–1.2	V
I_I	Input current, TTL	V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, Outputs open	f = 622.08 MHz,			50	mA
		V_{CC} = 5.25 V, See Note 4	f = 622.08 MHz,			75	

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. PECL outputs are terminated to V_{CC} – 2 V.
4. PECL outputs are terminated with a 50-Ω resistor to V_{CC} – 2 V.

operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty cycle, generated clock	See Note 4	45%	50%	55%	
RMS jitter, generated clock			9	12	ps
Peak-to-peak jitter, generated clock			35	120	ps

NOTE 4: PECL outputs are terminated with a 50-Ω resistor to $V_{CC}-2$ V.

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