

## ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

- Supports Segmentation and Reassembly of AAL5 Packets in Accordance With ITU-T Specifications I.361 and I.363 (11/93 Update)
- Integrated 32-Bit PCI Bus 2.1 (06/95) Interface for Transferring Packet Data to and From Host Memory
- Provides Simultaneous Segmentation of up to 2048 Packets
- Provides Simultaneous Reassembly of up to 2048 Packets
- Provides Full VPI/VCI Support (12 VPI Bits and 16 VCI Bits) for Transmit and Receive Operations
- Supports Constant-Bit-Rate (CBR) Traffic via High-Priority Mechanism or Local Static Scheduler Table
- Backward Compatible With the TNETA1570 in 32-Bit PCI Mode
- Provides Support for Available-Bit-Rate (ABR) Traffic via External Coprocessor Interface (COPI)
- Provides Support for VBR-nrt, VBR-rt, and UBR Traffic via External COPI
- Transmit-Channel Sleep Mode Prevents the SAR Polling Channels When No Packets Are Queued
- High-Performance Features Include Use of Sideband Signals to Reduce Polling Across the PCI Bus
- Host Accesses to the PHY-Layer Device Can Be Performed Indirectly via the TNETA1575 Local Peripheral Bus
- Local Peripheral Bus Maps the PHY Device Into the TNETA1575's PCI-Bus Address Space
- Supports Easy Access to the AAL5 Trailer Information
- Supports Buffer Scatter/Gather (Transmit and Receive Buffer Chaining)
- Optional Early Segmentation of Packets, So Segmentation Begins Once a Transmit Buffer Is Filled, Instead of Waiting for the Entire Packet to Be Available in Host Memory
- Calculates the HEC Byte for the Header of an Outgoing Cell
- Checks the HEC Byte of an Incoming Cell
- UTOPIA Level 1-Compliant Cell Interface
- Internal 32-Cell Receive FIFO
- Cell Interface Can Be Programmed to Operate as Either a Physical (PHY-Layer) Interface or as a SAR/Switch (ATM-Layer) Interface
- Provides Reassembly Time Out for Incoming Packets
- Provides an Internal Loopback Capability From Transmit to Receive
- Supports Boundary Scan Through a Five-Wire JTAG Interface in Accordance With IEEE Std 1149.1-1990 (Includes IEEE Std 1149.1a-1993)

### description

The TNETA1575 is an asynchronous transfer mode (ATM) segmentation and reassembly (SAR) device with a peripheral component interconnect (PCI)-bus interface and a coprocessor interface (COPI). The TNETA1575 continues the line of Texas Instruments (TI) ATM SAR devices directed toward the classical LAN-to-ATM translation market segment. Features have been extended to include the COPI interface, which interfaces to an external scheduler with high-performance features to eliminate polling on the PCI bus. The TNETA1575 is designed for the emerging class of high-performance enterprise networking hubs, which utilize ATM in the backplane, in addition to the traditional frame-/packet-based bus systems. Some of the features required for this application include: high level of virtual channel/virtual path support; support for isochronous services; early segmentation; and high-performance, 32-bit PCI-bus support. The feature set required by cell-switching enterprise hubs is different from the sets being offered by other SAR devices, which are directed primarily toward the adapter card market.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Thundercell is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



Copyright © 1996, Texas Instruments Incorporated

PRODUCT PREVIEW

TNETA1575

ATM SEGMENTATION AND REASSEMBLY DEVICE

WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

PRODUCT PREVIEW

		MFP PACKAGE	
		(TOP VIEW)	
		VCC	CMDA3
		CMDA15	GND
		CMDA14	CMDA2
		GND	CMDA1
		CMDA13	CMDA0
		CMDA12	VCC(5V)
		CMDA11	GND
		CMDA10	LINTR
		CMDA9	RCCX
		CMDA8	VCCX
		VCC	VCC
		CMDA7	DAX
		GND	GND
		CMDA6	COPFULL
		CMDA5	RESET
		CMDA4	LBDATA1
		VCC	LBDATA2
		CMDA16	VCC
		GND	LBDATA3
		CMDA15	LBDATA4
		CMDA14	LBDATA5
		CMDA13	LBDATA6
		CMDA12	GND
		CMDA11	LBDATA7
		CMDA10	LBREADY
		GND	VCC(5V)
		CMDA9	LBSC2
		VCC	LBR/W
		CMDA8	GND
		CMDA7	LBAD0
		CMDA6	LBAD1
		CMDA5	LBAD2
		CMDA4	LBAD3
		VCC	LBAD4
		CMDA17	GND
		GND	LBAD5
		CMDA16	LBAD6
		CMDA15	LBAD7
		CMDA14	LBAD8
		CMDA13	GND
		CMDA12	LBAD9
		CMDA11	VCC
		CMDA10	LBAD10
		GND	LBAD11
		CMDA9	PSB6
		VCC	GND
		CMDA8	PSB5
		CMDA7	PSB4
		CMDA6	PSB3
		CMDA5	VCC
		CMDA4	PSB2
		CMDA3	GND
		CMDA2	TXQUERDY
		CMDA1	SBLENGTH
		GND	LBINTR
		CMDA0	VCC(5V)
		VCC	PAD0
		GND	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19	
		CMDA18	
		CMDA17	
		VCC	
		CMDA16	
		GND	
		CMDA15	
		CMDA14	
		CMDA13	
		CMDA12	
		CMDA11	
		CMDA10	
		GND	
		CMDA9	
		VCC	
		CMDA8	
		CMDA7	
		CMDA6	
		CMDA5	
		CMDA4	
		CMDA3	
		CMDA2	
		CMDA1	
		GND	
		CMDA0	
		VCC	
		CMDA31	
		CMDA30	
		CMDA29	
		GND	
		CMDA28	
		CMDA27	
		CMDA26	
		VCC(5V)	
		CMDA25	
		CMDA24	
		GND	
		CMDA23	
		CMDA22	
		CMDA21	
		CMDA20	
		CMDA19</	

TNETA1575  
**ATM SEGMENTATION AND REASSEMBLY DEVICE  
 WITH PCI-HOST AND COPROCESSOR INTERFACES**  
 SDNS040A – MAY 1996 – REVISED JUNE 1996

## Terminal Functions

### PCI-bus interface

TERMINAL NAME	NO.	I/O	DESCRIPTION
PAD31 – PAD0	119–121, 123–124, 126–127, 129, 133–134, 136–139, 141–142, 158–160, 162, 164–167, 171–173, 175–177, 179, 181	I/O (3 state)	PCI address bus and data bus. PAD31 – PAD0 are multiplexed on the same PCI terminals. During the first phase of the address phase of a transaction, PAD31 – PAD0 contain a 32-bit physical address. This phase is the clock cycle when PFRAME is asserted.  During the data phase, PAD7 – PAD0 contain the least-significant byte and PAD31 – PAD24 contain the most-significant byte. Write data is stable when PIRDY is asserted. Read data is stable when PTRDY is asserted. Data is transferred during those clock cycles when both PIRDY and PTRDY are asserted.
PCBE3 – PCBE0	130, 144, 156, 169	I/O (3 state)	PCI-bus command and byte enable. PCBE3 – PCBE0 lines are multiplexed on the same PCI terminals. During the address phase of a transaction, PCBE3 – PCBE0 lines define the bus command. During the data phase, PCBE3 – PCBE0 lines define which bytes are valid.
PCLK	114	I (TTL)	PCI clock. PCLK provides timing for all transactions on the PCI interface.
PDEVSEL	149	I/O (3 state)	PCI device select. When actively driven, PDEVSEL indicates that the address of the driving device is decoded as the target of the current access. As an input, PDEVSEL indicates whether any device on the bus is selected.
PFRAME	145	I/O (3 state)	PCI frame. PFRAME is driven by the current master to indicate the beginning and duration of an access. PFRAME is asserted at the beginning of the bus transaction and remains asserted during data transfer. When PFRAME is deasserted, the transaction is in the final data phase.
PGNT	116	I (TTL)	PCI-bus grant. PGNT indicates to the agent that the arbiter has granted access to the bus. PGNT is a point-to-point signal and every master has its own.
PIDSEL	131	I (TTL)	PCI initialization and device select. PIDSEL is used as a chip select during configuration read and write transactions.
PINTA	112	O (open drain)	PCI interrupt. PINTA is an interrupt request from PCI SAR. PINTA indicates to the host that a condition has occurred that may require attention. The TNETA1575 uses only a single interrupt line.
PIRDY	147	I/O (3 state)	PCI initiator ready. PIRDY indicates the initiating agent's (bus master) ability to complete the current data phase of the transaction. During a write, PIRDY indicates valid data on PAD31 – PAD0. During a read, PIRDY indicates the master is prepared to accept the data. PIRDY is used with PTRDY. Wait cycles are inserted until both PIRDY and PTRDY are asserted.
PPAR†	155	I/O (3 state)	PCI parity. PPAR is even parity across PAD31 – PAD0 and PCBE3 – PCBE0. For data phases, PPAR is valid one clock after either PIRDY is asserted on a write or PTRDY is asserted on a read. Once asserted, PPAR remains valid until one clock after the completion of the current data phase. The master drives the PPAR for address- and write-data phases, and the target drives PPAR for the read-data phase.
PPERR‡	152	I/O (3 state)	PCI parity error. PPERR reports a data-parity error on all commands except special cycle. An agent cannot report a PPERR until it has claimed the access by asserting PDEVSEL and completed a data phase.

† If the host does not desire to implement parity in the system, terminal 155 is connected through a resistor to a valid logic level and the SERR enable bit in the PCI command register is set to 0.

‡ If the host does not desire to implement parity in the system, terminal 152 is connected through a 1-M $\Omega$  pullup resistor and the SERR enable bit in the PCI command register is set to 0.

PRODUCT PREVIEW

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**

SDNS040A – MAY 1996 – REVISED JUNE 1996

**Terminal Functions (Continued)**

**PCI-bus interface (continued)**

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{PREQ}}$	118	O (CMOS)	PCI request. $\overline{\text{PREQ}}$ indicates to the arbiter that this agent desires use of the bus. Every master has its own $\overline{\text{PREQ}}$ .
$\overline{\text{PRST}}$	113	I (TTL)	PCI reset. $\overline{\text{PRST}}$ forces the PCI sequence of each device to a known state.
PSB1–PSB0	110–111	O (CMOS)	PCI sideband. PSB1–PSB0 lines define the size of the transfer when the TNETA1575 is the bus master. The definitions of these signals are as follows: 00: 4-byte transfer 01: 16-byte transfer (except for receive-completion ring) 10: Payload transfer 11: Transfer to receive-completion ring (20-byte transfer) PSB1–PSB0 are synchronous to the address phase of the bus-master operations by the TNETA1575. The sideband signals do not change upon a bus retry after disconnect.
PSB2	187	I (TTL)	PCI sideband 2. PSB2 is an indication from the host to the SAR that the host has read an entry from the receive-completion ring without an interrupt. The SAR uses this signal to increment the receive-completion-ring entry counter. Pulse duration is for one clock cycle synchronous to the PCI-address phase. This input terminal has an internal 100- $\mu$ A pulldown active terminator. This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-k $\Omega$ down resistor and a 24-k $\Omega$ up resistor to ensure that the input is not driven above 3.3 V.
PSB3	189	O (CMOS)	PCI sideband 3. PSB3 is an indication from the SAR to the host that the SAR is reading an entry from sideband-controlled free-buffer ring 1. PSB3 is synchronous to the address phase of bus-master operations by the SAR. PSB3 does not change upon a bus retry after disconnect. Pulse duration is for one clock cycle synchronous to the PCI-address phase.
PSB4	190	I (TTL)	PCI sideband 4. PSB4 is an indication from the host to the SAR that the host has written a new entry into sideband-controlled free-buffer ring 1. The SAR uses this signal to increment the sideband-controlled free-buffer ring-1 entry counter. Pulse duration is for one clock cycle synchronous to the PCI-address phase. This input terminal has an internal 100- $\mu$ A pulldown active terminator. This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-k $\Omega$ down resistor and a 24-k $\Omega$ up resistor to ensure that the input is not driven above 3.3 V.
PSB5	191	O (CMOS)	PCI sideband 5. PSB5 is an indication from the SAR to the host that the SAR is reading an entry from sideband-controlled free-buffer ring 2. PSB5 is synchronous to the address phase of bus-master operations by the SAR. PSB5 does not change upon a bus retry after disconnect. Pulse duration is for one clock cycle synchronous to the PCI-address phase.
PSB6	193	I (TTL)	PCI sideband 6. PSB6 is an indication from the host to the SAR that the host has written a new entry into sideband-controlled free-buffer ring 2. The SAR uses this signal to increment the sideband-controlled free-buffer ring-2 entry counter. Pulse duration is for one clock cycle synchronous to the PCI-address phase. This input terminal has an internal 100- $\mu$ A pulldown active terminator. This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-k $\Omega$ down resistor and a 24-k $\Omega$ up resistor to ensure that the input is not driven above 3.3 V.
$\overline{\text{PSERR}}$	154	I/O (open drain)	PCI system error. $\overline{\text{PSERR}}$ reports address-parity errors and data-parity errors on special-cycle commands.
$\overline{\text{PSTOP}}$	150	I/O (3 state)	PCI stop. $\overline{\text{PSTOP}}$ indicates that the current target is requesting the master to stop the current transaction.
$\overline{\text{PTRDY}}$	148	I/O (3 state)	PCI target ready. $\overline{\text{PTRDY}}$ indicates the target agent's (selected device) ability to complete the current data phase of the transaction. During a read, $\overline{\text{PTRDY}}$ indicates that valid data is present on PAD31–PAD0. During a write, $\overline{\text{PTRDY}}$ indicates that the target is prepared to accept data.

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**  
SDNS040A – MAY 1996 – REVISED JUNE 1996

**Terminal Functions (Continued)**

**PCI-bus interface (continued)**

TERMINAL NAME	NO.	I/O	DESCRIPTION
SBLENGTH	184	O (CMOS)	Sideband length. SBLENGTH indicates to the host when the TNETA1575 is bursting eight free-buffer entries by asserting SBLENGTH high, or that it is bursting one entry when inactive low. Pulse duration is for one clock cycle synchronous to the PCI-address phase.
TXQUERDY	185	O (CMOS)	Transmit queue ready. TXQUERDY indicates to the host when the transmit queue register is available for a write access by the host. TXQUERDY is a PCI-sideband signal and is synchronous with the PCI clock.

**cell-segmentation interface**

TERMINAL NAME	NO.	I/O	DESCRIPTION
SEGCLAV	98	O (CMOS)	Segmentation cell available
			PHY mode SEGCLAV ( $\overline{\text{RXEMPTY}}/\text{RXCLAV}$ ) indicates that a complete cell is available.
			ATM mode SEGCLAV ( $\overline{\text{TXENB}}$ ) is active low when SEGDATA contains a valid byte.
SEGCLK	95	I (TTL)	Segmentation clock
			PHY mode SEGCLK (RXCLK) is used to synchronize transfers on SEGDATA. SEGCLK is sourced from the UTOPIA interface.
			ATM mode SEGCLK (TXCLK) is used to synchronize transfers on SEGDATA. SEGCLK is sourced from the ATMCLK.
SEGDATA7 – SEGDATA0	84–87, 89–92	O (CMOS)	Segmentation data
			PHY mode SEGDATA7 – SEGDATA0 (RXDATA) is byte-wide true data that is sourced by the TNETA1575. SEGDATA7 is the MSB.
			ATM mode SEGDATA7 – SEGDATA0 (TXDATA) is byte-wide true data that is sourced by the TNETA1575. SEGDATA7 is the MSB.
$\overline{\text{SEGEN}}$	96	I (TTL)	Segmentation enable
			PHY mode $\overline{\text{SEGEN}}$ ( $\overline{\text{RXENB}}$ ) indicates that a valid byte of SEGDATA will be sent during the next clock cycle.
			ATM mode $\overline{\text{SEGEN}}$ ( $\overline{\text{TXFULL}}/\text{TXCLAV}$ ) indicates that at least 1-byte of SEGDATA will be accepted.
SEGPARG	94	O (CMOS)	Segmentation parity
			PHY mode SEGPARG (RXPAR) is the odd-parity bit over SEGDATA7 – SEGDATA0.
			ATM mode SEGPARG (TXPAR) is the odd-parity bit over SEGDATA7 – SEGDATA0.
SEGSOC	97	O (CMOS)	Segmentation start of cell
			PHY mode SEGSOC (RXSOC) is active high when SEGDATA contains the first valid byte of the cell and is sourced by the TNETA1575.
			ATM mode SEGSOC (TXSOC) is active high when SEGDATA contains the first valid byte of the cell and is sourced by the TNETA1575.

**PRODUCT PREVIEW**

# TNETA1575

## ATM SEGMENTATION AND REASSEMBLY DEVICE

### WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

#### Terminal Functions (Continued)

#### high-priority segmentation (request and acknowledge)

TERMINAL NAME	NO.	I/O	DESCRIPTION
HPSACK	108	O (CMOS)	High-priority segmentation acknowledge. HPSACK is asserted for one PCI-bus clock cycle to acknowledge that HPSREQ is detected.
HPSREQ	109	I (TTL)	High-priority segmentation request. HPSREQ is sampled at each new segmentation opportunity and is synchronous to the PCI-bus clock. When HPSREQ is active, TNETA1575 initiates the procedure for transmitting a cell from TX DMA channel 1. To ensure that the high-priority segmentation request is processed, HPSREQ remains active until HPSACK is set low. HPSREQ is deasserted within two PCI-bus clock cycles of when HPSACK is asserted.

#### cell-reassembly interface

TERMINAL NAME	NO.	I/O	DESCRIPTION
RESCLAV	69	O (CMOS)	Reassembly cell available
			PHY mode RESCLAV (TXFULL/TXCLAV) indicates that a transfer of a complete cell can be accepted.
			ATM mode RESCLAV (RXENB) indicates that a valid byte RESDATA will be sent during the next clock cycle.
RESCLK	66	I (TTL)	Reassembly clock
			PHY mode RESCLK (TXCLK) is used to synchronize transfers on RESDATA. The UTOPIA interface is used as the source for RESCLK.
			ATM mode RESCLK (RXCLK) is used to synchronize transfers on RESDATA. ATMCLK is used as the source for RESCLK.
RESDATA7 – RESDATA0	72 – 75, 77 – 80	I (TTL)	Reassembly data
			PHY mode RESDATA7 – RESDATA0 (TXDATA). RESDATA7 is the MSB.
			ATM mode RESDATA7 – RESDATA0 (RXDATA). RESDATA7 is the MSB.
RESEN	67	I (TTL)	Reassembly enable
			PHY mode RESEN (TXENB) goes active low when RESDATA contains a valid byte.
			ATM mode RESEN (RXEMPTY/RXCLAV) indicates that transfer of a complete cell can be accepted.
RESPAR	71	I (TTL)	Reassembly parity
			PHY mode RESPAR (TXPAR) is the odd-parity bit over RESDATA7 – RESDATA0.
			ATM mode RESPAR (RXPAR) is the odd-parity bit over RESDATA7 – RESDATA0.
RESPERR	81	O (CMOS)	Reassembly parity error (not required by UTOPIA)
			PHY mode RESPERR indicates that parity error was present at the previous rising edge of RESCLK.
			ATM mode RESCLK.
RESSOC	70	I (TTL)	Reassembly start of cell
			PHY mode RESSOC (TXSOC) is received when RESDATA contains the first valid byte of the cell.
			ATM mode RESSOC (RXSOC) is received when RESDATA contains the first valid byte of the cell.

PRODUCT PREVIEW

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**  
SDNS040A – MAY 1996 – REVISED JUNE 1996

**Terminal Functions (Continued)**

**control-memory interface**

TERMINAL NAME	NO.	I/O	DESCRIPTION
CMAD15– CMAD0	58–57, 55–50, 48, 46–41, 39	O (CMOS)	Control-memory address. CMAD15–CMAD0 contain a 16-bit physical address to the control memory.
$\overline{\text{CMBS1}}$	62	O (CMOS)	Control memory bank select 1. $\overline{\text{CMBS1}}$ selects bank 1, containing 32K x 32 SRAM addresses in the lower 64K addresses, when active low.
$\overline{\text{CMBS2}}$	63	O (CMOS)	Control memory bank select 2. $\overline{\text{CMBS2}}$ selects bank 2, containing 32K x 32 SRAM addresses in the lower 64K addresses, when active low.
CMDATA31– CMDATA0	35–33, 31–29, 27–25, 23–18, 16, 14–9, 7, 5–1, 240, 238–236	I (TTL) O (CMOS)	Control-memory data. CMDATA31–CMDATA0 contain 32-bit data to/from the control memory.
$\overline{\text{CMOE}}$	36	O (CMOS)	Control-memory output enable. When $\overline{\text{CMOE}}$ is active low, the address is valid and data is read on the rising edge of $\overline{\text{CMOE}}$ .
$\overline{\text{CMSELHI}}$	61	O (CMOS)	Control memory select high. $\overline{\text{CMSELHI}}$ selects the upper 64K control-memory addresses when active low.
$\overline{\text{CMSELLO}}$	59	O (CMOS)	Control memory select low. $\overline{\text{CMSELLO}}$ selects the lower 64K control-memory addresses when active low.
$\overline{\text{CMWE}}$	37	O (CMOS)	Control-memory write enable. When $\overline{\text{CMWE}}$ is active low, the address and data are valid.

**traffic coprocessor interface**

TERMINAL NAME	NO.	I/O	DESCRIPTION
RCCX	232	O (CMOS)	Receive-cell status indication. RCCX indicates to the traffic coprocessor that a cell was received on the UTOPIA interface, and the RX DMA channel was assigned to the cell.
TCCX	231	O (CMOS)	Transmit-cell status indication. TCCX indicates to the traffic coprocessor that a cell was transmitted from the SAR, and the TX DMA channel was assigned to the cell.
DAX	229	O (CMOS)	Data availability indication. DAX indicates to the traffic coprocessor when data is available on a particular channel or when the SAR has completed segmentation of a packet.
$\overline{\text{LRESET}}$	226	O (CMOS)	Local reset. $\overline{\text{LRESET}}$ provides a reset indication to the traffic coprocessor. $\overline{\text{LRESET}}$ is derived from the PCI-bus reset input.
$\overline{\text{LINTR}}$	233	I (TTL)	Local interrupt. $\overline{\text{LINTR}}$ provides an interrupt indication from the traffic coprocessor to the SAR. When $\overline{\text{LINTR}}$ goes active low, the SAR sets a bit in the status register and generates a PCI interrupt unless the interrupt is masked through the interrupt mask register. This terminal has an internal 100- $\mu$ A pullup active terminator. This signal must be connected to an external 2.2-k $\Omega$ pullup resistor that is connected to a 3.3-V voltage source.
$\overline{\text{COPFULL}}$	227	I (TTL)	Coprocessor full. $\overline{\text{COPFULL}}$ indicates that the traffic coprocessor RX FIFO is about to fill up. A 100- $\mu$ A pulldown active terminator is connected to this input. The pulldown is disabled when the COPPRES bit is set in the SAR configuration register.

**PRODUCT PREVIEW**

# TNETA1575

## ATM SEGMENTATION AND REASSEMBLY DEVICE

### WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

#### Terminal Functions (Continued)

##### local-bus interface

TERMINAL NAME	NO.	I/O	DESCRIPTION
LBAD11– LBAD0	194–195, 197, 199–202, 204, 206–209	O (CMOS)	Local-Bus address. LBAD11–LBAD0 are driven by the TNETA1575 and are used to address the peripheral attached to the local bus. Terminal 194 is the most significant bit.
LBR $\overline{W}$	211	O (CMOS)	Local-bus read/write. LBR $\overline{W}$ is an active-low signal that indicates a write operation and is driven by the TNETA1575. A read operation is indicated as active high.
$\overline{LBCS1}$	99	O (CMOS)	Local-bus chip select 1. $\overline{LBCS1}$ is an active-low signal that is used to select an external peripheral on the TNETA1575 local bus.
$\overline{LBCS2}$	212	O (CMOS)	Local-bus chip select. 2 $\overline{LBCS2}$ is an active-low signal that is used to select an external peripheral on the TNETA1575 local bus.
$\overline{LBREADY}$	214	I (TTL) (with internal pullup)	Local-bus ready. $\overline{LBREADY}$ is driven by a local-bus slave device. The TNETA1575 has two modes of operation on this input terminal. The default mode causes the TNETA1575 to complete the bus transaction after eight PCI-bus cycles <u>regardless</u> of $\overline{LBREADY}$ . Alternatively, the TNETA1575 can be placed in a mode using $\overline{LBREADY}$ . This is a 3.3-V tolerant input signal. If it is driven by a 5-V signal, it must be connected to an external voltage divider consisting of a 36-k $\Omega$ down resistor and a 24-k $\Omega$ up resistor to ensure that the input is not driven above 3.3 V.
$\overline{LBINTR}$	183	I (TTL) (with internal pullup)	Local-bus interrupt. $\overline{LBINTR}$ is an active-low interrupt that is generated and driven by a local-bus device. This signal must be connected to an external 2.2-k $\Omega$ pullup resistor that is connected to a 3.3-V voltage source.
LBDATA7– LBDATA0	215, 217–220, 222, 224–225	I/O (TTL input / CMOS output) and (with internal pullup)	Local-bus data. LBDATA7–LBDATA0 are used to transfer data to and from a local-bus slave device, and are driven by the TNETA1575 or a local-bus slave device. LBDATA7, (terminal 215) is the most-significant bit.

##### boundary-scan interface

TERMINAL NAME	NO.	I/O	DESCRIPTION
TCK	103	I (TTL)	Test clock. TCK clocks the test-access-port (TAP) operation.
TDI	106	I (TTL)	Test data input. TDI shifts serial-test data and instructions into the device during TAP operation.
TDO	105	O (TTL)	Test data output. TDO shifts serial-test data and instructions out of the device during TAP operation.
TMS	104	I (TTL)	Test-mode select. TMS controls the state of the TAP controller.
$\overline{TRST}$	102	I (TTL)	Test reset. $\overline{TRST}$ asynchronously forces the TAP controller to a known state.

##### test signal

TERMINAL NAME	NO.	I/O	DESCRIPTION
TESTMODE	101	I (TTL)	Test mode. TESTMODE is used for device testing. High is for test mode and low is for normal operation.



### Terminal Functions (Continued)

#### miscellaneous signals

TERMINAL NAME	NO.	I/O	DESCRIPTION
ATMCLK1	82	O (CMOS)	ATM clock1
			PHY mode    ATMCLK1 is driven low and can be left as a no connection (NC).
			ATM mode    The ATMCLK1 is used as the clock source to provide for data transfers/synchronization across the transmit UTOPIA interface between the SAR and external devices not connected to the PCI-host interface. The ATMCLK1 is connected to SEGCLK in the ATM mode. If the TNETA1585 is not used, the ATMCLK1 can also be used as the clock source for the receive UTOPIA interface. The clock generated by the interface is 33 MHz (nominal), using the PCI clock.
ATMCLK2	64	O (CMOS)	ATM clock2. ATMCLK2 is an auxiliary ATM clock that is used as the clock source to the TNETA1585 or a similar-type device. When the TNETA1585 is used, ATMCLK2 is also connected to the RESCLK input. The clock generated by the interface is 33 MHz (nominal), using the PCI clock.
PHY/ $\overline{\text{ATM}}$	83	I (TTL)	PHY/ $\overline{\text{ATM}}$ mode select. PHY/ $\overline{\text{ATM}}$ selects ATM mode when low and the PHY mode when high.

#### power and ground

NAME	TERMINAL NO.	DESCRIPTION
GND	8, 15, 24, 32, 40, 47, 56, 76, 88, 107, 117, 122, 128, 135, 140, 146, 151, 157, 163, 168, 174, 180, 186, 192, 198, 203, 210, 216, 223, 228, 234, 239	Ground. GND is the 0-V reference for the device.
V <sub>CC</sub>	6, 17, 38, 49, 60, 65, 93, 115, 132, 143, 161, 170, 178, 188, 196, 205, 221, 230	Supply voltage. V <sub>CC</sub> is the 3.3-V supply for the digital logic.
V <sub>CC(5V)</sub>	28, 68, 100, 125, 153, 182, 213, 235	Supply voltage. V <sub>CC(5V)</sub> is the 5-V supply for the clamp diodes used with the 5-V tolerant input and output buffers for protection.

# TNETA1575 ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

---

## detail description

The TNETA1575 device contains the following interfaces:

- PCI-host interface
- Cell interface
- Local-bus interface
- Control-memory interface
- Traffic coprocessor interface
- JTAG interface

## PCI-host interface

The TNETA1575 incorporates a PCI revision 2.1-compliant (June 1, 1995) host interface. The following section describes the features and operation of the PCI-host interface.

The TNETA1575 operates as a PCI-slave device for configuration cycles, accesses to internal registers, and accesses to the onboard control memory. It also acts as a PCI-master device for accessing data structures, which are contained in host memory.

As a slave, the TNETA1575 incorporates the following features:

- Directly supports the memory read, memory write, configuration read and configuration write PCI commands and aliases the memory read multiple, memory read line, and memory write and invalidate to the basic memory commands.

- Supports single data-cycle transfers and disconnects with retry after the first data cycle.

- Does not retry single data accesses to any data structures accessed via the SAR, i.e., registers, control memory or coprocessor.

- Responds to accesses as a 32-bit agent with medium  $\overline{\text{DEVSEL}}$  timing (single wait state)

- Utilizes a 1-M block of addresses, which is mapped into the host memory space using a single base-address register.

- Does not support resource locking.

As a master, the TNETA1575 incorporates the following features:

- Utilizes the memory read, memory read line, memory read multiple, and memory write PCI bus commands.

- Initiates transactions as a 32-bit agent.

- Performs multiple data-cycle transfers, when possible, up to a maximum of 12 data cycles.

- The TNETA1575 asserts the  $\overline{\text{IRDY}}$  signal one clock cycle after the  $\overline{\text{FRAME}}$  signal is asserted.

- $\overline{\text{IRDY}}$  remains asserted during the burst cycle.

# TNETA1575

## ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

As described in the PCI local-bus specification rev 2.1, the TNETA1575 provides a 64-byte configuration space that can be accessed by system software for configuration, initialization, and error handling. The TNETA1575 responds to type 0 configuration accesses.

A configuration map of the 64-byte configuration space is as follows:

ADDRESS	BYTE 3	BYTE 2	BYTE 1	BYTE 0	READ/WRITE
0x00	Device ID		Vendor ID		R
0x04	Status		Command		R/W
0x08	Class Code			Revision ID	R
0x0C	BIST†	Header Type	Latency Timer	Cache Line Size	R/W
0x10	Base Address 0				R/W
0x14	Base Address 1†				R/W
0x18	Base Address 2†				R/W
0x1C	Base Address 3†				R/W
0x20	Base Address 4†				R/W
0x24	Base Address 5†				R/W
0x28	Cardbus CIS Pointer†				R
0x2C	Subsystem ID†		Subsystem Vendor ID†		R/W
0x30	Expansion ROM Base Address†				R/W
0x34	Reserved (returns 0 when read)				—
0x38	Reserved (returns 0 when read)				—
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	R/W
0x40	Reserved	Reserved	Reserved	Reserved	R/W
0x44 – 0xFF	Reserved (returns 0 when read)				R

<sup>†</sup> Optional registers are not implemented for the TNETA1575, which return 0 when read.

The control memory is accessed via the host PCI interface in full 32-bit words. Byte enable is not supported. All four bytes in a 32-bit word in the control memory are read or written in a single instruction.

If none of the byte enables are asserted for a write instruction, none of the data in the 32-bit word is altered. If any byte enable is asserted, then the entire 32-bit word is overwritten.

### cell interface

The TNETA1575 transfers and receives ATM cells through the cell interface. The cell interface is designed in accordance with the ATM forum UTOPIA level 1 specification and is configurable as either an 8-bit PHY or ATM interface. The ATM mode is chosen when the TNETA1575 interfaces with a framer such as the TNETA1500. The PHY mode is chosen when the TNETA1575 interfaces with a switch port. The operation of this dual ATM/PHY interface requires the use of two external terminals – ATMCLK and PHY/ATM. The ATMCLK output is a buffered version of the PCI clock.

When PHY/ATM is high (PHY mode), the segmentation interface functions as a PHY-RX port and the reassembly interface functions as a PHY-TX port. The clock speed supported by the interface is a maximum of 33 MHz. In this mode, the ATMCLK output normally is not used by the cell interface.

When PHY/ATM is low (ATM mode), the segmentation interface functions as an ATM-TX port and the reassembly interface functions as an ATM-RX port. The clock speed supported by the interface is a maximum of 33 MHz. In this mode, the ATMCLK can be used as the clock source to provide for data transfers/synchronization or another external-clock source(s) can be used.

The interface operates as a synchronous 8-bit (byte-wide) datapath. The interface functions with both octet-level and cell-level handshaking.

PRODUCT PREVIEW

# TNETA1575 ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

## segmentation interface, PHY mode

The segmentation-unit interface on the TNETA1575 operates as the RX UTOPIA interface on a PHY device when the TNETA1575 is operating in PHY mode. The PHY/ATM input terminal has to be high to operate in PHY mode.

This cell interface works on the low-to-high transition of SEGCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
SEGCLK	95	RXCLK
SEGDATA 7–SEGDATA0	84–87, 89–92	RXDATA7–RXDATA0
SEGPARG	94	RXPRTY
SEGSOC	97	RXSOC
<u>SEGEN</u>	96	<u>RXENB</u>
SEGCLAV	98	RXCLAV/RXEMPTY

## reassembly interface, PHY mode

The reassembly-unit interface on the TNETA1575 functions as the TX UTOPIA interface in a PHY device when the TNETA1575 is operating in PHY mode.

This reassembly-cell interface works on the low-to-high transition of RESCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

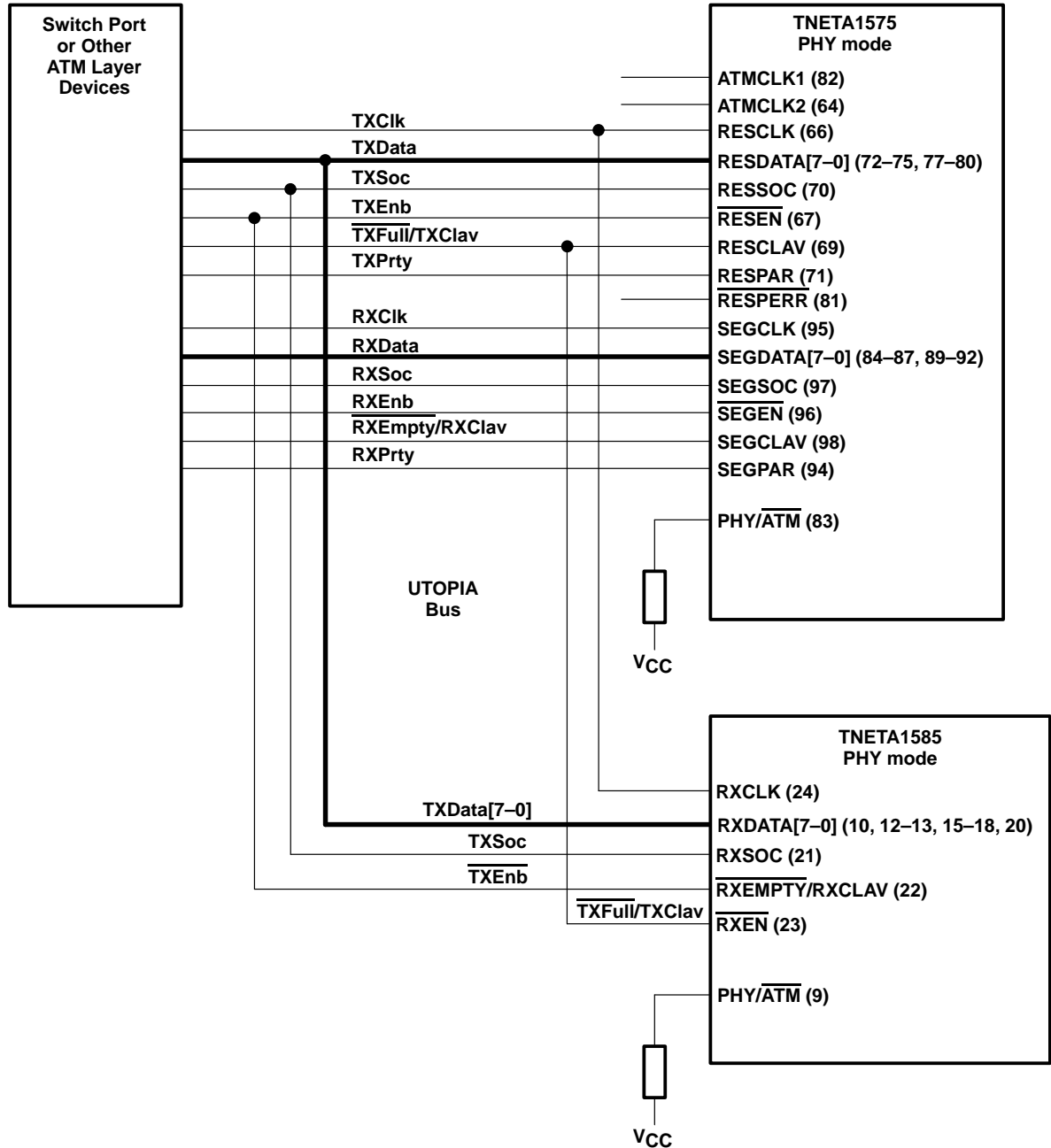
TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
RESCLK	66	TXCLK
RESDATA7–RESDATA0	72–75, 77–80	TXDATA7–TXDATA0
RESPARG	71	TXPRTY
RESSOC	70	TXSOC
<u>RESEN</u>	67	<u>TXENB</u>
RESCLAV	69	TXCLAV/TXFULL
<u>RESPERR</u>	81	N/A

# TNETA1575

## ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

connecting the TNETA1575 to the UTOPIA bus (See Figure 1 and Note A)



NOTE A: Figures 1 and 2 show the interconnections needed to interface to a TNETA1585 device. If the TNETA1575 is operated without the external scheduler device, then the lines going to the TNETA1585 are ignored, and everything remains as depicted above.

Figure 1. UTOPIA Bus Connections In PHY Mode

PRODUCT PREVIEW

# TNETA1575 ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

## *segmentation interface in ATM mode*

The segmentation-unit interface on the TNETA1575 operates as a TX UTOPIA interface in an ATM-layer device. The PHY/ATM terminal must be driven low to make the TNETA1575 operate in ATM mode.

This cell interface works on the low-to-high transition of SEGCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
SEGCLK	95	TXCLK
SEGDATA7–SEGDATA0	84–87, 89–92	TXDATA7–TXDATA0
SEGPART	94	TXPARTY
SEGSOC	97	TXSOC
SEGEN	96	TXCLAV/TXFULL
SEGCLAV	98	TXENB

## *reassembly interface in ATM mode*

The reassembly-unit interface on the TNETA1575 operates as the RX UTOPIA interface in an ATM device when the TNETA1575 is configured in ATM mode.

This receive cell interface works on the low-to-high transition of RESCLK to sample and generate signals. All signals are active high, unless noted with a bar above the signal name.

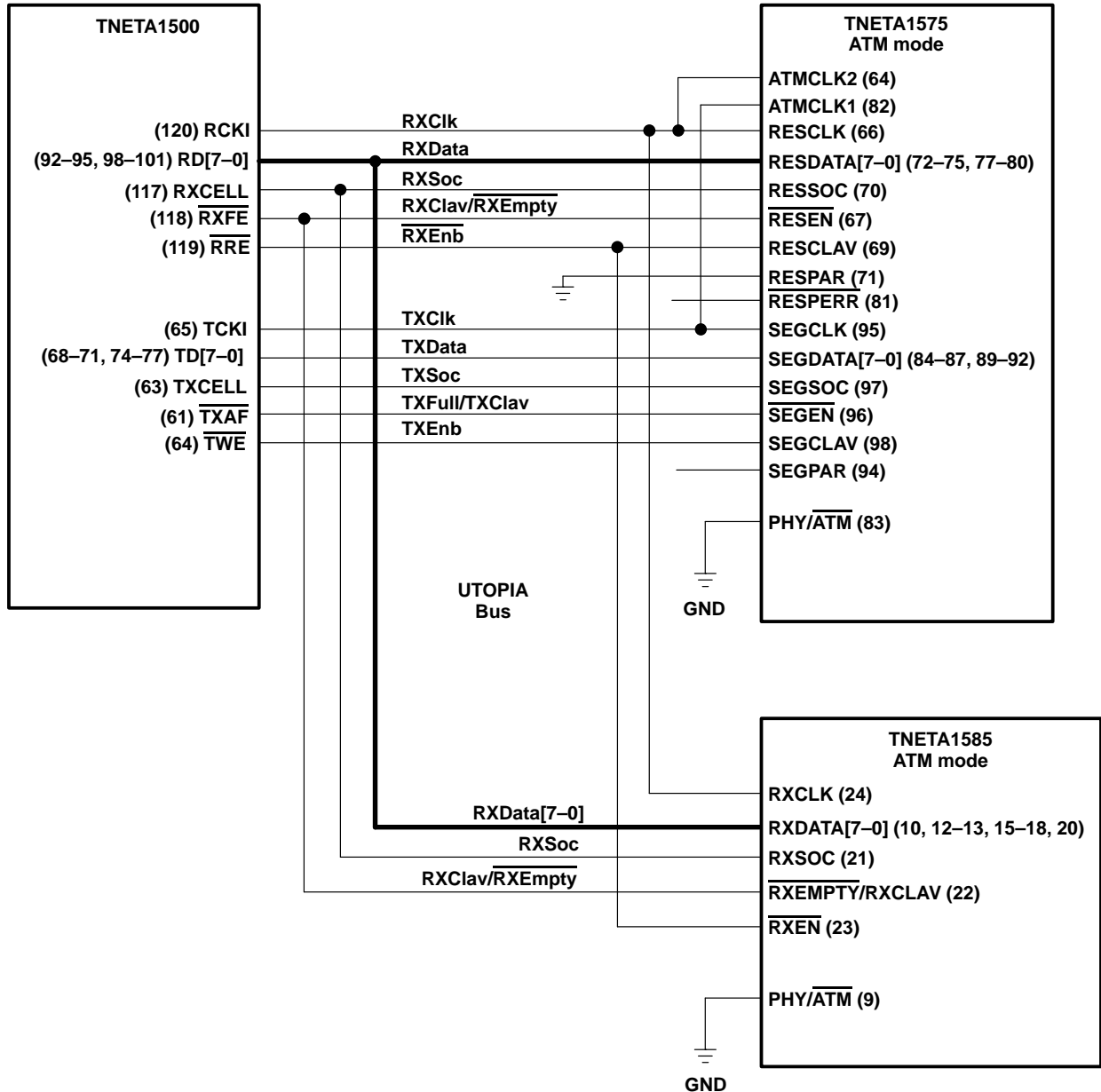
TNETA1575 SIGNAL NAME	TNETA1575 TERMINAL NUMBER	UTOPIA SIGNAL NAME
RESCLK	66	RXCLK
RESDATA7–RESDATA0	72–75, 77–80	RXDATA7–RXDATA0
RESPART	71	RXPARTY
RESSOC	70	RXSOC
RESEN	67	RXCLAV/RXEMPTY
RESCLAV	69	RXENB
RESPERR	81	N/A

# TNETA1575

## ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

*connecting the TNETA1575 to the UTOPIA bus (see Figure 2 and Note A)*



NOTE A: Figures 1 and 2 show the interconnections needed to interface to a TNETA1585 device. If the TNETA1575 is operated without the external scheduler device, then the lines going to the TNETA1585 are ignored, and everything remains as depicted above.

**Figure 2. UTOPIA Bus Connections in ATM Mode**

PRODUCT PREVIEW

# TNETA1575

## ATM SEGMENTATION AND REASSEMBLY DEVICE

### WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

#### local-bus interface

This interface allows access to the registers in two devices on the local bus. The TNETA1575 accepts a ready signal from devices on the bus as a handshake. This accommodates slow devices, and also can be used to relax timing constraints on the register interface for PHY-layer devices. The local bus is accessed exclusively via PCI-bus transactions with TNETA1575 as the slave, with the exception of the local-bus interrupt signal. The 12-bit address of the local bus comprises the PCI-bus address lines (bits 13–2). These directly drive the local-bus address bits (11–0). The signals in this interface are defined in the terminal-function table of this document.

#### control-memory interface

Control memory contains the local data structures and state information used by the device to transmit and receive data on a virtual connection (VC) or channel. The scheduler table, transmit active-packet counters, free-buffer ring-pointer table, and TX/RX DMA state table are located in control memory. The scheduler table contains 2,048 entries, consisting of one word each. The transmit active-packet counters contain the number of packets that have been queued for transmit on each packet segmentation ring. The free-buffer ring-pointer table contains the pointers to the receive free-buffer rings. There are 256 entries in the free-buffer ring-pointer table (one entry for each free-buffer ring), and each entry consists of two words. The TX/RX DMA state table contains 2,048 entries, one entry for each transmit-/receive-channel pair. Each entry consists of 16 words; eight words for the transmit operation and eight words for the receive operation. The definitions and functional description of the TNETA1575 data structures are discussed in detail in the *TNETA1575 Programmer's Reference Guide*, literature number SDNU015.

These local data structures are located off the chip in external SRAM. The TNETA1575 is designed to operate with 15-ns (or faster) asynchronous SRAM devices. The total SRAM requirement to support a full implementation of control memory is approximately 37K x 32. The device can operate with a control-memory SRAM of size 32K x 32. A system design with the 32K x 32 SRAM size only supports up to 1,792 TX/RX-channel pairs. To support the entire range of 2,048 TX/RX-channel pairs, the TNETA1575 requires a SRAM configuration of 64K x 32.

The control-memory map is listed below for the TNETA1575 device:

#### control-memory map

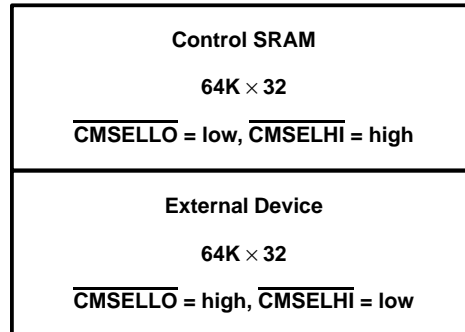
MEMORY BLOCK	SIZE (IN 32-BIT WORDS)	CONTROL-MEMORY ADDRESS (HEX)	PCI-OFFSET ADDRESS (HEX)
Scheduler table	2,048	00000–007FF	00000–01FFC
Active packet counters	1,024	00800–00BFF	02000–02FFC
Free-buffer ring cache†	14	00C00–00C0D	03000–03034
Reserved	498	00C0E–00DFF	03038–037FC
Free-buffer ring pointer-table	512	00E00–00FFF	03800–03FFC
TX/RX DMA state table	32,768	01000–08FFF	04000–23FFC
DMA lookup table†	4,096	09000–09FFF	24000–27FFF
Local-bus device 1 (LBCS1)	4,096	0A000–0AFFF	28000–2BFFC
Local-bus device 2 (LBCS2)	4,096	0B000–0BFFF	2C000–2FFFC
Reserved	16,384	0C000–0FFFF	30000–3FFFC
Traffic coprocessor memory space	65,536	10000–1FFFF	40000–7FFFC

† The free-buffer ring cache and the DMA lookup table are physically located on the chip. They are not located off of the chip in the control memory.



### control-memory interface (continued)

The SAR control-memory port is used to select both the external SRAM that stores the local-data structures and state information for the TNETA1575 and an external device that can be used to provide an external scheduler and other transmit data structures. The total control-memory address space consists of 128K locations, with 64K locations dedicated to the TNETA1575 SRAM, and the remaining 64K dedicated to an external device such as an external scheduler (see Figure 3).



**Figure 3. Control-Memory Address Space**

Control memory select bit  $\overline{\text{CMSELHI}}$  is used to select the upper 64K-address space.  $\overline{\text{CMSELHI}}$  is active low when the higher 64K addresses are selected and inactive when the lower 64K-addresses are selected. The control-memory select bit  $\overline{\text{CMSELLO}}$  is used to select the lower 64K-address space.

In addition, when the  $\overline{\text{CMSELLO}}$  terminal is active low and the lower 64K addresses are selected, the user can select between a single 64K x 32 SRAM bank or two 32K x 32 SRAM banks. The two terminals  $\overline{\text{CMSB1}}$  and  $\overline{\text{CMSB2}}$  are active low and allow the user to select between the two banks, as follows:

1.  $\overline{\text{CMSELLO}}$  is active low and CMA15 is low to select bank 1 ( $\overline{\text{CMSB1}}$  is enabled).
2.  $\overline{\text{CMSELLO}}$  is active low and CMA15 is high to select bank 2 ( $\overline{\text{CMSB2}}$  is enabled).

There are 16 control-memory address terminals that are used to address the various blocks of control memory. Together with the two select terminal ( $\overline{\text{CMSELLO}}$  and  $\overline{\text{CMSELHI}}$ ) and the two bank switching terminals, these 20 terminals provide for a total of 128K addressable-memory locations.

CONTROL-MEMORY ADDRESS SPACE SELECTED (HEXADECIMAL)	$\overline{\text{CMSELLO}}$	$\overline{\text{CMSB1}}$	$\overline{\text{CMSB2}}$	$\overline{\text{CMSELHI}}$
00000 – 07FFF	L	L	H	H
08000 – 0FFFF	L	H	L	H
10000 – 1FFFF	H	H	H	L

# TNETA1575 ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

## traffic coprocessor interface

The TNETA1575 provides a traffic coprocessor interface (COPI) to add flexibility to the segmentation scheduling algorithm. The COPI is implemented using the control-memory interface and three unidirectional serial channels that transfer information from the TNETA1575 to the coprocessor and COPI-full indicator signal.

The TNETA1575 acts as an initiator of all transfers to and from the coprocessor.

The primary method of communication between the TNETA1575 and a coprocessor is via the control-memory interface. It is intended that an external coprocessor be mapped into the control-memory space starting at address 10000 and extending to address 1FFFF. This equates to a total address space of 64K 32-bit words that is reserved for use by the coprocessor.

The mapping of the coprocessor in control memory provides a means for the TNETA1575 to initialize the coprocessor, to obtain information related to the scheduling of cells, and to obtain RM cell contents.

In this document, the three serial channels and the COPI-full indicator signal are described.

## received cell-indication channel

A serial-bit interface allows the TNETA1575 to signal to the coprocessor that a cell has been received on a particular DMA channel. This interface is necessary to avoid duplicating the hardware that is used to resolve a VPI/VCI to a DMA channel. When a cell is received, the VPI/VCI value from the header is extracted and is used as a key in a lookup algorithm. When the lookup is complete, the TNETA1575 sends a 13-bit frame to the coprocessor, which is formatted as follows:

DMA NUMBER	GOOD/BAD CELL INDICATOR	FRAMING
(12–2)	(1)	(0)

The frame is transmitted to the coprocessor through the RCCX terminal, starting with bit 0. When a frame is not actively being transmitted, the RCCX terminal is driven to a 0.

## transmitted cell-indication channel

A single-bit interface allows the TNETA1575 to signal to the coprocessor that a cell will be transmitted on a particular DMA channel. This interface is necessary to facilitate statistics processing in the coprocessor and to aid in ATM-forum available-bit-rate scheduling. As soon as the TNETA1575 determines that it has the data to send a cell, it simultaneously sends a 17-bit frame to the coprocessor, which is formatted as follows:

DMA NUMBER	CLP INDICATOR	CELL TYPE	SCHEDULING SOURCE	SEND ACKNOWLEDGE	FRAMING
(16–6)	(5)	(4–3)	(2)	(1)	(0)

The frame is transmitted to the coprocessor through the TCCX terminal, starting with bit 0. When a frame is not actively being transmitted, the TCCX terminal is driven to a 0.

## data-availability channel

A single-bit interface allows the TNETA1575 to signal to the coprocessor when data is available or unavailable on a particular channel. When the host writes to the transmit queue register to notify the TNETA1575 that a packet has been queued, or if the TNETA1575 completes segmentation of the last packet on a particular DMA channel, a 13-bit frame is sent to the coprocessor, which is formatted as follows:

DMA NUMBER	DATA AVAILABLE/UNAVAILABLE	FRAMING
(12–2)	(1)	(0)

The frame is transmitted to the coprocessor through the DAX terminal, starting with bit 0. When a frame is not actively being transmitted, the DAX terminal is driven to a 0.

# TNETA1575 ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

## ***COP – interface full-indication signal***

The COPI interface on the TNETA1575 provides a  $\overline{\text{COPFULL}}$  input terminal that indicates when the traffic coprocessor interface receive FIFOs are within one cell of filling up. The TNETA1575 reacts by deasserting the UTOPIA receive enable signal (RESCLAV or RXENABLE, depending on whether PHY or ATM mode is selected) according to the UTOPIA specification. After the  $\overline{\text{COPFULL}}$  input terminal goes inactive low, the TNETA1575 asserts the UTOPIA receive enable signal RESCLAV or RXENABLE, depending upon whether PHY or ATM mode is selected on the UTOPIA interface. If this terminal is not connected, the TNETA1575 operates under normal conditions.

## ***TNETA1575 / TNETA1585 interconnect***

Figure 4 shows the interconnect of the TNETA1575 (SAR) and the TNETA1585 traffic cop, including information on connection of the control-memory interface, the coprocessor interface, and the cell interfaces.

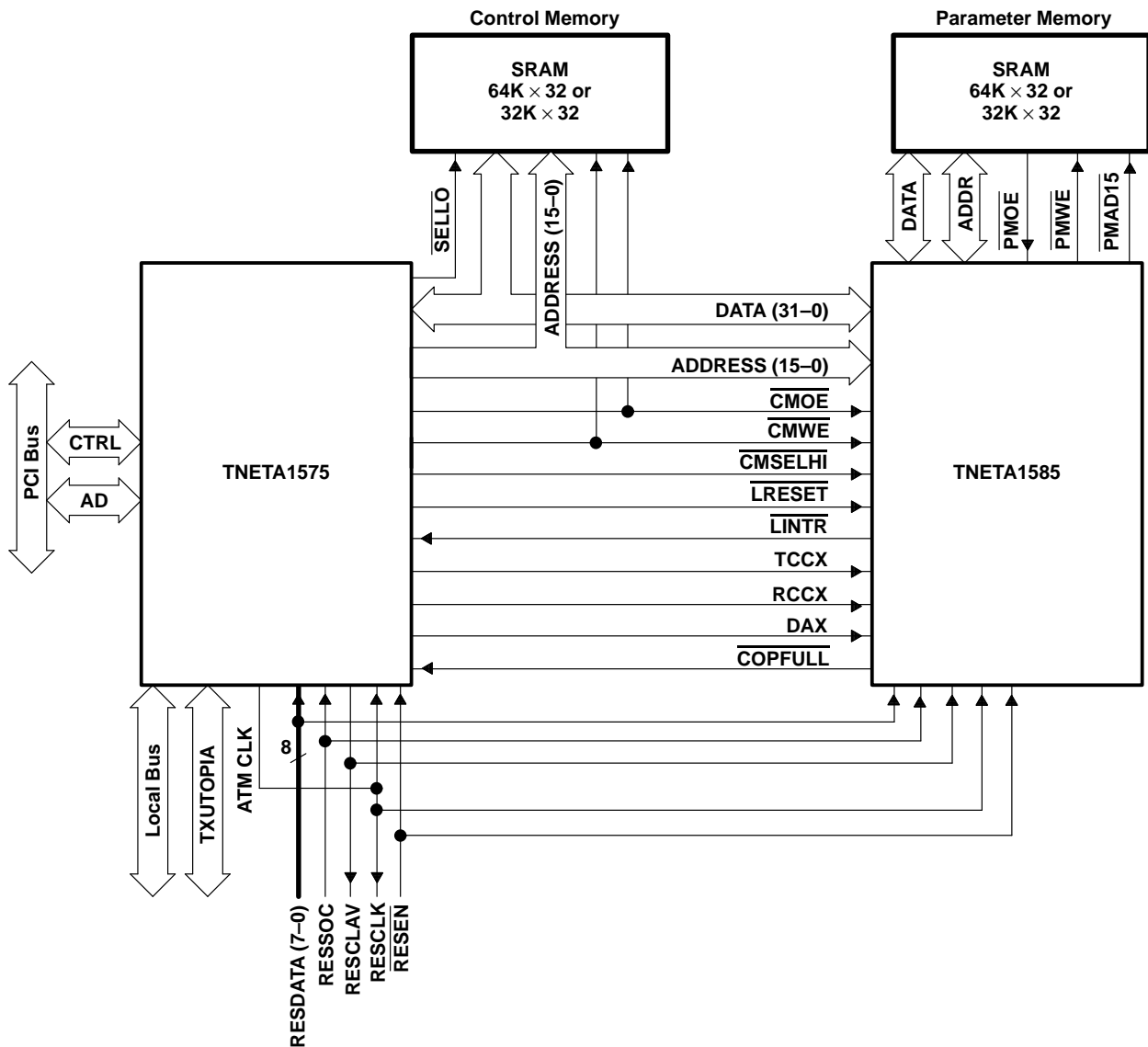


Figure 4. TNETA1575 Interconnect to TNETA1585

PRODUCT PREVIEW

# TNETA1575

## ATM SEGMENTATION AND REASSEMBLY DEVICE

### WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

#### JTAG interface

The TNETA1575 supports boundary scan through a five-wire JTAG interface in accordance with IEEE Std 1149.1–1990 (includes IEEE Std 1149.1a–1993), IEEE Standard Test Access Port and Boundary-Scan Architecture.

The maximum operating frequency is 10 MHz for the JTAG interface.

#### JTAG instruction set.

The TNETA1575 supports the following instructions:

INSTRUCTION	OP CODE (BINARY FORMAT)
Extest	000
Idcode	100
Sample/Preload	001
Bypass	111
Internal Scan	010
High Z	101

#### idcode

Bit number	VARIANT	PART NUMBER	MANUFACTURER	LSB
31–28	27–12	11–1	0	
Binary code	0000	TBD	00000010111	1

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 4 V
Supply voltage range, $V_{CC(5V)}$ (see Note 1)	–0.5 V to 5.5 V
Input voltage range, standard TTL, 3-V PCI, $V_I$	–0.5 V to $V_{CC} + 0.5$ V
Input voltage range, 5-V tolerant TTL, $V_I$	$V_{CC(5V)} + 0.5$ V
Output voltage range, standard TTL, 3-V PCI, $V_O$	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, 5-V tolerant TTL, $V_O$	5 V to $V_{CC} + 0.5$ V
Input clamp current, TTL, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 2)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 3)	±20 mA
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to the GND terminals.
  2. Applies for external input and bidirectional buffers without hysteresis.  $V_I > V_{CC}$  does not apply to fail-safe terminals. Use  $V_I > V_{CC(5V)}$  for 5-V tolerant terminals.
  3. Applies for external output and bidirectional buffers.  $V_O > V_{CC}$  does not apply to fail-safe terminals. Use  $V_O > V_{CC(5V)}$  for 5-V tolerant terminals.

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**

SDNS040A – MAY 1996 – REVISED JUNE 1996

**recommended operating conditions**

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Commercial	3	3.3	3.6	V
V <sub>CC(5 V)</sub>	Supply voltage, 5-V tolerant TTL	Commercial	4.5	5	5.5	V
V <sub>I</sub>	Input voltage	TTL, 3-V PCI	0		V <sub>CC</sub>	V
		5-V tolerant TTL	0		V <sub>CC(5 V)</sub>	
V <sub>O</sub>	Output voltage	TTL, 3-V PCI	0		V <sub>CC</sub>	V
		5-V tolerant TTL	0		V <sub>CC</sub>	
V <sub>IH</sub>	High-level input voltage	TTL	2		V <sub>CC</sub>	V
		3-V PCI	0.475 V <sub>CC</sub>		V <sub>CC</sub>	
		5-V tolerant TTL†	2		V <sub>CC(5 V)</sub>	
V <sub>IL</sub>	Low-level input voltage	TTL	0		0.8	V
		3-V PCI	0		0.325 V <sub>CC</sub>	
		5-V tolerant TTL	0		0.8	
T <sub>A</sub>	Operating free-air temperature		0		70	°C

† V<sub>CC</sub> must be applied with output on high-impedance state (Z) for 5-V tolerant operation.

**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	TTL	I <sub>OH</sub> = 8 mA	V <sub>CC</sub> – 0.6	V	
			I <sub>OH</sub> = 4 mA			
	5-V tolerant TTL	I <sub>OH</sub> = 8 mA	V <sub>CC</sub> – 0.6			
		I <sub>OH</sub> = 4 mA				
	3-V PCI	I <sub>OH</sub> = 8.6 V <sub>CC</sub> (mA)	0.5 V <sub>CC</sub>			
V <sub>OL</sub>	Low-level output voltage	TTL	I <sub>OL</sub> = 8 mA	0.4	V	
			I <sub>OL</sub> = 4 mA	0.4		
	5-V tolerant TTL	I <sub>OL</sub> = 8 mA	0.4			
		I <sub>OL</sub> = 4 mA	0.4			
	3-V PCI	I <sub>OL</sub> = 8 V <sub>CC</sub> (mA)	0.3 V <sub>CC</sub>			
I <sub>IH</sub>	High-level input current	TTL	V <sub>I</sub> = V <sub>IH</sub> (max), See Note 4	±1	μA	
		5-V tolerant TTL	V <sub>I</sub> = V <sub>IH</sub> (min)	–760		
		3-V PCI	V <sub>I</sub> = V <sub>IH</sub> (max), See Note 4	±1		
I <sub>IL</sub>	Low-level input current	TTL	V <sub>I</sub> = V <sub>IL</sub> (min), See Note 5	±1	μA	
		5-V tolerant TTL		±1		
		3-V PCI		±1		
I <sub>OZ</sub>	High-impedance-state output current	TTL		±20	μA	
		5-V tolerant TTL		±20		
		3-V PCI		±20		

NOTES: 4. These specifications apply only when the pulldown terminator is turned off.

5. These specifications apply only when the pullup terminator is turned off.

**PRODUCT PREVIEW**

# TNETA1575 ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

## timing requirements (see Note 7) PCI-bus interface

NO.		MIN	NOM	MAX	UNIT
	$f_{\text{clock}}(\text{PCLK})$ Clock frequency, PCLK $\uparrow$		33		MHz
	$t_{\text{su}}(\text{BUS})$ Setup time, bused signals valid before PCLK $\uparrow$ (see Note 6)	7			ns
	$t_{\text{su}}(\text{PGNT})$ Setup time, $\overline{\text{PGNT}}$ low before PCLK $\uparrow$ (see Note 6)	10			ns
	$t_{\text{su}}(\text{PREQ})$ Setup time, $\overline{\text{PREQ}}$ low before PCLK $\uparrow$ (see Note 6)	12			ns
	$t_{\text{h}}(\text{IN})$ Hold time, inputs valid after PCLK $\uparrow$	0			ns

† The UTOPIA-clock (ATMCLK) frequency cannot be greater than three times the PCI-clock (PCLK) frequency or less than one third the PCI-clock (PCLK) frequency because synchronization can break down on the FIFOs and cells can be lost. If this relationship is maintained between the PCLK clock and the ATMCLK clock, the PCLK clock can operate at or below 33 MHz and cells will not be lost.

NOTES: 6.  $\overline{\text{PREQ}}$  and  $\overline{\text{PGNT}}$  are point-to-point signals, and have different output valid delay and input setup times than do bused signals. PGNT has a setup time of 10 ns;  $\overline{\text{PREQ}}$  has a setup time of 12 ns. All other signals are bused.

7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

## switching characteristics (see Note 7) PCI-bus interface

NO.	PARAMETER	MIN	MAX	UNIT
	$t_{\text{d}}(\text{BUSV})$ Delay time, PCLK $\uparrow$ to bused signals valid (see Note 6)	2	11	ns
	$t_{\text{d}}(\text{PGNT})$ Delay time, PCLK $\uparrow$ to $\overline{\text{PGNT}}$ low (see Note 6)	2	12	ns
	$t_{\text{d}}(\text{PREQ})$ Delay time, PCLK $\uparrow$ to $\overline{\text{PREQ}}$ low (see Note 6)	2	12	ns
	$t_{\text{on}}(\text{FLT-ACT})$ Turn-on time, float to active	2		ns
	$t_{\text{off}}(\text{ACT-FLT})$ Turn-off time, active to float		28	ns
	$t_{\text{on}}(\text{RST})$ Turn-on time, power stable to reset active	1		ms
	$t_{\text{on}}(\text{PCLK-RST})$ Turn-on time, PCLK stable to reset active	100		$\mu\text{s}$
	$t_{\text{off}}(\text{RST-OFF})$ Turn-off time, reset active to output float		40	ns

NOTES: 6.  $\overline{\text{PREQ}}$  and  $\overline{\text{PGNT}}$  are point-to-point signals, and have different output valid delay and input setup times than do bused signals. PGNT has a setup time of 10 ns;  $\overline{\text{PREQ}}$  has a setup time of 12 ns. All other signals are bused.

7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**  
SDNS040A – MAY 1996 – REVISED JUNE 1996

**timing requirements (see Note 7 and Figure 5)**  
**PCI-bus interface**

NO.		MIN	MAX	UNIT
1	$t_w(\text{PCLKH})$ Pulse duration, PCLK high	12		ns
2	$t_w(\text{PCLKL})$ Pulse duration, PCLK low	12		ns
3	$t_{su}(\text{PGNT})$ Setup time, PGNT low before PCLK $\uparrow$	10		ns
4	$t_{su}(\text{PAD})$ Setup time, PAD31 – PAD0 valid before PCLK $\uparrow$	7		ns
5	$t_{su}(\text{PTRDY})$ Setup time, $\overline{\text{PTRDY}}$ low before PCLK $\uparrow$	7		ns
6	$t_{su}(\text{PDEVSEL})$ Setup time, $\overline{\text{PDEVSEL}}$ low before PCLK $\uparrow$	7		ns
7	$t_h(\text{PAD})$ Hold time, PAD31 – PAD0 valid after PCLK $\uparrow$	0		ns
8	$t_h(\text{PTRDY})$ Hold time, $\overline{\text{PTRDY}}$ low after PCLK $\uparrow$	0		ns
9	$t_h(\text{PDEVSEL})$ Hold time, $\overline{\text{PDEVSEL}}$ low after PCLK $\uparrow$	0		ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

**switching characteristics (see Note 7 and Figure 5)**  
**PCI-bus interface**

NO.	PARAMETER	MIN	MAX	UNIT
10	$t_d(\text{PFRAME})$ Delay time, PCLK $\uparrow$ to $\overline{\text{PFRAME}}\downarrow$	2	11	ns
11	$t_d(\text{PAD})$ Delay time, PCLK $\uparrow$ to PAD31 – PAD0 valid	2	11	ns
12	$t_d(\text{PCBE})$ Delay time, PCLK $\uparrow$ to PCBE3 – PCBE0 valid	2	11	ns
13	$t_d(\text{PIRDY})$ Delay time, PCLK $\uparrow$ to $\overline{\text{PIRDY}}\downarrow$	2	11	ns
14	$t_d(\text{PREQ})$ Delay time, PCLK $\uparrow$ to $\overline{\text{PREQ}}\downarrow$	2	12	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

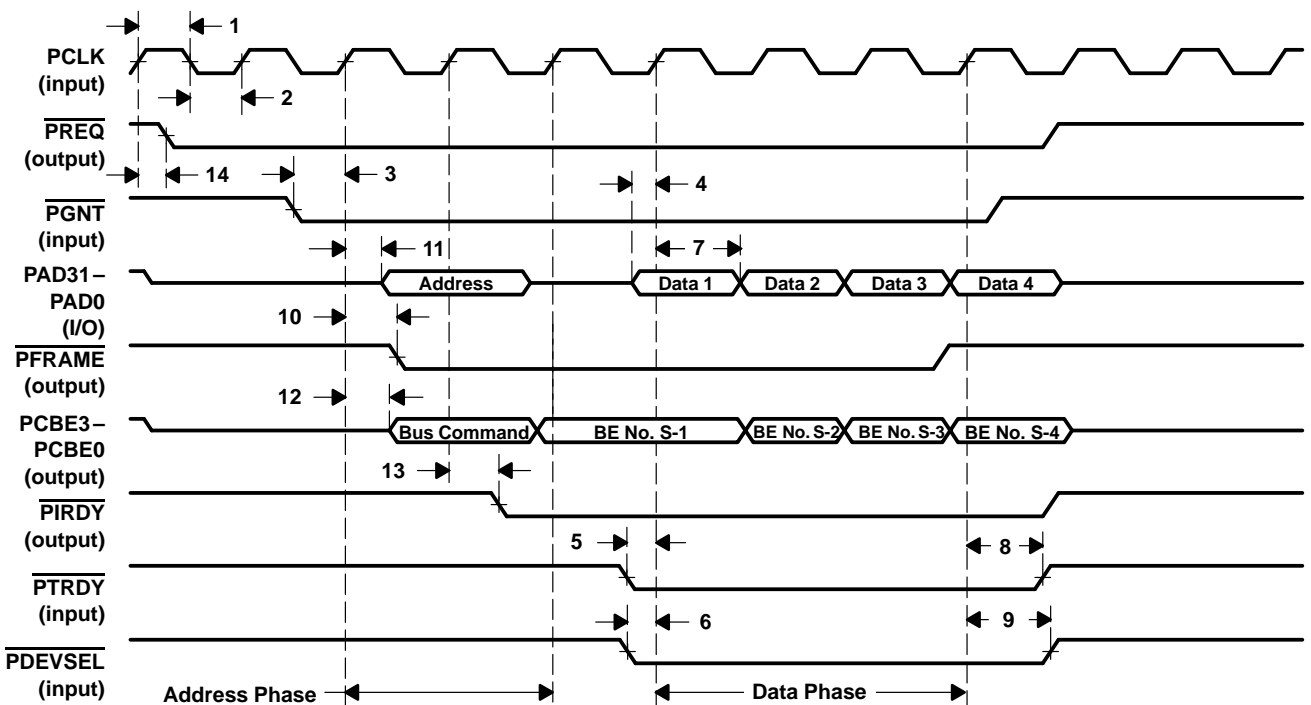


Figure 5. TNETA1575 Read Operation (PCI SAR as Master)

PRODUCT PREVIEW

TNETA1575  
ATM SEGMENTATION AND REASSEMBLY DEVICE  
WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

timing requirements (see Note 7 and Figure 6)  
PCI-bus interface

NO.		MIN	MAX	UNIT
1	$t_{su}(PGNT)$ Setup time, $\overline{PGNT}$ low before $PCLK\uparrow$	10		ns
2	$t_{su}(PTRDY)$ Setup time, $\overline{PTRDY}$ low before $PCLK\uparrow$	7		ns
3	$t_{su}(PDEVSEL)$ Setup time, $\overline{PDEVSEL}$ low before $PCLK\uparrow$	7		ns
4	$t_h(PTRDY)$ Hold time, $\overline{PTRDY}$ low after $PCLK\uparrow$	0		ns
5	$t_h(PDEVSEL)$ Hold time, $\overline{PDEVSEL}$ low after $PCLK\uparrow$	0		ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

PRODUCT PREVIEW



**switching characteristics (see Note 7 and Figure 6)**  
**PCI-bus interface**

NO.	PARAMETER	MIN	MAX	UNIT
6	$t_d(\overline{\text{PREQ}})$ Delay time, PCLK↑ to $\overline{\text{PREQ}}\downarrow$	2	12	ns
7	$t_d(\overline{\text{PFRAME}})$ Delay time, PCLK↑ to $\overline{\text{PFRAME}}\downarrow$	2	11	ns
8	$t_d(\overline{\text{PCBE}})$ Delay time, PCLK↑ to $\overline{\text{PCBE}}$ valid	2	11	ns
9	$t_d(\overline{\text{PIRDY}})$ Delay time, PCLK↑ to $\overline{\text{PIRDY}}\downarrow$	2	11	ns
10	$t_d(\overline{\text{PAD}})$ Delay time, PCLK↑ to PAD31 – PAD0 valid	2	11	ns
11	$t_d(\overline{\text{PSB}})$ Delay time, PCLK↑ to PSB1 – PSB0 valid	2	11	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

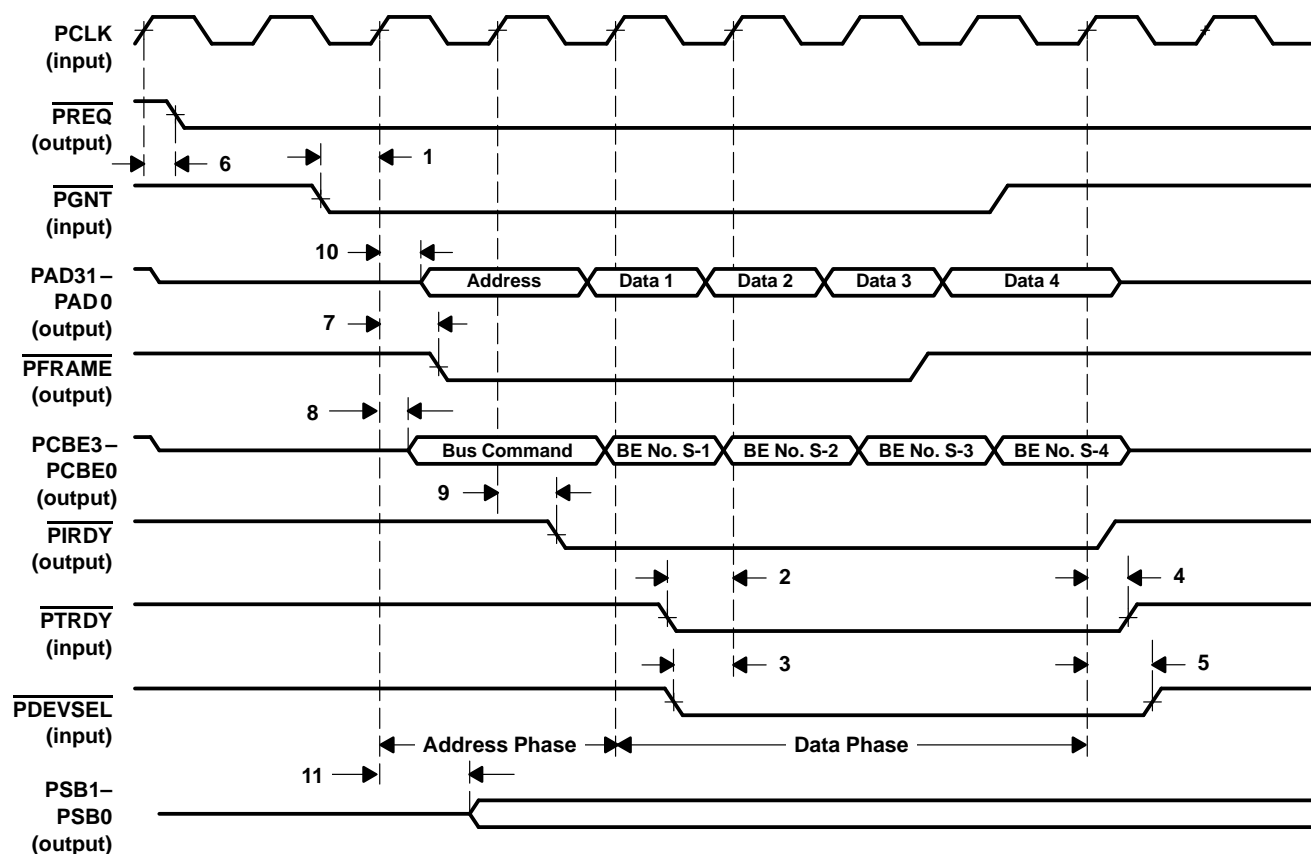


Figure 6. TNETA1575 Write Operation (PCI SAR as Master)

PRODUCT PREVIEW

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**  
SDNS040A – MAY 1996 – REVISED JUNE 1996

**timing requirements (see Note 7 and Figure 7)**  
**PCI-bus interface**

NO.		MIN	MAX	UNIT
1	$t_{su}(PIDSEL)$ Setup time, $PIDSEL$ high before $PCLK\uparrow$	7		ns
2	$t_{su}(PAD)$ Setup time, $PAD31-PAD0$ valid before $PCLK\uparrow$	7		ns
3	$t_{su}(PCBE)$ Setup time, $PCBE3-PCBE0$ valid before $PCLK\uparrow$	7		ns
4	$t_{su}(PIRDY)$ Setup time, $\overline{PIRDY}$ low before $PCLK\uparrow$	7		ns
5	$t_h(PIDSEL)$ Hold time, $PIDSEL$ high after $PCLK\uparrow$	0		ns
6	$t_h(PAD)$ Hold time, $PAD31-PAD0$ valid after $PCLK\uparrow$	0		ns
7	$t_h(PCBE)$ Hold time, $PCBE3-PCBE0$ valid after $PCLK\uparrow$	0		ns
8	$t_h(PIRDY)$ Hold time, $\overline{PIRDY}$ low after $PCLK\uparrow$	0		ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

**switching characteristics (see Note 7 and Figure 7)**  
**PCI-bus interface**

NO.	PARAMETER	MIN	MAX	UNIT
9	$t_d(PAD)$ Delay time, $PCLK\uparrow$ to $PAD31-PAD0$ valid	2	11	ns
10	$t_d(PTRDY)$ Delay time, $PCLK\uparrow$ to $PTRDY\downarrow$	2	11	ns
11	$t_d(PDEVSEL)$ Delay time, $PCLK\uparrow$ to $\overline{PDEVSEL}\downarrow$	2	11	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

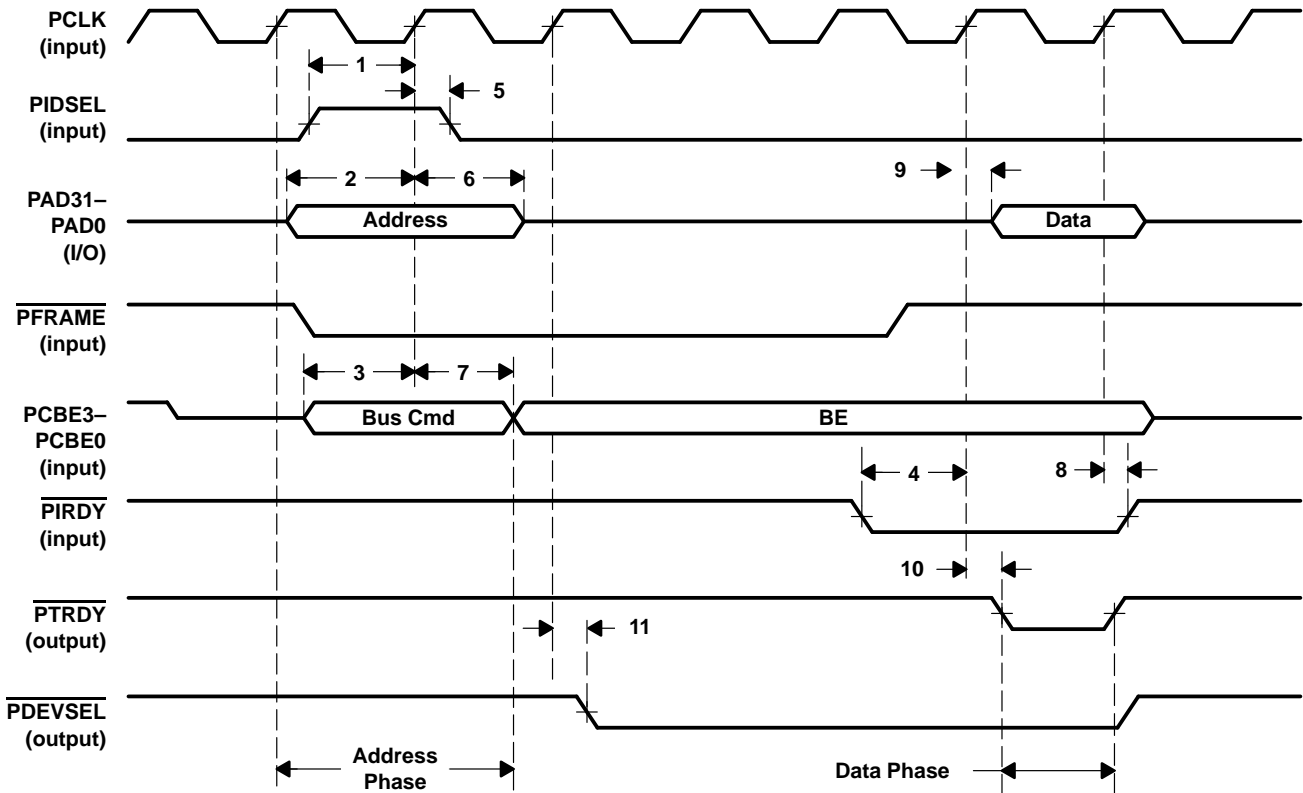


Figure 7. TNETA1575 Read Operation (PCI SAR as Slave)

**timing requirements (see Note 7 and Figure 8)**  
**PCI-bus interface**

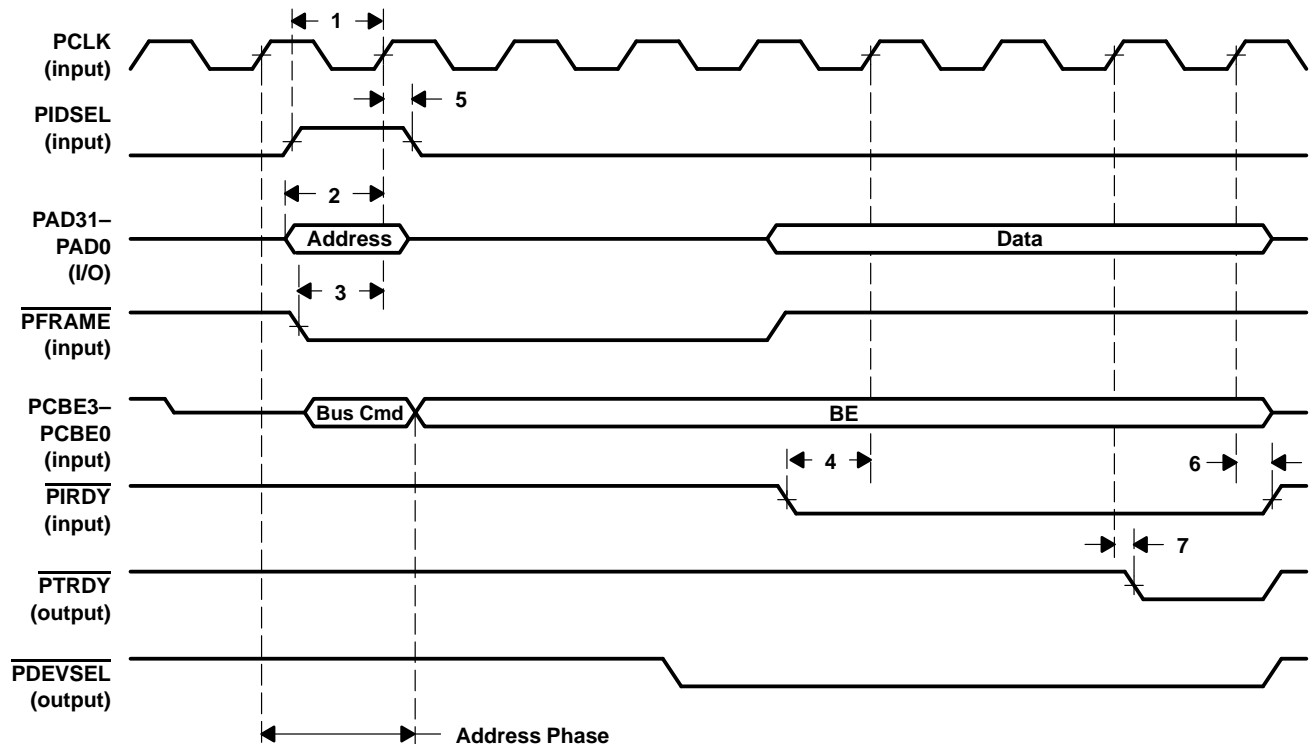
NO.		MIN	MAX	UNIT
1	$t_{su}(PIDSEL)$ Setup time, $PIDSEL$ high before $PCLK\uparrow$	7		ns
2	$t_{su}(PAD)$ Setup time, $PAD31-PAD0$ valid before $PCLK\uparrow$	7		ns
3	$t_{su}(PFRAME)$ Setup time, $\overline{PFRAME}$ low before $PCLK\uparrow$	7		ns
4	$t_{su}(PIRDY)$ Setup time, $\overline{PIRDY}$ low before $PCLK\uparrow$	7		ns
5	$t_h(PIDSEL)$ Hold time, $PIDSEL$ high after $PCLK\uparrow$	0		ns
6	$t_h(PIRDY)$ Hold time, $\overline{PIRDY}$ low after $PCLK\uparrow$	0		ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

**switching characteristics (see Note 7 and Figure 8)**  
**PCI-bus interface**

NO.	PARAMETER	MIN	MAX	UNIT
7	$t_d(PTRDY)$ Delay time, $PCLK\uparrow$ to $PTRDY\downarrow$	2	11	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.



**Figure 8. TNETA1575 Write Operation (PCI SAR as Slave)**

PRODUCT PREVIEW

TNETA1575

ATM SEGMENTATION AND REASSEMBLY DEVICE

WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

switching characteristics (see Note 7 and Figure 9)  
PCI sideband

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_d(\text{PAD})$ Delay time, PCLK high to PAD31–PAD0 valid	2	11	ns
2	$t_d(\text{PSB})$ Delay time, PCLK high to PSB1–0 valid	2	11	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

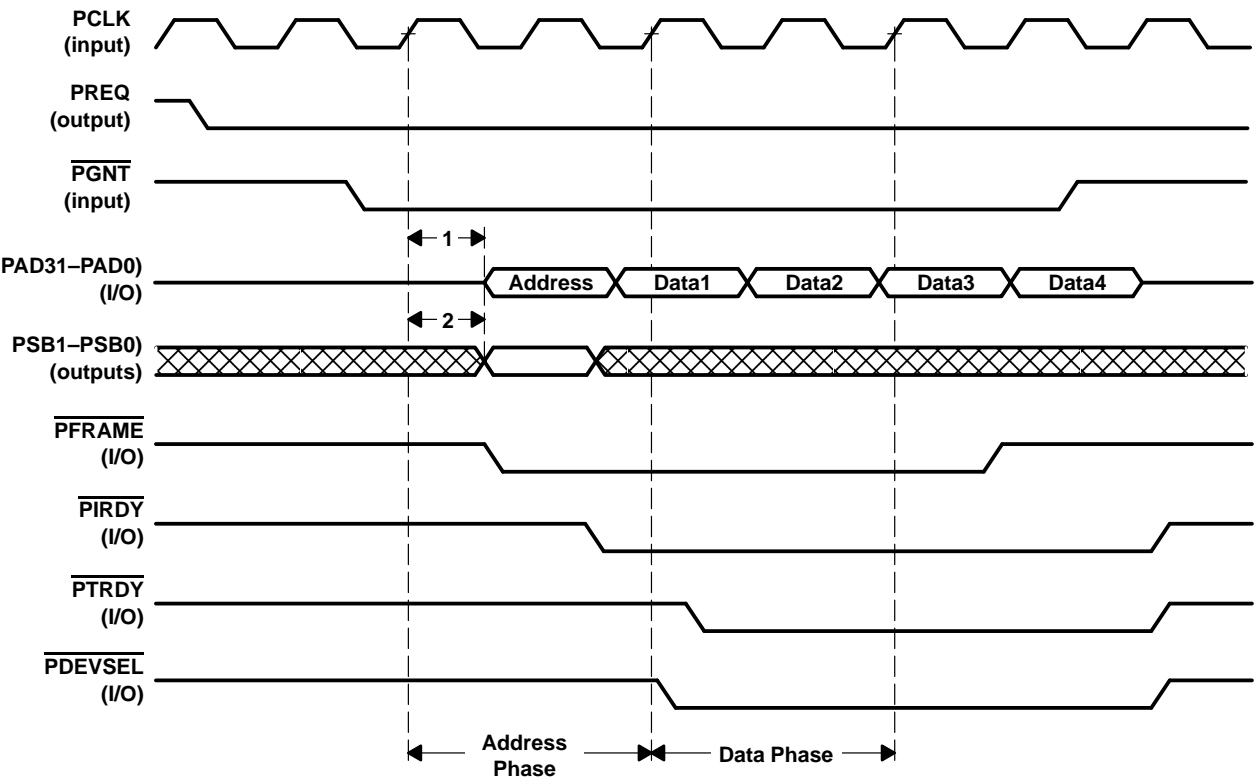


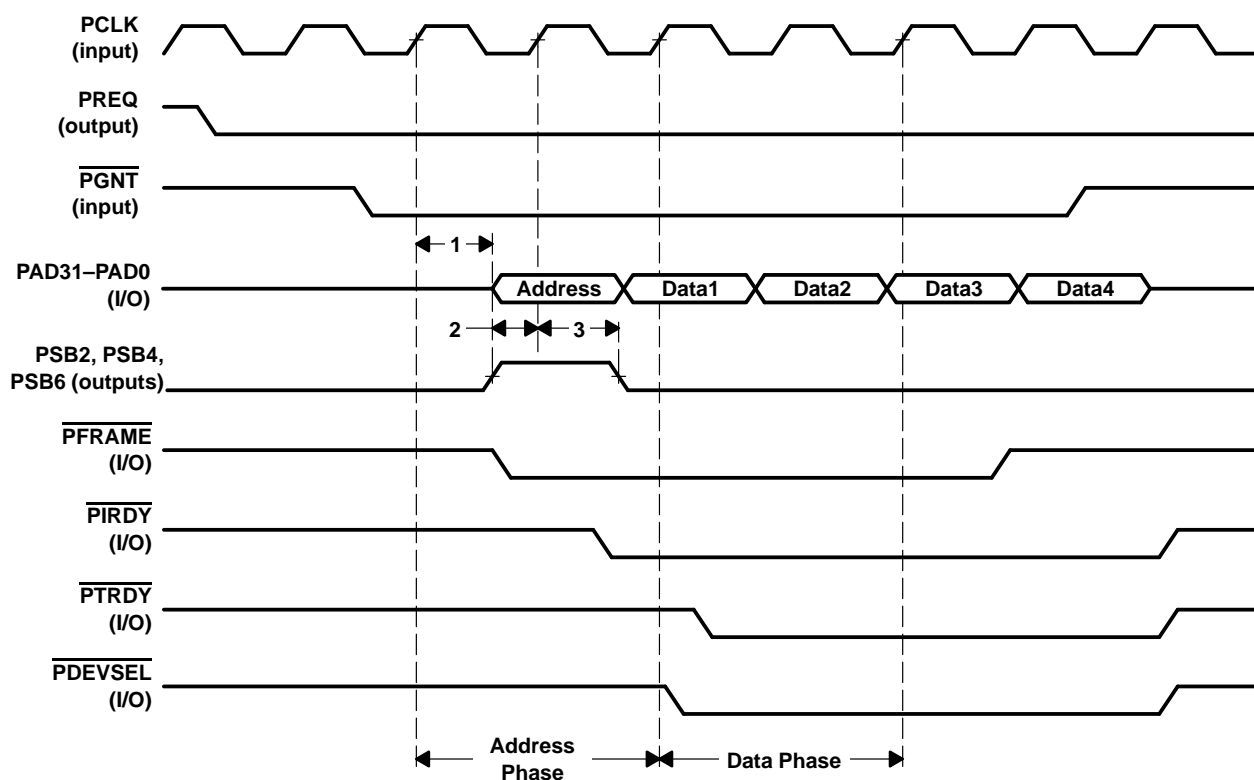
Figure 9. TNETA1575 Master Write Operation and PCI-Sideband (PSB1–PSB0 Signals) Timing

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**  
SDNS040A – MAY 1996 – REVISED JUNE 1996

**timing requirements (see Note 7 and Figure 10)**  
**PCI sideband**

NO.		MIN	MAX	UNIT
1	$t_d(\text{PAD})$ Delay time, PCLK high to PAD31–PAD0 valid	2	11	ns
2	$t_{su}(\text{PSB2})$ Setup time, PSB2 high before PCLK↑	7		ns
2	$t_{su}(\text{PSB4})$ Setup time, PSB4 high before PCLK↑	7		ns
2	$t_{su}(\text{PSB6})$ Setup time, PSB6 high before PCLK↑	7		ns
3	$t_h(\text{PSB2})$ Hold time, PSB2 high after PCLK↑	0		ns
3	$t_h(\text{PSB4})$ Hold time, PSB4 high after PCLK↑	0		ns
3	$t_h(\text{PSB6})$ Hold time, PSB6 high after PCLK↑	0		ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.



**Figure 10. TNETA1575 Master Write Operation and PCI Sideband (PSB2, PSB4, and PSB6 Signals) Timing**

**PRODUCT PREVIEW**

TNETA1575  
ATM SEGMENTATION AND REASSEMBLY DEVICE  
WITH PCI-HOST AND COPROCESSOR INTERFACES  
SDNS040A – MAY 1996 – REVISED JUNE 1996

switching characteristics (see Note 7 and Figure 11)  
PCI bus (TXQUERDY)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_d(\text{TXQUERDY})$ Delay time, PCLK high to TXQUERDY inactive		15	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

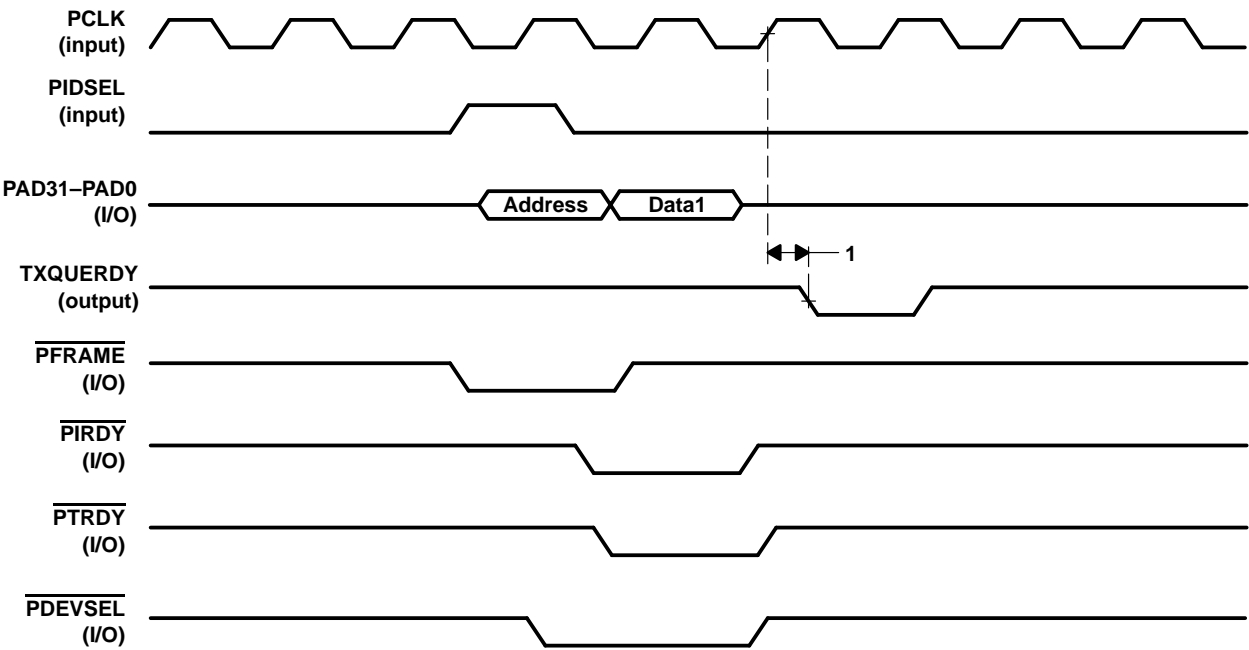
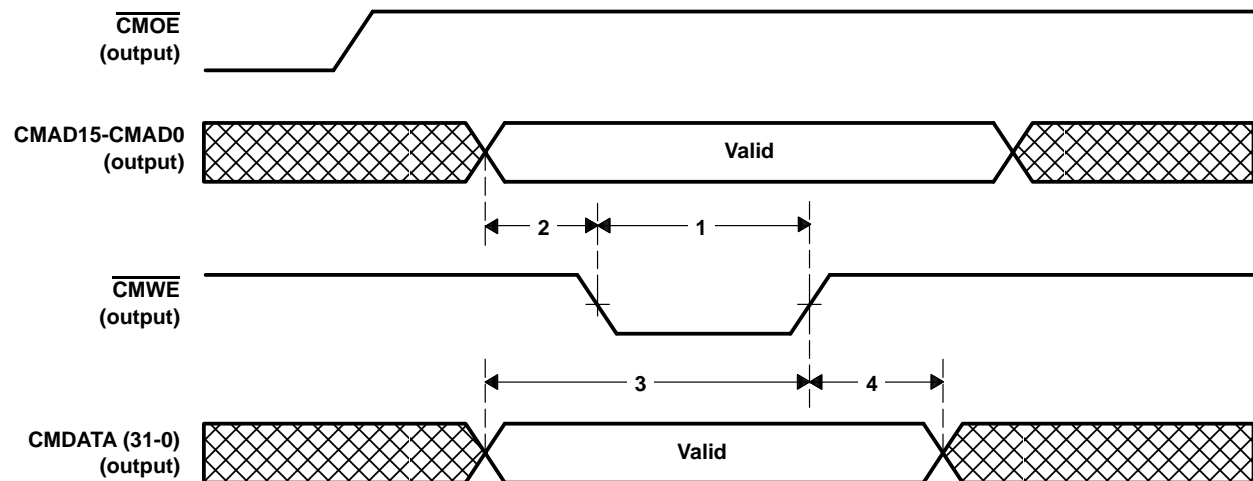


Figure 11. TNETA1575 Write Operation to the TXQUERDY Register and Timing  
(TXQUERDY Going Inactive)

**switching characteristics (see Note 7 and Figure 12)**  
**control-memory interface**

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_w(\overline{\text{CMWE}})$ Pulse duration, $\overline{\text{CMWE}}$ low	28	31	ns
2	$t_d(\overline{\text{CMWE}})1$ Delay time, CMAD15–CMAD0 valid to $\overline{\text{CMWE}}\downarrow$	12	15	ns
3	$t_d(\overline{\text{CMWE}})2$ Delay time, CMDATA31–CMDATA0 valid to $\overline{\text{CMWE}}\uparrow$	10	14	ns
4	$t_d(\text{CMDATA})$ Delay time, $\overline{\text{CMWE}}\uparrow$ to CMDATA31–CMDATA0 invalid	15	19	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.



**Figure 12. TNETA1575 Control-Memory Interface Write Operation**

TNETA1575  
ATM SEGMENTATION AND REASSEMBLY DEVICE  
WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

switching characteristics (see Note 7 and Figure 13)  
control-memory interface

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{su}(\text{CMDATA})$ Setup time, CMDATA31–CMDATA0 valid before $\overline{\text{CMOE}}\uparrow$	10		ns
2	$t_h(\text{CMDATA})$ Hold time, CMDATA31–CMDATA0 valid after $\overline{\text{CMOE}}\uparrow$	0		ns
3	$t_d(\text{CMOE})$ Delay time, CMAD15–CMAD0 valid to $\overline{\text{CMOE}}\downarrow$		3	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

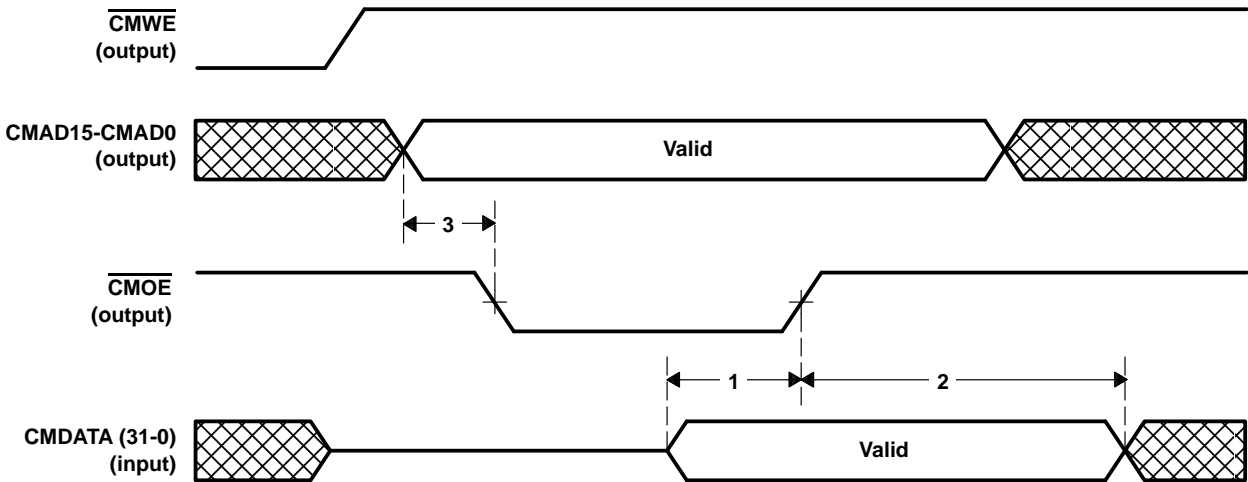


Figure 13. TNETA1575 Control-Memory Interface Read Operation

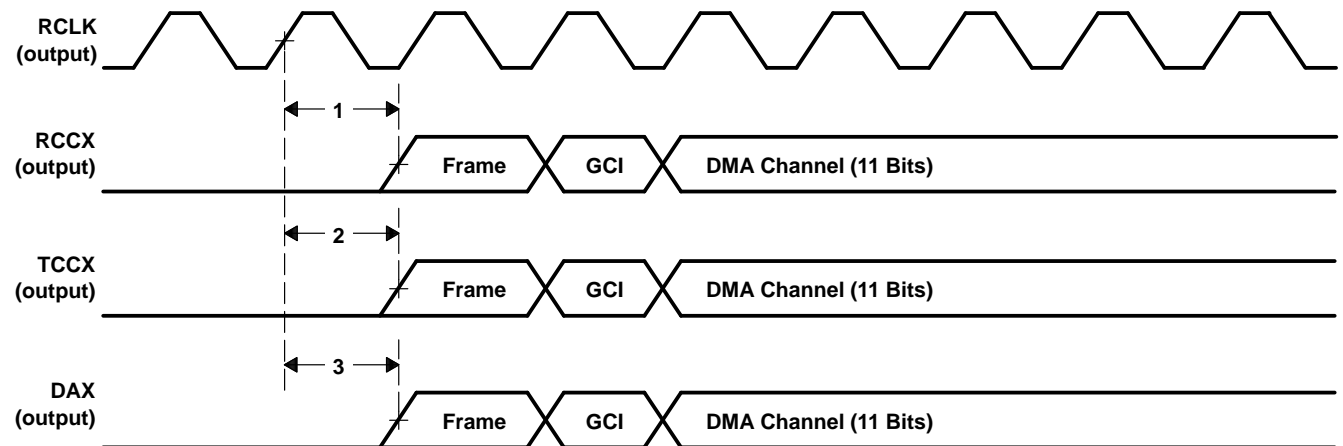
PRODUCT PREVIEW



**switching characteristics (see Note 7 and Figure 14 )  
 traffic coprocessor interface**

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_d(\text{RCCX})$ Delay time, PCLK $\uparrow$ to RCCX valid	2	11	ns
2	$t_d(\text{TCCX})$ Delay time, PCLK $\uparrow$ to TCCX valid	2	11	ns
3	$t_d(\text{DAX})$ Delay time, PCLK $\uparrow$ to DAX valid	2	11	ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

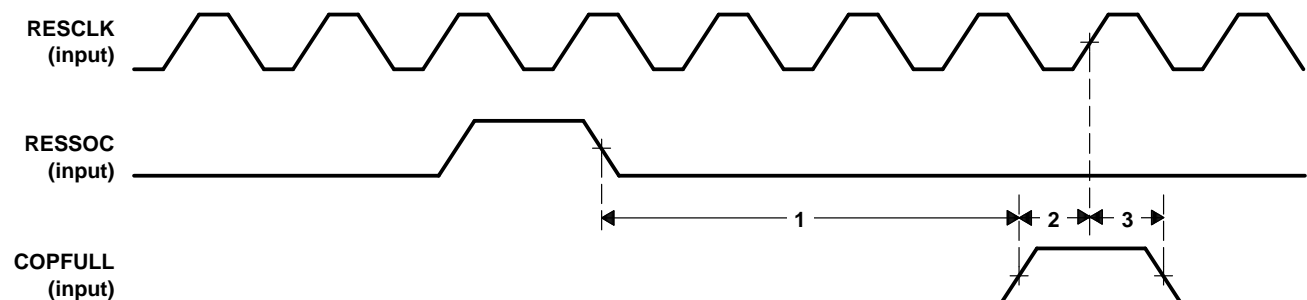


**Figure 14. Traffic Coprocessor Interface Outputs**

**timing requirements (see Note 7 and Figure 15)  
 traffic coprocessor interface**

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_d(\text{COPFULL})$ Delay time, RESSOC $\downarrow$ to COPFULL $\uparrow$	8	40	ns
2	$t_{su}(\text{COPFULL})$ Setup time, COPFULL high before RESCLK $\uparrow$	10		ns
3	$t_h(\text{COPFULL})$ Hold time, COPFULL high after RESCLK $\uparrow$	1		ns

NOTE 7: All timing requirements and switching characteristic values are preliminary and subject to change upon production release.



**Figure 15. Traffic Coprocessor Interface Inputs**

**TNETA1575**  
**ATM SEGMENTATION AND REASSEMBLY DEVICE**  
**WITH PCI-HOST AND COPROCESSOR INTERFACES**  
SDNS040A – MAY 1996 – REVISED JUNE 1996

**timing requirements (see Notes 7 and 8, and Figure 16)**  
**UTOPIA interface**

NO.		MIN	MAX	UNIT
	$f_{\text{clock}}(\text{ACLK})$ Clock frequency, $\text{ATMCLK}\uparrow$	$0.33 f_{\text{clock}}(\text{PCLK})$	$3 f_{\text{clock}}(\text{PCLK})$	MHz
1	$t_w(\text{SEGCLKH})$ Pulse duration, SEGCLK high	12		ns
2	$t_w(\text{SEGCLKL})$ Pulse duration, SEGCLK low	12		ns
3	$t_{su}(\text{SEGEN})$ Setup time, $\overline{\text{SEGEN}}$ low before $\text{SEGCLK}\uparrow$	10		ns
4	$t_h(\text{SEGEN})$ Hold time, $\overline{\text{SEGEN}}$ low after $\text{SEGCLK}\uparrow$	1		ns

† The UTOPIA-clock (ATMCLK) frequency cannot be greater than three times the PCI-clock (PCLK) frequency or less than one third the PCI-clock (PCLK) frequency because synchronization can break down on the FIFOs and cells can be lost. If this relationship is maintained between the PCLK clock and the ATMCLK clock, the PCLK clock can operate at or below 33 MHz and cells will not be lost.

- NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
8. All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

**switching characteristics (see Notes 7 and 8, and Figure 16)**  
**UTOPIA interface**

NO.	PARAMETER	MIN	MAX	UNIT
5	$t_d(\text{SEGCLAV})$ Delay time, $\text{SEGCLK}\uparrow$ to $\text{SEGCLAV}\downarrow$	1	20	ns
6	$t_d(\text{SEGSOC})$ Delay time, $\text{SEGCLK}\uparrow$ to $\text{SEGSOC}\uparrow$	1	20	ns
7	$t_d(\text{SEGDATA})$ Delay time, $\text{SEGCLK}\uparrow$ to SEGDATA7–SEGDATA0 valid	1	20	ns
8	$t_d(\text{SEGPARG})$ Delay time, $\text{SEGCLK}\uparrow$ to SEGPARG valid	1	20	ns

- NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
8. All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

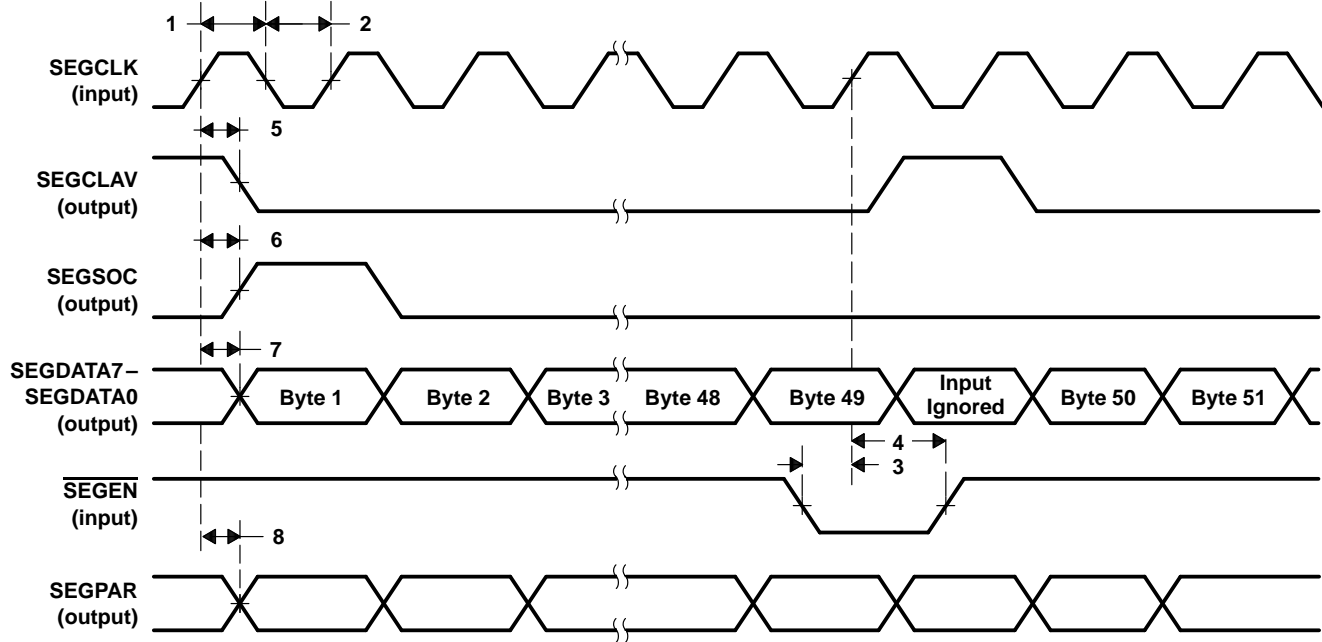


Figure 16. Segmentation-Cell Interface (PHY/ATM Low)

**timing requirements (see Notes 7 and 8, and Figure 17)**  
**UTOPIA interface**

NO.		MIN	MAX	UNIT
1	$t_w(\text{SEGCLKH})$ Pulse duration, SEGCLK high	10		ns
2	$t_w(\text{SEGCLKL})$ Pulse duration, SEGCLK low	10		ns
3	$t_{su}(\text{SEGEN})$ Setup time, $\overline{\text{SEGEN}}$ high before SEGCLK $\uparrow$	10		ns
4	$t_h(\text{SEGEN})$ Hold time, $\overline{\text{SEGEN}}$ high after SEGCLK $\uparrow$	1		ns

NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
8. All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

**switching characteristics (see Notes 7 and 8, and Figure 17)**  
**UTOPIA interface**

NO.	PARAMETER	MIN	MAX	UNIT
5	$t_d(\text{SEGSOC})$ Delay time, SEGCLK $\uparrow$ to SEGSOC $\uparrow$	1	20	ns
6	$t_d(\text{SEGDATA})$ Delay time, SEGCLK $\uparrow$ to SEGDATA7–SEGDATA0 valid	1	20	ns
7	$t_d(\text{SEGPARG})$ Delay time, SEGCLK $\uparrow$ to SEGPARG $\uparrow$	1	20	ns
8	$t_d(\text{SEGCLAV})_1$ Delay time, SEGCLK $\uparrow$ to SEGCLAV $\uparrow$	1	20	ns
9	$t_d(\text{SEGCLAV})_2$ Delay time, SEGCLK $\uparrow$ to SEGCLAV $\downarrow$	1	20	ns

NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
8. All output signals are generated on the rising edge of SEGCLK. All inputs are sampled on the rising edge of SEGCLK.

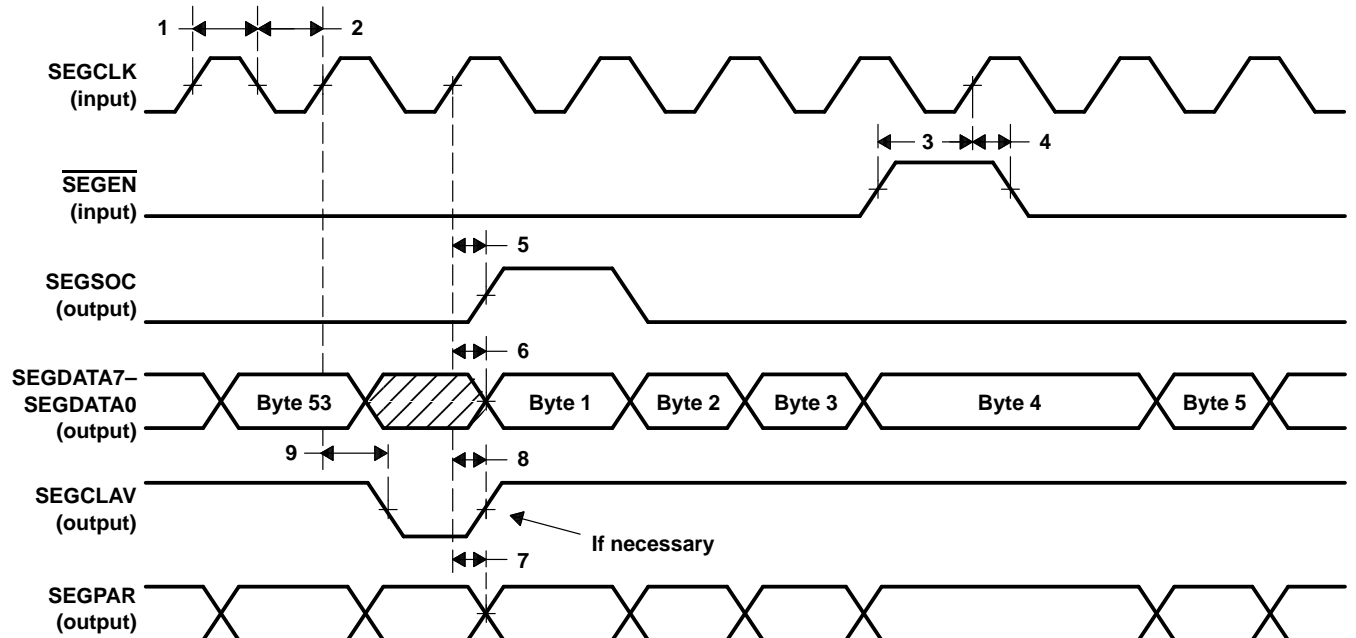


Figure 17. Segmentation-Cell Interface (PHY/ATM High)

TNETA1575

ATM SEGMENTATION AND REASSEMBLY DEVICE

WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

timing requirements (see Notes 7 and 9, and Figure 18)

UTOPIA interface

NO.		MIN	MAX	UNIT
1	t <sub>w</sub> (RESCLKH) Pulse duration, RESCLK high	12		ns
2	t <sub>w</sub> (RESCLKL) Pulse duration, RESCLK low	12		ns
3	t <sub>su</sub> (RESSOC) Setup time, RESSOC high before RESCLK↑	10		ns
4	t <sub>su</sub> (RESEN) Setup time, $\overline{\text{RESEN}}$ low before RESCLK↑	10		ns
5	t <sub>su</sub> (RESDATA) Setup time, RESDATA7–RESDATA0 valid before RESCLK↑	10		ns
6	t <sub>su</sub> (RESPAR) Setup time, RESPAR valid before RESCLK↑	10		ns
7	t <sub>h</sub> (RESSOC) Hold time, RESSOC high after RESCLK↑	1		ns
8	t <sub>h</sub> (RESEN) Hold time, $\overline{\text{RESEN}}$ low after RESCLK↑	1		ns

NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.

9. All output signals are generated on the rising edge of RESCLK.

PRODUCT PREVIEW

**switching characteristics (see Notes 7 and 9, and Figure 18)**  
**UTOPIA interface**

NO.	PARAMETER	MIN	MAX	UNIT
9	$t_d(\text{RESCLAV})$ Delay time, RESCLK $\uparrow$ to RESCLAV $\uparrow$	1	20	ns
10	$t_d(\text{RESPERR})_1$ Delay time, RESCLK $\uparrow$ to $\overline{\text{RESPERR}}\downarrow$	1	20	ns
11	$t_d(\text{RESPERR})_2$ Delay time, RESCLK $\uparrow$ to $\overline{\text{RESPERR}}\uparrow$	1	20	ns

NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
9. All output signals are generated on the rising edge of RESCLK.

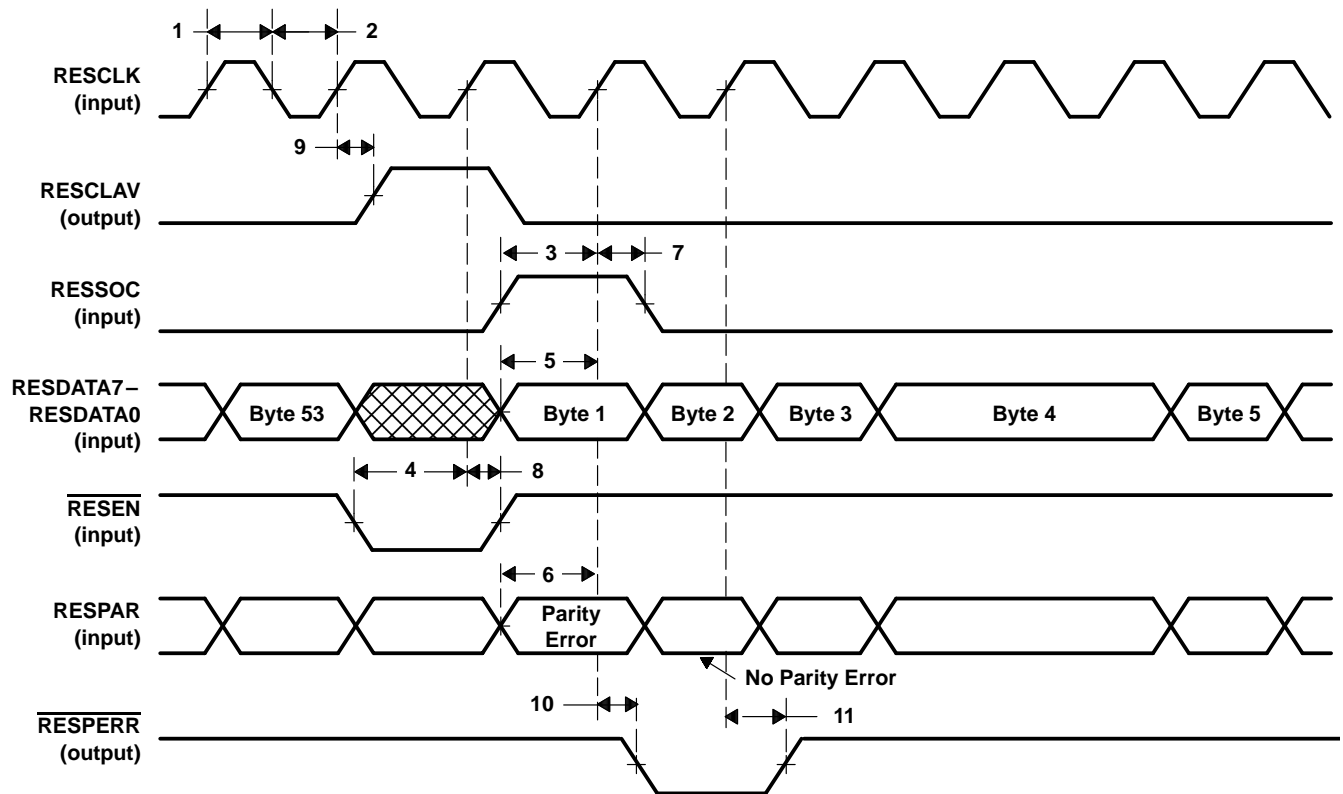


Figure 18. Reassembly-Cell Interface (PHY/ATM Low)

TNETA1575  
ATM SEGMENTATION AND REASSEMBLY DEVICE  
WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

timing requirements (see Notes 7 and 10, and Figure 19)  
UTOPIA interface

NO.		MIN	MAX	UNIT
1	t <sub>w</sub> (RESCLKH) Pulse duration, RESCLK high	10		ns
2	t <sub>w</sub> (RESCLKL) Pulse duration, RESCLK low	10		ns
3	t <sub>su</sub> (RESEN) Setup time, $\overline{\text{RESEN}}$ high before RESCLK $\uparrow$	10		ns
4	t <sub>su</sub> (RESSOC) Setup time, RESSOC high before RESCLK $\uparrow$	10		ns
5	t <sub>su</sub> (RESDATA) Setup time, RESDATA7–RESDATA0 valid before RESCLK $\uparrow$	10		ns
6	t <sub>su</sub> (RESPAR) Setup time, RESPAR valid before RESCLK $\uparrow$	10		ns
7	t <sub>h</sub> (RESEN) Hold time, $\overline{\text{RESEN}}$ high after RESCLK $\uparrow$	1		ns
8	t <sub>h</sub> (RESSOC) Hold time, RESSOC high after RESCLK $\uparrow$	1		ns
9	t <sub>h</sub> (RESDATA) Hold time, RESDATA7–RESDATA0 valid after RESCLK $\uparrow$	1		ns
10	t <sub>h</sub> (RESPAR) Hold time, RESPAR valid after RESCLK $\uparrow$	1		ns

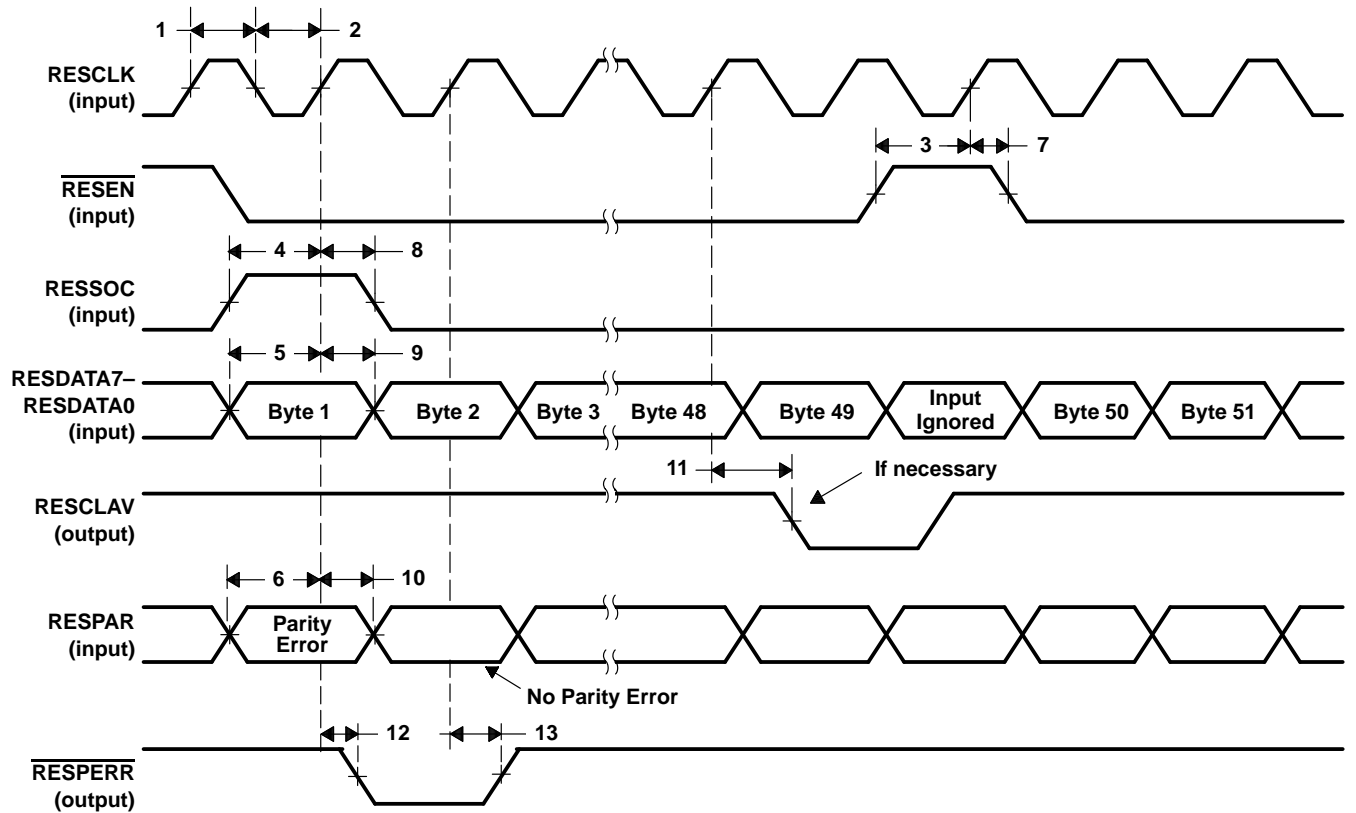
NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
10. All output signals are generated on the rising edge of RESCLK. All input signals are sampled on the rising edge of RESCLK.

PRODUCT PREVIEW

**switching characteristics (see Notes 7 and 10, and Figure 19)**  
**UTOPIA interface**

NO.	PARAMETER	MIN	MAX	UNIT
11	$t_d(\text{RESCLAV})$ Delay time, RESCLK $\uparrow$ to RESCLAV $\downarrow$	1	20	ns
12	$t_d(\text{RESPERR})_1$ Delay time, RESCLK $\uparrow$ to $\overline{\text{RESPERR}}\downarrow$	1	20	ns
13	$t_d(\text{RESPERR})_2$ Delay time, RESCLK $\uparrow$ to $\overline{\text{RESPERR}}\uparrow$	1	20	ns

NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
10. All output signals are generated on the rising edge of RESCLK. All input signals are sampled on the rising edge of RESCLK.



**Figure 19. Reassembly-Cell Interface (PHY/ATM High)**

TNETA1575  
ATM SEGMENTATION AND REASSEMBLY DEVICE  
WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

switching characteristics (see Notes 7 and 11, and Figure 20)  
local-bus interface

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_d(\overline{\text{LBCS1}})_1$ Delay time, $\overline{\text{LBR}}/\overline{\text{W}}\uparrow$ to $\overline{\text{LBCS1}}\downarrow$			ns
2	$t_d(\overline{\text{LBREADY}})$ Delay time, $\overline{\text{LBREADY}}\downarrow$ to $\overline{\text{LBCS1}}\uparrow$			ns

- NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
11. If  $\overline{\text{LBREADY}}$  does not go low within 8 PCI-clock cycles after  $\overline{\text{LBCS1}}$  goes active low, TNETA1575 latches in the data of the  $\text{LBDATA7-LBDATA0}$  bus and terminates the read operation.

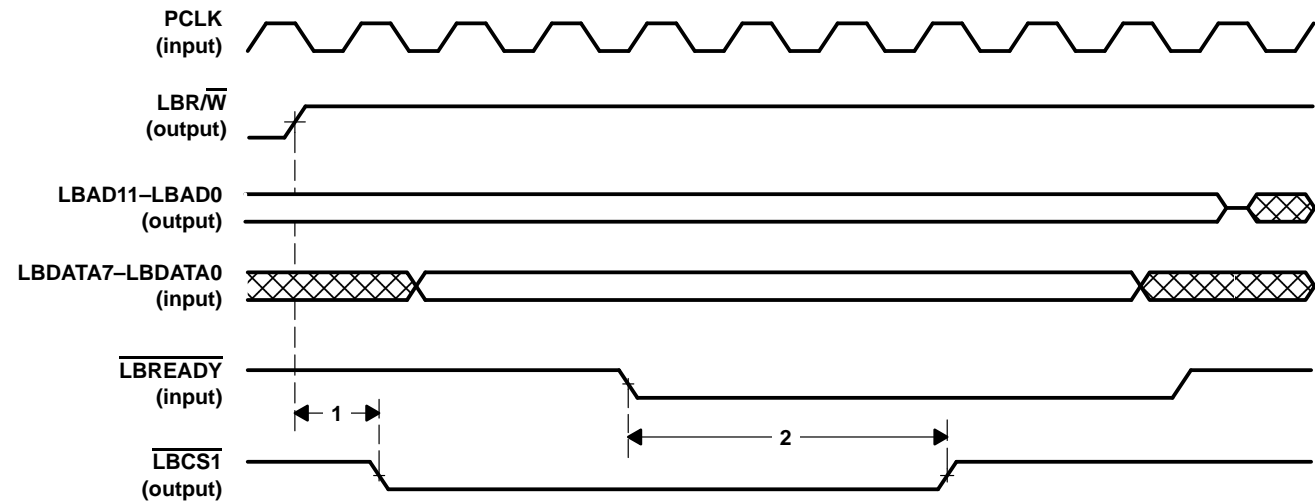


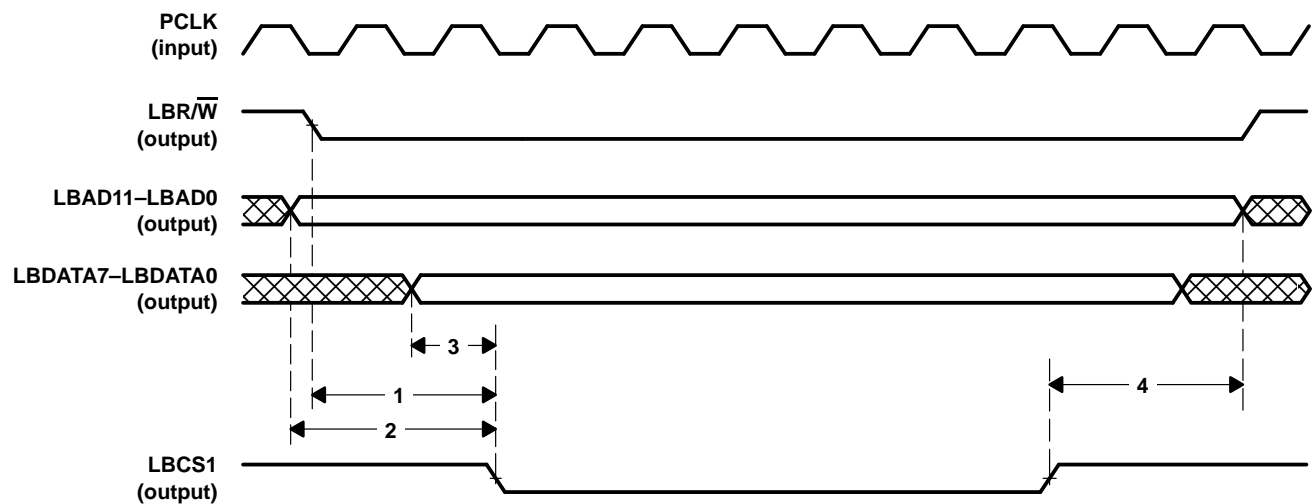
Figure 20. Local-Bus Interface (Read Operation)



**switching characteristics (see Notes 7 and 12, and Figure 21)**  
**local-bus interface**

NO.		MIN	MAX	UNIT
1	$t_d(\text{LBCS1})_1$ Delay time, $\text{LBR}/\overline{\text{W}}\downarrow$ to $\text{LBCS1}\downarrow$			ns
2	$t_d(\text{LBCS1})_2$ Delay time, $\text{LBAD}11\text{--}\text{LBAD}0$ valid to $\text{LBCS1}\downarrow$			ns
3	$t_d(\text{LBCS1})_3$ Delay time, $\text{LBDA}7\text{--}\text{LBDA}0$ valid to $\text{LBCS1}\downarrow$			ns
4	$t_d(\text{LBAD})$ Delay time, $\text{LBCS1}\uparrow$ to $\text{LBAD}11\text{--}\text{LBAD}0$ invalid			ns

NOTES: 7. All timing requirements and switching characteristic values are preliminary and subject to change upon production release.  
12. The LBCS1 is asserted low for 8 PCI-clock cycles during a write operation to allow access to slow devices.



**Figure 21. Local-Bus Interface (Write Operation)**

# TNETA1575 ATM SEGMENTATION AND REASSEMBLY DEVICE WITH PCI-HOST AND COPROCESSOR INTERFACES

SDNS040A – MAY 1996 – REVISED JUNE 1996

## APPLICATIONS INFORMATION

### introduction

The TNETA1575 implements a range of features targeted for cell-switching enterprise hubs. The growth in acceptance of ATM in the backbone transfers quickly to the backplane (the collapsed backbone). The TNETA1575 is also suited for lower-cost applications such as stackable hubs. The growth in acceptance of ATM in the backbone can lead to an increase in demand for ATM connectivity in the installed base of stackable classical-LAN switching products.

To support these applications, a different SAR architecture is required that includes the following characteristics:

- Cell interface that can go beyond 155-Mbit/s transfer rates. This increases the number of front-end legacy interfaces that can be supported by a single SAR device.
- Direct support for constant-bit-rate (CBR) traffic via a dedicated input, a scheduling mechanism and priority-queue scheme make isochronous services available to enterprise hubs, video servers, and to stackable hubs, enabling the delivery of real-time services to the desktop via dedicated classical-LAN connections.
- Support for the full range of virtual paths and virtual channels, and 2K-ABR channels that are required to enable the deployment of large and scaleable virtual LANs
- Support for an internal scheduler. The COPI is used to interface to an external scheduler, which would provide support for all the ATM classes of service.
- High-performance features. On the transmit side, these include the transmit-channel sleep mode, which prevents polling of transmit channels with no data queued. On the receive side, these include features that utilize PCI-bus sideband signals to eliminate polling across the PCI bus completely.
- Early segmentation. This is very important to systems that require reduced latency (isochronous hubs). Early segmentation enables multimedia applications to take full advantage of ATM facilities.
- Support for the full range of virtual paths and virtual channels. This is a requirement for the collapsed backbones that are a part of virtual LANs, and the feature offers support for multimedia applications.
- An option to program the UTOPIA-cell interface as either a PHY or ATM-layer system. This option provides the TNETA1575 a capability to function as a PHY where the cell switch is distributed or as an ATM-layer interface for adapter cards or ATM uplinks.

### system-level overview

The TNETA1575 and the TNETA1585 provide a flexible, high-performance solution that implements the ATM forum's available-bit-rate (ABR) service category, as specified in the ATM-forum traffic management 4.0 interoperability specification. A summary of these two devices follows:

#### TNETA1575 HyperSAR-PLUS

The TNETA1575 is a SAR engine based on TI's TNETA1570 architecture. Its primary interfaces are:

- 32-bit PCI for host transfers
- UTOPIA for cell transfers
- COPI for traffic-COP flow-control management
- Control memory for status information
- Local-bus interface for accessing the PHY device via the SAR

## APPLICATIONS INFORMATION

### system-level overview (continued)

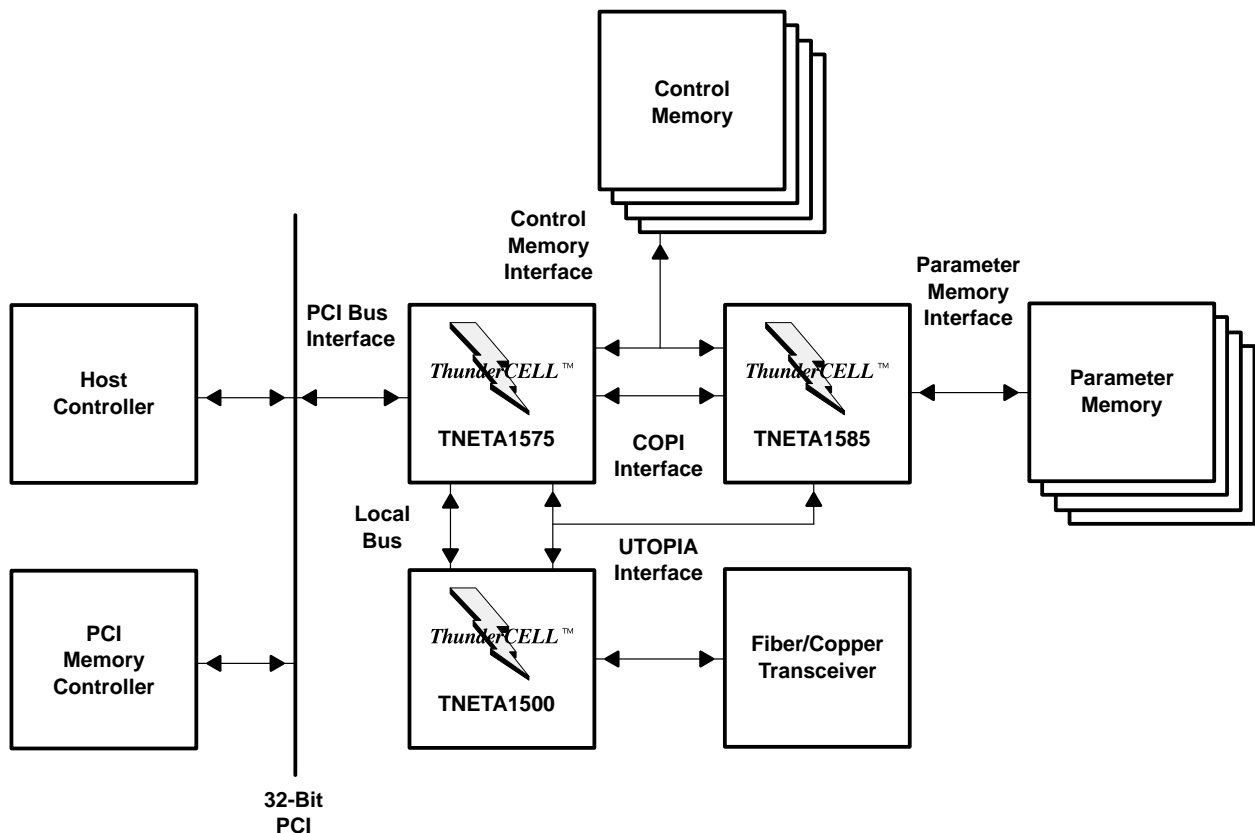
The TNETA1575 has the following internal FIFO capabilities:

- A transmit FIFO for internal interfacing between the segmentation engine and the cell transmit block. The TX FIFO holds 4 cells.
- A receive FIFO for internal interfacing between the reassembly engine and the cell receive block. The RX FIFO holds 32 cells.

### TNETA1585 traffic coprocessor<sup>†</sup>

The TNETA1585 is an ABR scheduler that conforms to the ATM-forum's interoperability specifications. Other than scheduling cells, the primary function is to handle the processing of resource management (RM) cells in both the transmit and receive directions.

A system-level interconnect of the chip set, with associated systems, is shown in Figure 22.



**Figure 22. System-Level Chip Set (TNETA1575, TNETA1585, and TNETA1500)**

<sup>†</sup> Vendors can develop their own second-tier schedulers, which conform to the coprocessor interface as defined in this specification, in advance of the availability of the TNETA1585 device.

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.