

- Provides SONET Interface to Any Type of Payload
- Programmable STS-1 or STS-N Modes
- Receives Bit-Serial STS-1 Signals to Line Side Using External Reference Frame-Pulse Input for STS-N Applications
- Transmits Bit-Serial STS-1 Signals From Line Side Using External Reference Frame Pulse for Outgoing Phase Synchronization
- Transmits Bit-Serial STS-1 Signals From Line Side Using External Reference Frame Pulse for Outgoing Phase Synchronization
- Programmable Full STS-1 or SPE-Only I/O on Terminal Side
- Bit-Serial or Byte-Parallel I/O on Terminal Side
- Optional AIS Communication With Another TNETS3001 or TNETS3003
- Interface to Microprocessors With Hierarchical Scan and Optional Hardware Interrupt on Alarms
- SONET Alarm Processing Performance Monitoring
- Meets 1991 ANSI/Bellcore Standards:
  - T1X1.5/90-025R1
  - TA-NWT-000253

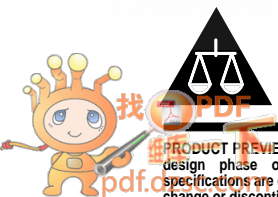
## description

The TNETS3001, synchronous optical network (SONET) overhead terminator, performs section overhead, line overhead, and path overhead signal processing at the STS-1 (51.84 Mbit/s) data rate. Repeaters, line-termination points, and path termination points are just a few applications that use the versatile TNETS3001.

The TNETS3001 contains three status registers, seven control registers, transport overhead RAM, and path overhead RAM; a line-side interface, terminal-side interface, orderwire/APS interface, datacom interface, and microprocessor interface are also integrated into a single 84-pin plastic chip carrier, which is suitable for socket or surface mounting. Status and control registers configure the device and allow for different line-side and terminal-side clock rates (receive/transmit pointer is recalculated as necessary to compensate for the clock differences); the registers also enable the overhead terminator to perform loopback and serial/parallel inputs or outputs. All transport and path overhead bytes are stored in the device RAM. Depending on the application, new overhead bytes are substituted from RAM to either terminal or line side. Besides software and hardware interrupts, alarm detection and alarm-indication signal (AIS) generation are provided. The device is controlled via a 9-bit address bus and an 8-bit interleaved data bus.

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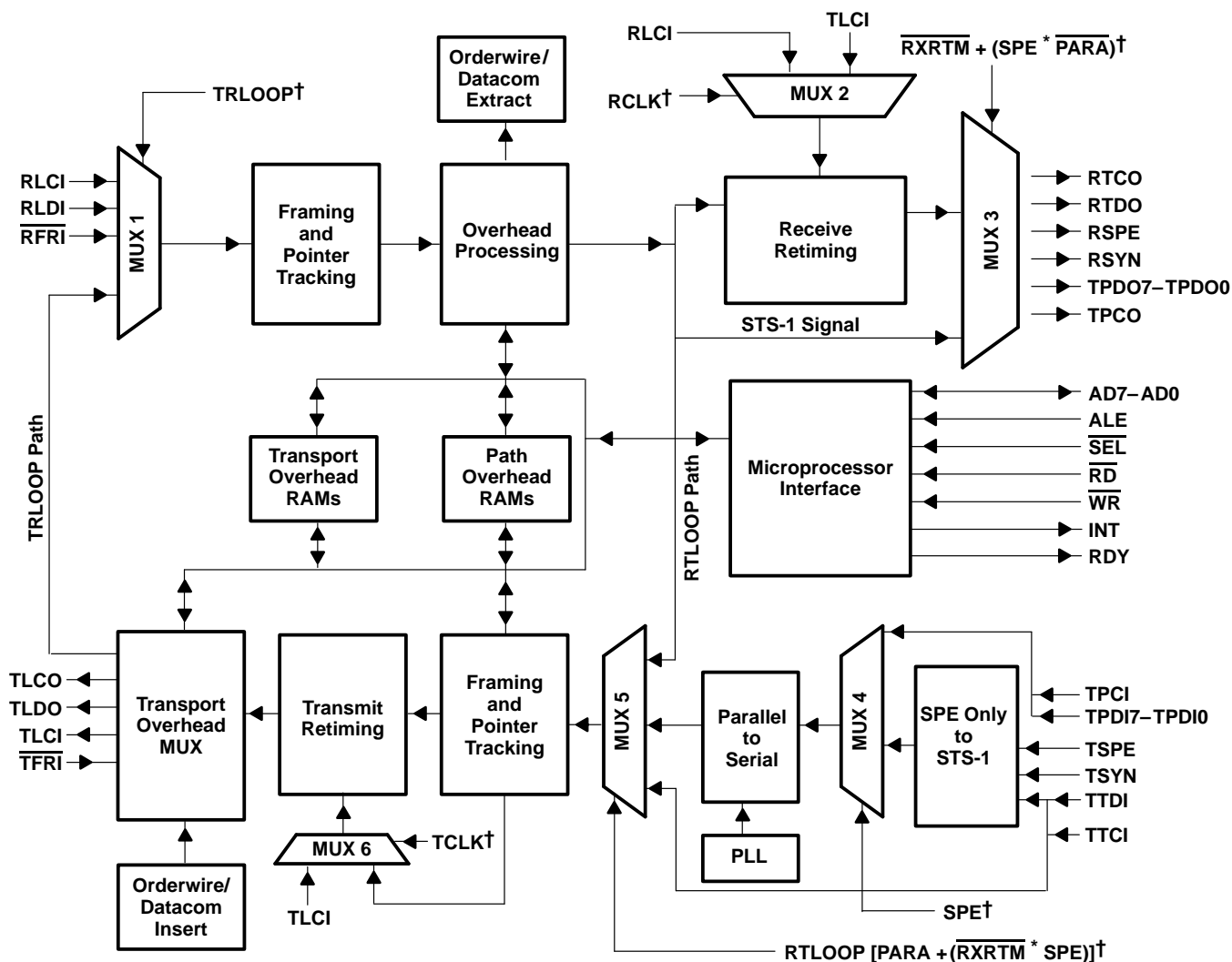


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[illegible]

### functional block diagram



† The following internal control bits are identified as shown:

RCLK – See control register 5, bit 6

TCLK – See control register 5, bit 5

**RXRTM** – See control register 9, bit 1

SPE – See control register 5, bit 7

PARA – See control register 2, bit 6

TRLOOP – See control register 0, bit 0

RTLOOP – See control register 3, bit 0

RTCCCR: RTC control register 0, bit 0

### **detailed description**

The input multiplexer MUX 1 shown in the functional block diagram selects either the line-side input or the loopback signal from the transmit-line output as the input to the framing and pointer-tracking function. The framing and pointer-tracking function performs frame synchronization to the incoming STS-1 signal, serial-to-parallel conversion, and pointer tracking; incoming STS-1 alarms are also detected. The overhead-processing function stores the line, section, and path-overhead bytes into RAM locations for access by the microprocessor. It then optionally multiplexes the line, section, and path-overhead bytes from the RAM locations written by the microprocessor. Incoming SONET performance-monitoring functions and debouncing of selected overhead bytes are also performed by the overhead-processing function. The orderwire/datacom extract function extracts and routes the section and line data-communication bytes to the two datacom interfaces and the APS and the two orderwire bytes to the orderwire interface.

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### detailed description (continued)

The receive-retiming function retimes the line input to the reference frequency, performs pointer recalculation, and SPE-only extraction. All transport-overhead bytes are demultiplexed and the payload is retimed. The reference clock used for retiming is selected by MUX 2 as either the line clock (RLCI) or the reference clock TLCI. The terminal-side output multiplexer MUX 3 allows selection of either the output of the overhead-processing function or the output of the receive-retiming function.

In the transmit direction, the SPE-only signal to STS-1 function receives serial SPE-only signals from the terminal and introduces framing and pointer bytes to produce a parallel STS-1 signal. The parallel-to-serial function uses the phase-lock loop (PLL) to serialize either the data from the SPE-only function or parallel input from the terminal. The MUX 5 multiplexer selects the input to the transmit-framing and the pointer-tracking function from either loopback data from the output of the receive-side overhead-processing function or the output of the parallel-to-serial converter or serial STS-1 input from the terminal.

The framing and pointer-tracking function performs frame synchronization to the serial STS-1 signal, serial-to-parallel conversion, and pointer tracking. Incoming STS-1 alarms are also detected. The section, line, and path-overhead bytes are stored into RAM locations for access by the microprocessor. The path-overhead bytes are then optionally multiplexed from the RAM locations written by the microprocessor.

The transmit-retiming function performs retiming to the reference frequency and pointer recalculation. The transport-overhead multiplexer optionally multiplexes the section and line overhead bytes from the RAM written by the microprocessor. The orderwire/datacom insert optionally multiplexes the orderwire, datacom and APS bytes from the two datacom interfaces and the orderwire interface into the transmit outgoing transport-overhead RAM locations.

The transport-overhead RAMs consist of locations for storing received incoming transport-overhead bytes, received outgoing transport-overhead bytes (written by the microprocessor), transmitted incoming transport-overhead bytes, and transmitted outgoing transport-overhead bytes. It also stores B1 and B2 performance monitors and pointer-justification counters. The RAM also acts as a temporary storage for datacom and orderwire bytes received from the respective interfaces.

The path-overhead RAMs consist of locations for storing received incoming path-overhead bytes, received outgoing path-overhead bytes (written by the microprocessor), transmitted incoming path-overhead bytes, and transmitted outgoing path-overhead bytes. It also stores B3 and FEBE performance monitors.

The microprocessor interface provides access to the control registers that select various modes of operation and status registers that report various alarm conditions. It also provides access to the transport- and path-overhead RAMs and provides both software and hardware interrupt capability based on the status of the device.

When in the serial mode (PABA = 0) with SPE = 1, the terminal output of the TNETS3001 contains payload bits but no transport-overhead (TOH) bits (see the TNETS3001 memory map section of this data sheet). The RSPE output provides a gapping signal for the SPE-only mode of operation. Nominally, there are 24 bits ( $8 \times 3$ ) of TOH and 696 bits ( $8 \times 87$ ) of payload. For this circumstance, the RSPE provides 24 equally spaced gaps in the output data ( $720/24 = 30$ , every 30th bit is gapped). When there is an increment in the pointer, there must be 32 equally spaced gaps and when there is a decrement, there are 16 equally spaced gaps for the row containing the pointer bytes.

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## Terminal Functions

### power supply

| TERMINAL |                       | I/O | DESCRIPTION                          |
|----------|-----------------------|-----|--------------------------------------|
| NAME     | NO.                   |     |                                      |
| AGND     | 56                    | O   | Analog ground                        |
| AVCC     | 58                    | I   | Analog supply voltage, 5 V $\pm$ 5 % |
| GND      | 5, 14, 24, 62, 68, 78 | O   | Digital ground                       |
| VCC      | 1, 17, 28, 47, 69     | I   | Supply voltage, 5 V $\pm$ 5 %        |

### microprocessor interface

| TERMINAL                      |                         | I/O        | DESCRIPTION   |
|-------------------------------|-------------------------|------------|---|
| NAME                          | NO.                     |            |   |
| A8                            | 22                      | I<br>TTL   | Address bus. This is bit 8 of the address bus.  |
| AD7–AD4<br>AD3–AD2<br>AD1–AD0 | 21–18<br>16–15<br>13–12 | I/O<br>TTL | Address/data bus. These signals provide the time-multiplexed address and data interface between the microprocessor and internal RAM.  |
| ALE                           | 32                      | I<br>TTL   | Address latch enable. ALE is an active-high signal provided by the microprocessor that latches the address into a TNETS3001 address latch for a bus cycle.  |
| INT                           | 33                      | O<br>TTL   | Interrupt. INT is an active-high signal that confirms an interrupt request to the microprocessor. The hardware interrupt request is enabled by HINT = 1 (bit 5, address 0FA).   |
| $\overline{\text{RD}}$        | 25                      | I<br>TTL   | Read. $\overline{\text{RD}}$ is an active-low input generated by the microprocessor for reading the TNETS3001.  |
| RDY                           | 31                      | O          | Ready. RDY is an active-high acknowledgment from the TNETS3001 that indicates a transfer can be completed. RDY goes low when the address being read or written to corresponds to a RAM location. When status or control registers are accessed, RDY remains high. RDY is an open-drain output capable of sinking a maximum of 16 mA. The value of the pullup resistor depends on the number of devices that use the RDY signal in the system. |
| RST                           | 63                      | I<br>TTL   | Reset. RST resets all internal counters and sets all alarms. RST is a positive pulse with a minimum width of 300 ns. RST must be used after power is applied, registers are initialized, and the clocks are stable.   |
| $\overline{\text{SEL}}$       | 34                      | I<br>TTL   | Select. $\overline{\text{SEL}}$ is an active-low signal that enables data transfers between the microprocessor and TNETS3001 RAM during a read/write bus cycle.   |
| $\overline{\text{WR}}$        | 23                      | I<br>TTL   | Write. $\overline{\text{WR}}$ is an active-low signal generated by the microprocessor for writing to the TNETS3001.   |

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## Terminal Functions (Continued)

### receive line-side interface

| TERMINAL<br>NAME          | NO. | I/O       | DESCRIPTION   |
|---------------------------|-----|-----------|---|
| $\overline{\text{RFRI}}$  | 6   | I<br>CMOS | Receive-line frame in. $\overline{\text{RFRI}}$ is an optional active-low frame pulse that occurs during the C1 byte, bit 7 time. When used, $\overline{\text{RFRI}}$ reduces the OOF exit time from two frames to one frame.   |
| RLCI                      | 8   | I<br>CMOS | Receive-line clock in. RLCI is a 51.84-MHz clock that clocks in the serial data and the optional framing pulse. RLCI is used as the time base for framing, pointer tracking, demultiplexing the transport-overhead bytes, and for RAM access in the receive side.                                 |
| RLDI                      | 7   | I<br>CMOS | Receive-line data in. RLDI is the incoming serial STS-1/STS-N data that is clocked into the TNETS3001 on the rising edge of RLCI.   |
| $\overline{\text{RXLOS}}$ | 9   | I<br>TTL  | Receive loss of signal. $\overline{\text{RXLOS}}$ is an active-low external loss-of-signal indicator from a higher multiplexer such as an SM3. TNETS3001 combines $\overline{\text{RXLOS}}$ with the internal loss of signal and reports the result to the microprocessor as the RLOS status bit. |

### transmit line-side interface

| TERMINAL<br>NAME         | NO. | I/O       | DESCRIPTION  |
|--------------------------|-----|-----------|--|
| $\overline{\text{TFRI}}$ | 30  | I<br>CMOS | Transmit-frame reference in. $\overline{\text{TFRI}}$ is an optional active-low frame pulse, synchronous with TLCI, that determines outgoing A1A2 epoch. $\overline{\text{TFRI}}$ can be used only if $\text{TCLK} = 1$ (bit 6 address 1FA). |
| TLCI                     | 29  | I<br>CMOS | Transmit line-side clock in. TLCI is the 51.84-MHz reference-clock input.  |
| TLCO                     | 27  | O<br>CMOS | Transmit line-side clock out. TLCO is an outgoing serial STS-1/STS-N clock. Depending on the operating mode, TLCO is derived from TLCI, TTCI, or TPCI.   |
| TLDO                     | 26  | O<br>CMOS | Transmit line-side data out. TLDO is outgoing serial STS-1/STS-N data that is clocked out of the TNETS3001 on the falling edge of TLCO.  |

### orderwire/APS interface

| TERMINAL<br>NAME        | NO. | I/O      | DESCRIPTION  |
|-------------------------|-----|----------|--|
| LRFR                    | 65  | O<br>TTL | Receive-line orderwire-framing pulse. LRFR is an active-low signal that occurs one clock cycle after the LSB of the K2 byte in the serial-bit stream (OTDO).                       |
| LTFR                    | 39  | O<br>TTL | Transmit-line orderwire-framing pulse. LTFR is the transmit-frame pulse for line-orderwire codec/filter.   |
| ORCO                    | 70  | O<br>TTL | Receive orderwire and APS clock. ORCO is a 576-kHz clock, derived from RLCI, used for clocking the orderwire and APS bytes from the TNETS3001.                                     |
| ORDO                    | 67  | O<br>TTL | Receive-orderwire byte and APS-byte output. The two orderwire bytes and APS bytes are clocked out of the TNETS3001 on positive transitions of ORCO.                                |
| OTCO                    | 42  | O<br>TTL | Transmit orderwire and APS clock. OTCO is a 576-kHz clock, synchronous to TLCO, used for sourcing the orderwire and APS bytes into the TNETS3001.                                  |
| OTDI                    | 41  | I<br>TTL | Transmit-orderwire byte and APS-byte input. The two orderwire bytes and APS bytes are clocked into the TNETS3001 on negative transitions of OTCO.                                  |
| $\overline{\text{RAP}}$ | 66  | O<br>TTL | Receive APS framing pulse. $\overline{\text{RAP}}$ is an active-low signal that occurs one clock cycle after the LSB of the K2 byte in the serial-bit stream (OTDO).               |
| SRFR                    | 64  | O<br>TTL | Receive-section orderwire-framing pulse. SRFR is the receive-frame pulse for section-orderwire codec/filter.   |
| STFR                    | 38  | O<br>TTL | Transmit-section orderwire-framing pulse. STFR is the transmit-frame pulse for section-orderwire codec/filter.   |
| $\overline{\text{TAP}}$ | 40  | O<br>TTL | Transmit APS-framing pulse. $\overline{\text{TAP}}$ is an active-low signal that occurs one clock cycle before the MSB of the K1 byte is expected in the serial-bit stream (OTDI). |

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## Terminal Functions (Continued)

### section and line data-communication interface

| TERMINAL<br>NAME | NO. | I/O      | DESCRIPTION   |
|------------------|-----|----------|---|
| STDI             | 43  | I<br>TTL | Transmit section data-communication data input. STDI is serial 192-kbit/s data (D1 – D3 bytes) clocked into the TNETS3001 on positive transitions of STCO.              |
| STCO             | 44  | O<br>TTL | Transmit section data-communication clock output. STCO is a 192-kHz clock, derived from TLCO, used for sourcing the section data-communication data into the TNETS3001. |
| LTDI             | 45  | I<br>TTL | Transmit line data-communication data input. LTDI is serial 576-kbit/s data (D4 – D12 bytes) clocked into the TNETS3001 on positive transitions of LTCO.                |
| LTCO             | 46  | O<br>TTL | Transmit line data-communication clock output. LTTCO is a 576-kHz clock, derived from TLCO, used for sourcing the line data-communication data into the TNETS3001.      |
| SRDO             | 71  | O<br>TTL | Receive section data-communication data output. SRDO is serial 192-kbit/s data (D1 – D3 bytes) clocked out of the TNETS3001 on positive transitions of SRCO.            |
| LRCO             | 72  | O<br>TTL | Receive line data-communication clock output. LRDO is a 576-kHz clock, derived from RLCI, used for clocking out the line data-communication serial data.                |
| LRDO             | 73  | O<br>TTL | Receive line data-communication data output. LRDO is serial 576-kbit/s data (D4 – D12 bytes) clocked out of the TNETS3001 on negative transitions of LRDO.              |
| SRCO             | 74  | O<br>TTL | Receive section data-communication clock output. SRDO is a 192-kHz clock, derived from RLCI, used for clocking out the section data-communication data.                 |

### terminal-side interface

| TERMINAL<br>NAME           | NO.            | I/O         | DESCRIPTION  |
|----------------------------|----------------|-------------|--|
| RTCO                       | 3              | I/O<br>CMOS | Receive terminal-side clock output. RTCO is a 51.84-MHz terminal clock used for clocking out RTDO. Depending on operating mode, RTCO is derived either from RLCI or TLCI.  |
| RTDO                       | 4              | O<br>CMOS   | Receive terminal-side data output. RTDO is serial 51.84-Mbit/s STS-1 receive data clocked out of the TNETS3001 on negative transitions of RTCO.  |
| RSPE                       | 10             | O<br>CMOS   | Receive terminal-side SPE indication. RSPE is an active-high signal that indicates the synchronous payload envelope in the terminal data output (RTDO or TPDO). For SPE-only mode, RSPE is a gapping signal.                         |
| RSYN                       | 75             | O<br>CMOS   | Receive terminal-side synchronization pulse. RSYN is high during the C1 byte and J1 byte of RTDO or TPDO. In serial SPE-only mode, RSYN is high only during the J1 byte of RTDO.   |
| TPCO                       | 2              | O<br>TTL    | Terminal-side parallel-clock output. TPCO is a 6.48-MHz clock, derived from RTCO, that clocks out received terminal byte data (TPDO).  |
| TPDO7–TPDO2<br>TPDO1–TPDO0 | 84–79<br>77–76 | O<br>TTL    | Terminal-side parallel-data output. Byte-wide 6.48-Mbyte/s receive terminal data is clocked out of the TNETS3001 on positive transitions of TPCO.  |
| TTCI                       | 60             | I<br>CMOS   | Transmit terminal-side serial-clock input. TTCI is a 51.84-MHz terminal clock used for clocking in TTDI.   |
| TTDI                       | 61             | I<br>CMOS   | Transmit terminal-side data input. TTDI is serial 51.84-Mbit/s transmit terminal data clocked into the TNETS3001 on positive transitions of TTCI.  |
| TSPE                       | 36             | I<br>CMOS   | Transmit terminal-side SPE indication. TSPE is required input for the SPE-only mode. A high value indicates the location of the SPE bits in TTDI. A low value identifies the location of a gap in the input data.                    |
| TSYN                       | 37             | I<br>CMOS   | Transmit terminal-side synchronization pulse. TSYN is required input for the SPE-only mode. TSYN must be high during incoming J1 byte of TTDI or TPDI in the SPE-only mode. A high value during the C1 byte of the data is optional. |
| TPCI                       | 59             | I<br>CMOS   | Terminal-side parallel-clock input. TPCI is a 6.48-MHz clock used for clocking TPDI, TSPE, and TSYN.   |
| TPDI7–TPDI0                | 48–55          | I<br>TTL    | Terminal-side parallel-data input. TPDI7–TPDI0 is byte-wide 6.48-Mbyte/s transmit terminal data clocked into the TNETS3001 on positive transitions of TPCI.  |

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### Terminal Functions (Continued)

#### alarm-indication ports

| TERMINAL<br>NAME         | NO. | I/O      | DESCRIPTION   |
|--------------------------|-----|----------|---|
| $\overline{\text{RAIS}}$ | 11  | O<br>TTL | Receive alarm-indication signal. $\overline{\text{RAIS}}$ is an active-low signal indicating that a downstream AIS must be generated. RAIS is activated when PTE =1 or LTE =1 and any of the following conditions are active: RLOC, RLOS, RLOF, RLAIS, RLOP, RPAIS. |
| $\overline{\text{TAIS}}$ | 35  | I<br>TTL | Transmit alarm-indication signal. $\overline{\text{TAIS}}$ is an active-low input that causes AIS to be introduced into the transmit line.  |

#### phase-lock loop

| TERMINAL<br>NAME | NO. | I/O | DESCRIPTION  |
|------------------|-----|-----|--|
| TCAP             | 57  | I/O | External resistor capacitor. TCAP is a 1.2-k $\Omega$ , 1/4 W, 5% carbon composition resistor in series with a 1000-pF capacitor connected to analog ground. The RC network is required when the terminal interface is used in the following modes: parallel and SPE only. |

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|   |                            |
|---|----------------------------|
| Supply voltage range, $V_{CC}$ (see Note 1) | –0.3 V to 7 V              |
| Input voltage range, $V_I$                  | –0.5 V to $V_{CC} + 0.5$ V |
| Operating free-air temperature range, $T_A$ | –40°C to 85°C              |
| Operating junction temperature              | 150°C                      |
| Storage temperature range, $T_{stg}$        | –55°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

#### recommended operating conditions

|           |                          | MIN               | NOM  | MAX  | UNIT |
|-----------|--------------------------|-------------------|------|------|------|
| $V_{CC}$  | Supply voltage           | 4.75              | 5    | 5.25 | V    |
| $AV_{CC}$ | Supply voltage, analog   | 4.75              | 5    | 5.25 | V    |
| $V_{IH}$  | High-level input voltage | CMOS              | 3.15 |      | V    |
|           |                          | CMOS (see Note 2) | 2    |      |      |
|           |                          | TTL               | 2    |      |      |
|           |                          | TTL (see Note 3)  | 2    |      |      |
| $V_{IL}$  | Low-level input voltage  | CMOS              |      | 1.65 | V    |
|           |                          | CMOS (see Note 2) |      | 0.8  |      |
|           |                          | TTL               |      | 0.8  |      |
|           |                          | TTL (see Note 3)  |      | 0.8  |      |

NOTES: 2. Input has a 100-k $\Omega$  internal pullup resistor.

3. Input has a 9-k $\Omega$  internal pullup resistor.

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**electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)**

| PARAMETER         |   | TEST CONDITIONS   |  | MIN                     | TYP                   | MAX | UNIT |
|-------------------|---|-------------------|--|-------------------------|-----------------------|-----|------|
| V <sub>OH</sub>   | High-level output voltage                 | 4-mA TTL          | V <sub>CC</sub> = 4.75 V                     | I <sub>OH</sub> = -2 mA | V <sub>CC</sub> - 0.5 |     | V    |
|                   |   | 8-mA TTL          |  | I <sub>OH</sub> = -4 mA | V <sub>CC</sub> - 0.5 |     | V    |
|                   |   | 4-mA CMOS         |  |                         | V <sub>CC</sub> - 0.5 |     | V    |
| V <sub>OL</sub>   | Low-level output voltage                  | 4-mA TTL          | V <sub>CC</sub> = 4.75 V                     | I <sub>OL</sub> = 4 mA  |                       | 0.4 | V    |
|                   |   | 4-mA CMOS         |  | I <sub>OL</sub> = 4 μA  |                       | 0.4 | V    |
|                   |   | 8-mA TTL          |  | I <sub>OL</sub> = 8 mA  |                       | 0.4 | V    |
|                   |   | 16-mA open drain  |  | I <sub>OL</sub> = 16 mA |                       | 0.4 | V    |
| I <sub>I</sub>    | Input current                             | TTL               | V <sub>CC</sub> = 5.25 V                     |                         |                       | 10  | μA   |
|                   |   | CMOS              |  |                         |                       | 10  | μA   |
|                   |   | CMOS (see Note 2) |  |                         | 50                    | 120 | μA   |
| I <sub>IL</sub>   | Low-level input current, TTL (see Note 3) |                   | V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0 |                         | 0.5                   | 1.4 | mA   |
| I <sub>CC</sub>   | Supply current                            |                   |  |                         |                       |     | mA   |
| A <sub>I</sub> CC | Supply current, analog                    |                   |  |                         |                       |     | mA   |
| C <sub>i</sub>    | Input capacitance                         |                   |  |                         |                       | 5.5 | pF   |

NOTES: 2. Input has a 100-kΩ internal pullup resistor.  
3. Input has a 9-kΩ internal pullup resistor.

**operating characteristics over recommended ranges of operating free-air temperature and supply voltage**

| PARAMETER      |                       | TEST CONDITIONS   |  |  | MIN | MAX | UNIT |
|----------------|-----------------------|---|--|--|-----|-----|------|
| t <sub>r</sub> | Rise time, TTL        | C <sub>L</sub> = 15 pF, I <sub>OL</sub> = 4 mA, I <sub>OH</sub> = -2 mA |  |  |     |     | ns   |
| t <sub>f</sub> | Fall time, TTL        |   |  |  |     |     |      |
| t <sub>r</sub> | Rise time, TTL        | C <sub>L</sub> = 25 pF, I <sub>OL</sub> = 8 mA, I <sub>OH</sub> = -4 mA |  |  |     |     | ns   |
| t <sub>f</sub> | Fall time, TTL        |   |  |  |     |     |      |
| t <sub>r</sub> | Rise time, CMOS       | C <sub>L</sub> = 15 pF, I <sub>OL</sub> = 4 mA, I <sub>OH</sub> = -4 mA |  |  |     |     | μs   |
| t <sub>f</sub> | Fall time, CMOS       |   |  |  |     |     |      |
| t <sub>f</sub> | Fall time, open drain | C <sub>L</sub> = 15 pF, I <sub>OL</sub> = 6 mA                          |  |  |     |     | ns   |

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timing requirements,  $C_L = 15\text{ pF}$  (see Note 4 and Figure 1)

| NO. |   | MIN | NOM   | MAX | UNIT |
|-----|---|-----|-------|-----|------|
| 1   | $t_{c(RLCI)}$ Clock cycle time, RLCI                        |     | 19.29 |     | ns   |
| 2   | $t_{w(RLCIH)}$ Pulse duration, RLCI high                    |     | 9.65  |     | ns   |
| 3   | $t_{w(RLCIL)}$ Pulse duration, RLCI low                     |     | 9.65  |     | ns   |
| 4   | $t_{su(RLDI)}$ Setup time, RLDI valid before RLCI↑          |     |       |     | ns   |
| 4   | $t_{su(RFRI)}$ Setup time, $\overline{RFRI}$ ↓ before RLCI↑ |     |       |     | ns   |
| 5   | $t_{h(RLDI)}$ Hold time, RLDI valid after RLCI↑             |     |       |     | ns   |
| 5   | $t_{h(RFRI)}$ Hold time, $\overline{RFRI}$ ↑ after RLCI↑    |     |       |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

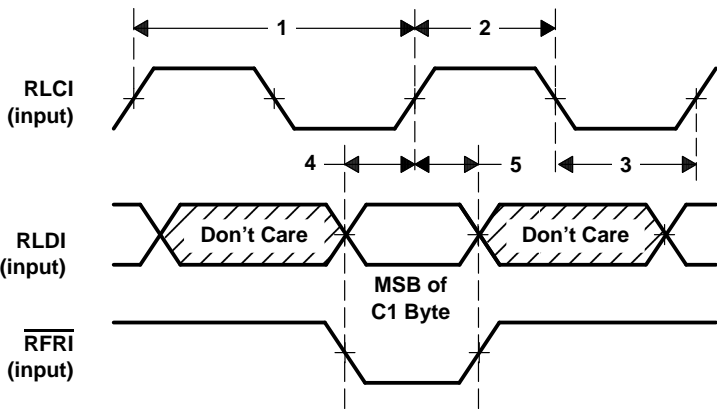


Figure 1. Line-Side Input Timing

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timing requirements,  $C_L = 15 \text{ pF}$  (see Notes 4 and 5, and Figure 2)

| NO. |   | MIN | NOM   | MAX | UNIT |
|-----|---|-----|-------|-----|------|
| 1   | $t_c(\text{TLCI})$ Clock cycle time, TLCI   |     | 19.29 |     | ns   |
| 2   | $t_w(\text{TLCI-H})$ Pulse duration, TLCI high  |     | 9.65  |     | ns   |
| 3   | $t_w(\text{TLCI-L})$ Pulse duration, TLCI low   |     | 9.65  |     | ns   |
| 4   | $t_{su}(\text{TFRI})$ Setup time, $\overline{\text{TFRI}}$ low before $\text{TLCI}\uparrow$ |     |       |     | ns   |
| 5   | $t_h(\text{TFRI})$ Hold time, $\overline{\text{TFRI}}$ high after $\text{TLCI}\uparrow$     |     |       |     | ns   |

NOTES: 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

5:  $\overline{\text{TFRI}}$  can be used only if the control bit  $\text{TCLK} = 1$ .

operating characteristics,  $C_L = 15 \text{ pF}$  (see Notes 4 and 5, and Figure 2)

| NO. |   | MIN | NOM | MAX | UNIT |
|-----|---|-----|-----|-----|------|
| 6   | $t_d(\text{TLCO})$ Delay time, $\text{TLCI}\uparrow$ to $\text{TLCO}\uparrow$ |     |     |     | ns   |
| 7   | $t_d(\text{TLDO})$ Delay time, $\text{TLCO}\downarrow$ to $\text{TLDO}$ valid |     |     |     | ns   |

NOTES: 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

5:  $\overline{\text{TFRI}}$  can be used only if the control bit  $\text{TCLK} = 1$ .

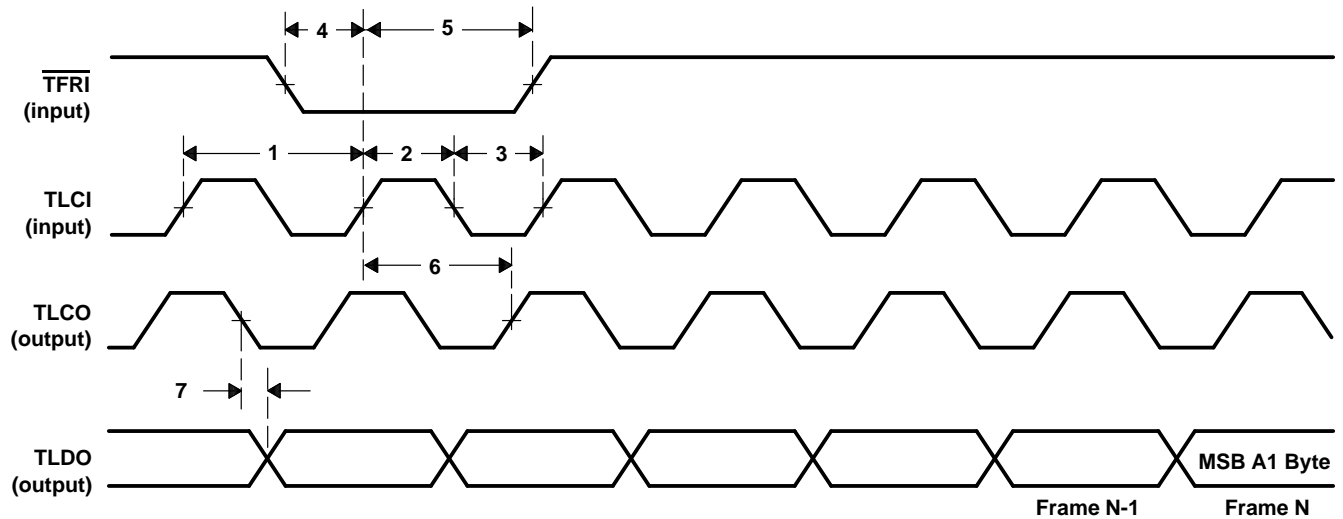


Figure 2. Line-Side Output Timing

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operating characteristics,  $C_L = 15\text{ pF}$  (see Note 4 and Figure 3)

| NO. |   | MIN | TYP  | MAX | UNIT |
|-----|---|-----|------|-----|------|
| 1   | $t_{c(ORCO)}$ Clock cycle time, ORCO                                  |     | 1736 |     | ns   |
| 2   | $t_{w(ORCO-H)}$ Pulse duration, ORCO high                             |     | 868  |     | ns   |
| 3   | $t_{w(ORCO-L)}$ Pulse duration, ORCO low                              |     | 868  |     | ns   |
| 4   | $t_{d(SRFR)}$ Delay time, $ORCO\uparrow$ to $SRFR\uparrow$            |     |      |     | ns   |
| 4   | $t_{d(LRFR)}$ Delay time, $ORCO\uparrow$ to $LRFR\uparrow$            |     |      |     | ns   |
| 5   | $t_{d(RAP)}$ Delay time, $ORCO\uparrow$ to $\overline{RAP}\downarrow$ |     |      |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

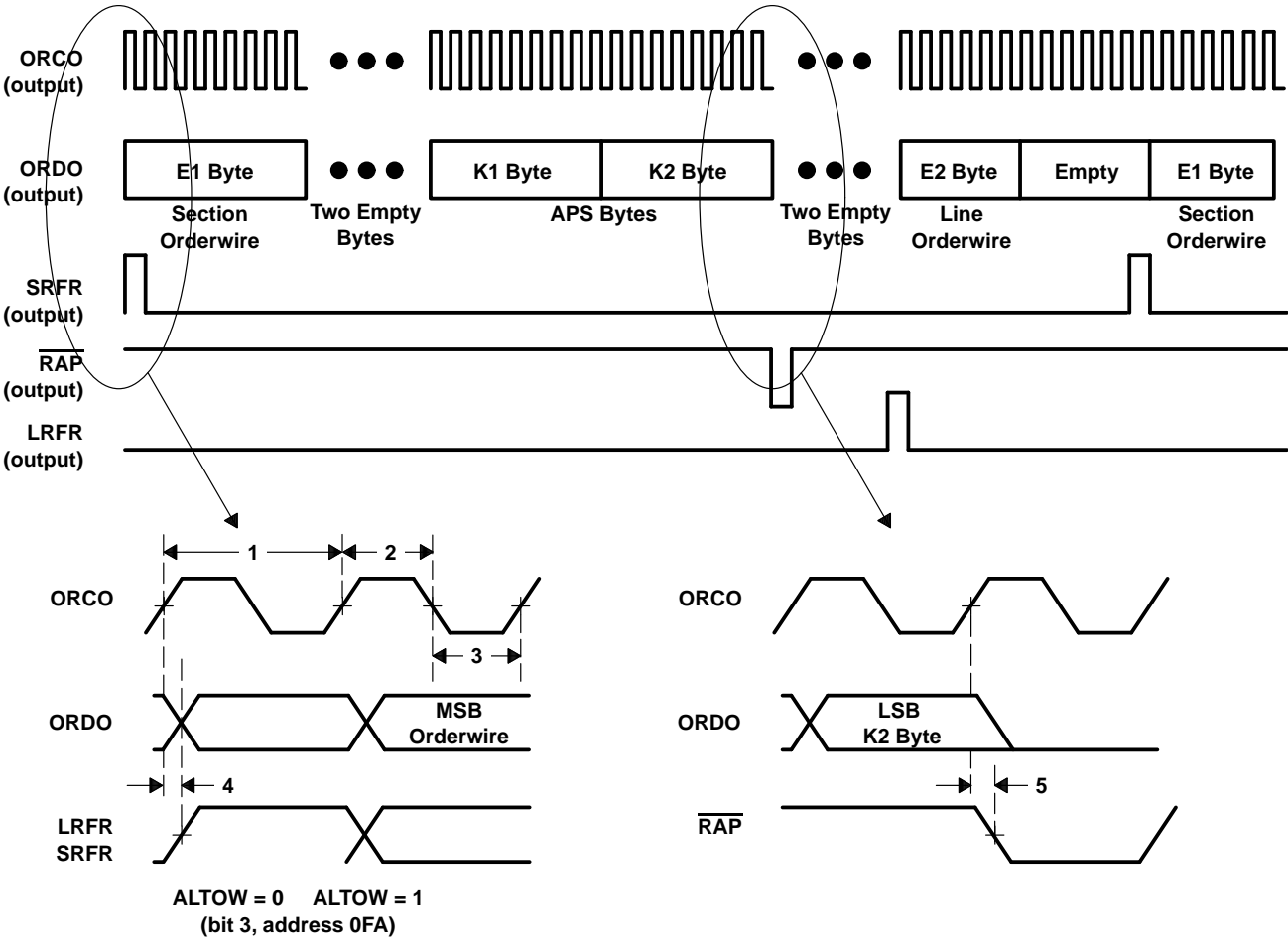


Figure 3. APS and Orderwire Output Timing

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timing requirements,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 4)

| NO. |   | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1   | $t_{su}(\text{OTDI})$ Setup time, OTDI valid before $\text{OTCO}\downarrow$ |     |     | ns   |
| 2   | $t_h(\text{OTDI})$ Hold time, OTDI valid after $\text{OTCO}\downarrow$      |     |     | ns   |

operating characteristics,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 4)

| NO. |   | MIN | TYP  | MAX | UNIT |
|-----|---|-----|------|-----|------|
| 3   | $t_c(\text{OTCO})$ Clock cycle time, OTCO                                       |     | 1736 |     | ns   |
| 4   | $t_w(\text{ORCOH})$ Pulse duration, ORCO high                                   |     | 868  |     | ns   |
| 5   | $t_w(\text{OTCOL})$ Pulse duration, ORCO low                                    |     | 868  |     | ns   |
| 6   | $t_d(\text{LTFR})$ Delay time, $\text{OTCO}\uparrow$ to $\text{LTFR}\uparrow$   |     |      |     | ns   |
| 6   | $t_d(\text{STFR})$ Delay time, $\text{OTCO}\uparrow$ to $\text{STFR}\uparrow$   |     |      |     | ns   |
| 7   | $t_d(\text{TAP})$ Delay time, $\text{OTCO}\downarrow$ to $\text{TAP}\downarrow$ |     |      |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

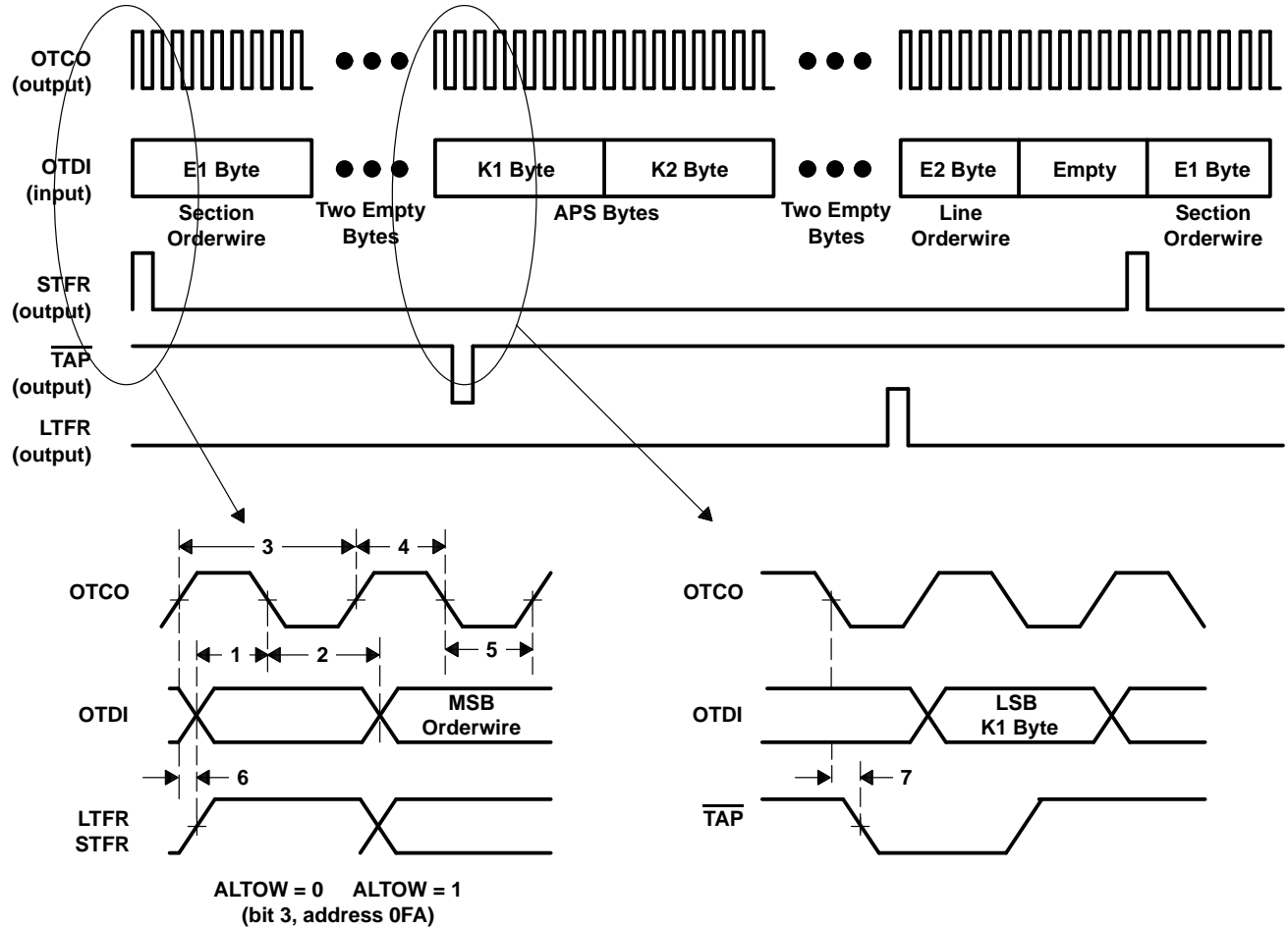


Figure 4. APS and Orderwire Input Timing

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operating characteristics,  $C_L = 15\text{ pF}$  (see Note 4 and Figure 5)

| NO. |  | MIN | TYP  | MAX | UNIT          |
|-----|--|-----|------|-----|---------------|
| 1   | $t_c(\text{SRCO})$ Clock cycle time, SRCO                            |     | 5.21 |     | $\mu\text{s}$ |
| 2   | $t_w(\text{SRCOH})$ Pulse duration, SRCO high                        |     | 2.6  |     | $\mu\text{s}$ |
| 3   | $t_w(\text{SRCOL})$ Pulse duration, SRCO low                         |     | 2.6  |     | $\mu\text{s}$ |
| 4   | $t_d(\text{SRDO})$ Delay time, $\text{SRCO}\downarrow$ to SRDO valid |     |      |     |               |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

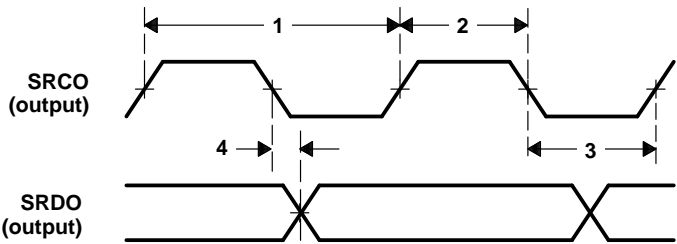


Figure 5. Section-Datcom-Channel Output Timing

operating characteristics,  $C_L = 15\text{ pF}$  (see Note 4 and Figure 6)

| NO. |  | MIN | TYP  | MAX | UNIT |
|-----|--|-----|------|-----|------|
| 1   | $t_c(\text{LRCO})$ Clock cycle time, LRCO                            |     | 1736 |     | ns   |
| 2   | $t_w(\text{LRCOH})$ Pulse duration, LRCO high                        |     | 868  |     | ns   |
| 3   | $t_w(\text{LRCOL})$ Pulse duration, LRCO low                         |     | 868  |     | ns   |
| 4   | $t_d(\text{LRDO})$ Delay time, $\text{LRCO}\downarrow$ to LRDO valid |     |      |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

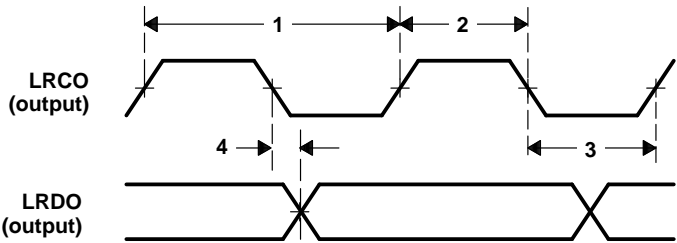


Figure 6. Line-Datcom-Channel Output Timing

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timing requirements,  $C_L = 15$  pF (see Note 4 and Figure 7)

| NO. |  | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 1   | $t_{su}(STDI)$ Setup time, STDI valid before STCO↓ |     |     | ns   |
| 2   | $t_h(STDI)$ Hold time, STDI valid after STCO↓      |     |     | ns   |

operating characteristics,  $C_L = 15$  pF (see Note 4 and Figure 7)

| NO. |  | MIN | TYP  | MAX | UNIT |
|-----|--|-----|------|-----|------|
| 3   | $t_c(STCO)$ Clock cycle time, STCO     |     | 5.21 |     | μs   |
| 4   | $t_w(STCOH)$ Pulse duration, STCO high |     | 2.6  |     | μs   |
| 5   | $t_w(STCOL)$ Pulse duration, STCO low  |     | 2.6  |     | μs   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

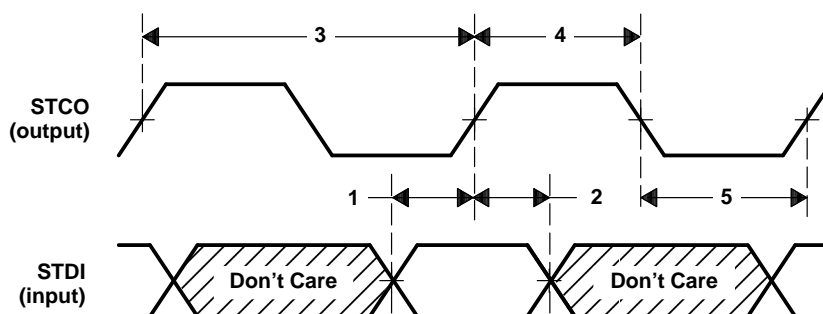


Figure 7. Section-Datcom-Channel Input Timing

timing requirements,  $C_L = 15$  pF (see Note 4 and Figure 8)

| NO. |  | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 1   | $t_{su}(LTDI)$ Setup time, LTDI valid before LTCO↑ |     |     | ns   |
| 2   | $t_h(LTDI)$ Hold time, LTDI valid after LTCO↑      |     |     | ns   |

operating characteristics,  $C_L = 15$  pF (see Note 4 and Figure 8)

| NO. |  | MIN | NOM  | MAX | UNIT |
|-----|--|-----|------|-----|------|
| 3   | $t_c(LTCO)$ Clock cycle time, LTCO     |     | 1736 |     | ns   |
| 4   | $t_w(LTCOH)$ Pulse duration, LTCO high |     | 868  |     | ns   |
| 5   | $t_w(LTCOL)$ Pulse duration, LTCO low  |     | 868  |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

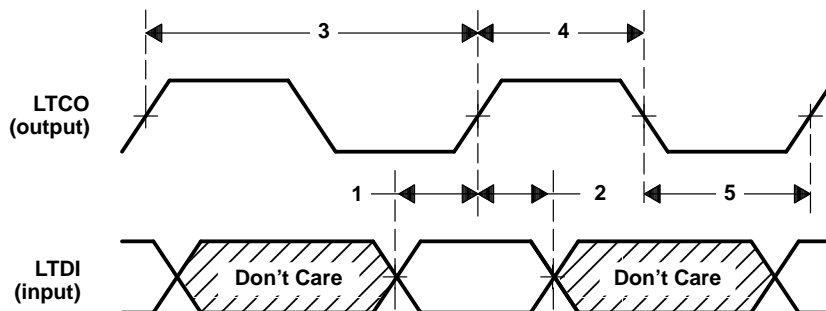


Figure 8. Line-Datcom-Channel Input Timing

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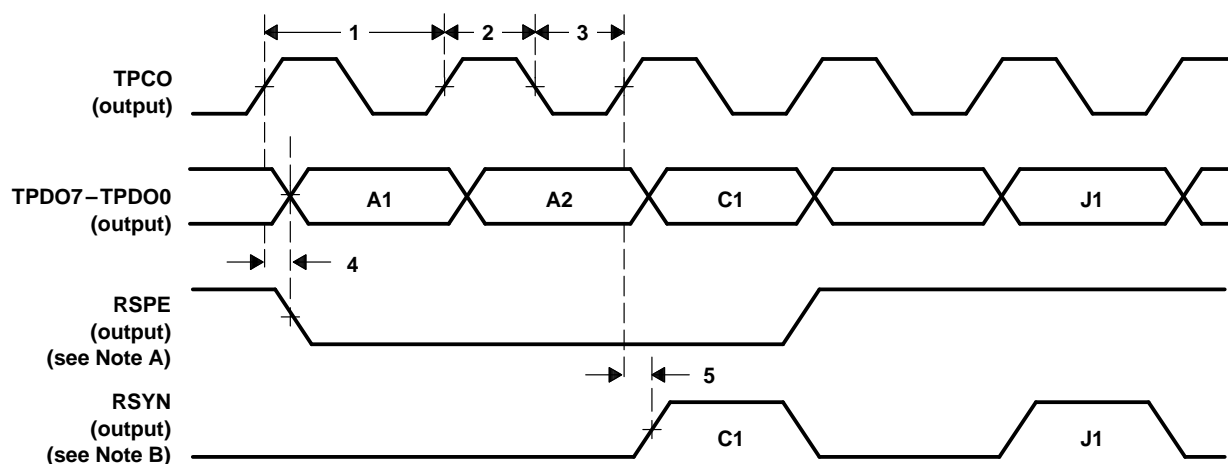
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operating characteristics,  $C_L = 15$  pF (see Note 4 and Figure 9)

| NO. |   | MIN | TYP   | MAX | UNIT |
|-----|---|-----|-------|-----|------|
| 1   | $t_c(\text{TPCO})$ Clock cycle time, TPCO                                       |     | 154.3 |     | ns   |
| 2   | $t_w(\text{TPCOH})$ Pulse duration, TPCO high                                   |     | 77.2  |     | ns   |
| 3   | $t_w(\text{TPCOL})$ Pulse duration, TPCO low                                    |     | 77.2  |     | ns   |
| 4   | $t_d(\text{TPDO})$ Delay time, $\text{TPCO}\uparrow$ to $\text{TPDO}\uparrow$   |     |       |     | ns   |
| 4   | $t_d(\text{RSPE})$ Delay time, $\text{TPCO}\uparrow$ to $\text{RSPE}\downarrow$ |     |       |     | ns   |
| 5   | $t_d(\text{RSYN})$ Delay time, $\text{TPCO}\uparrow$ to $\text{RSYN}\uparrow$   |     |       |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.



NOTES: A. Pointer movements are indicated by RSPE in subframe No. 4.  
B. J1 can be anywhere in the payload.

Figure 9. Terminal Parallel STS-1 and Parallel SPE-Only Output Timing

timing requirements,  $C_L = 15$  pF (see Note 4 and Figure 10)

| NO. |   | MIN | NOM   | MAX | UNIT |
|-----|---|-----|-------|-----|------|
| 1   | $t_c(\text{TPCI})$ Clock cycle time, TPCI                                 |     | 154.3 |     | ns   |
| 2   | $t_w(\text{TPCIH})$ Pulse duration, TPCI high                             |     | 77.2  |     | ns   |
| 3   | $t_w(\text{TPCIL})$ Pulse duration, TPCI low                              |     | 77.2  |     | ns   |
| 4   | $t_{su}(\text{TPDI})$ Setup time, TPDI valid before $\text{TPCI}\uparrow$ |     |       |     | ns   |
| 5   | $t_h(\text{TPDI})$ Hold time, TPDI valid after $\text{TPCI}\uparrow$      |     |       |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

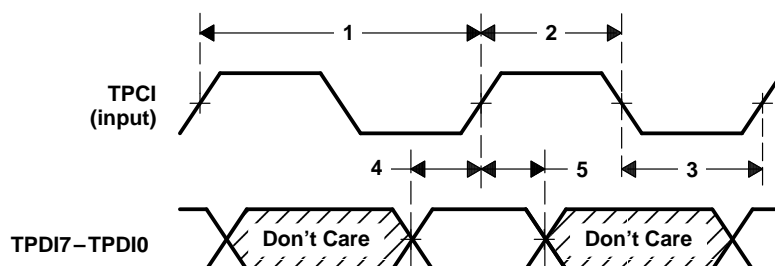


Figure 10. Terminal Parallel STS-1 Input Timing



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operating characteristics,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 11)

| NO. |   | MIN | TYP   | MAX | UNIT |
|-----|---|-----|-------|-----|------|
| 1   | $t_c(\text{RTCO})$ Clock cycle time, RTCO                             |     | 19.29 |     | ns   |
| 2   | $t_w(\text{RTCOH})$ Pulse duration, RTCO high                         |     | 9.65  |     | ns   |
| 3   | $t_w(\text{RTCOL})$ Pulse duration, RTCO low                          |     | 9.65  |     | ns   |
| 4   | $t_d(\text{RTDO})$ Delay time, $\text{RTCO} \downarrow$ to RTDO valid |     |       |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

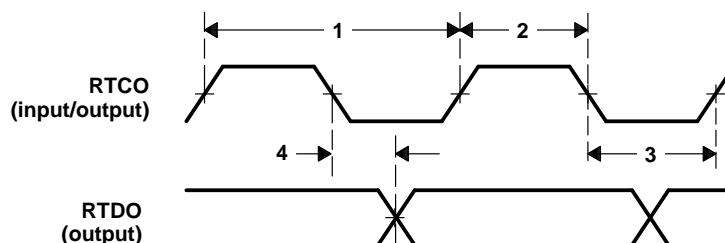


Figure 11. Terminal Serial STS-1 Output Timing

timing requirements,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 12)

| NO. |  | MIN | NOM   | MAX | UNIT |
|-----|--|-----|-------|-----|------|
| 1   | $t_c(\text{TTCI})$ Clock cycle time, TTCI                                  |     | 19.29 |     | ns   |
| 2   | $t_w(\text{TTCIH})$ Pulse duration, TTCI high                              |     | 9.65  |     | ns   |
| 3   | $t_w(\text{TTCIL})$ Pulse duration, TTCI low                               |     | 9.65  |     | ns   |
| 4   | $t_{su}(\text{TTDI})$ Setup time, TTDI valid before $\text{TTCI} \uparrow$ |     |       |     | ns   |
| 5   | $t_h(\text{TTDI})$ Hold time, TTDI valid after $\text{TTCI} \uparrow$      |     |       |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

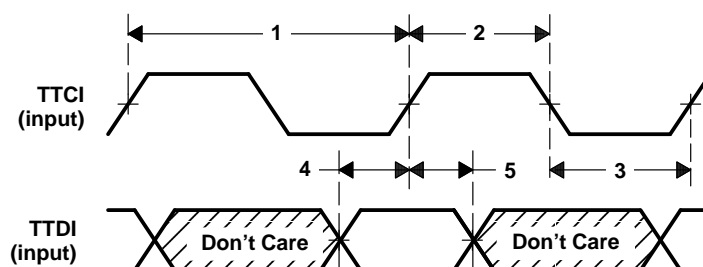


Figure 12. Terminal Serial STS-1 Input Timing

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operating characteristics,  $C_L = 15\text{ pF}$  (see Note 4 and Figure 13)

| NO. |   | MIN | TYP   | MAX | UNIT |
|-----|---|-----|-------|-----|------|
| 1   | $t_c(\text{RTCO})$ Clock cycle time, RTCO   |     | 19.29 |     | ns   |
| 2   | $t_w(\text{RTCOH})$ Pulse duration, RTCO high   |     | 9.65  |     | ns   |
| 3   | $t_w(\text{RTCOL})$ Pulse duration, RTCO low  |     | 9.65  |     | ns   |
| 4   | $t_w(\text{RSYNH})$ Pulse duration, RSYN high   |     |       |     | ns   |
| 5   | $t_d(\text{RTDO})$ Delay time, $\text{RTCO}\downarrow$ to RTDO valid                                    |     |       |     | ns   |
| 5   | $t_d(\text{RSPE})$ Delay time, $\text{RTCO}\downarrow$ to RSPE valid                                    |     |       |     | ns   |
| 5   | $t_d(\text{RSYN})$ Delay time, $\text{RTCO}\downarrow$ to RSYN valid                                    |     |       |     | ns   |
| 6   | $t_d(\text{RSPE})_{\text{GAP}}$ Delay time, gap from $\text{RSPE}\downarrow$ to $\text{RSPE}\downarrow$ |     |       |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

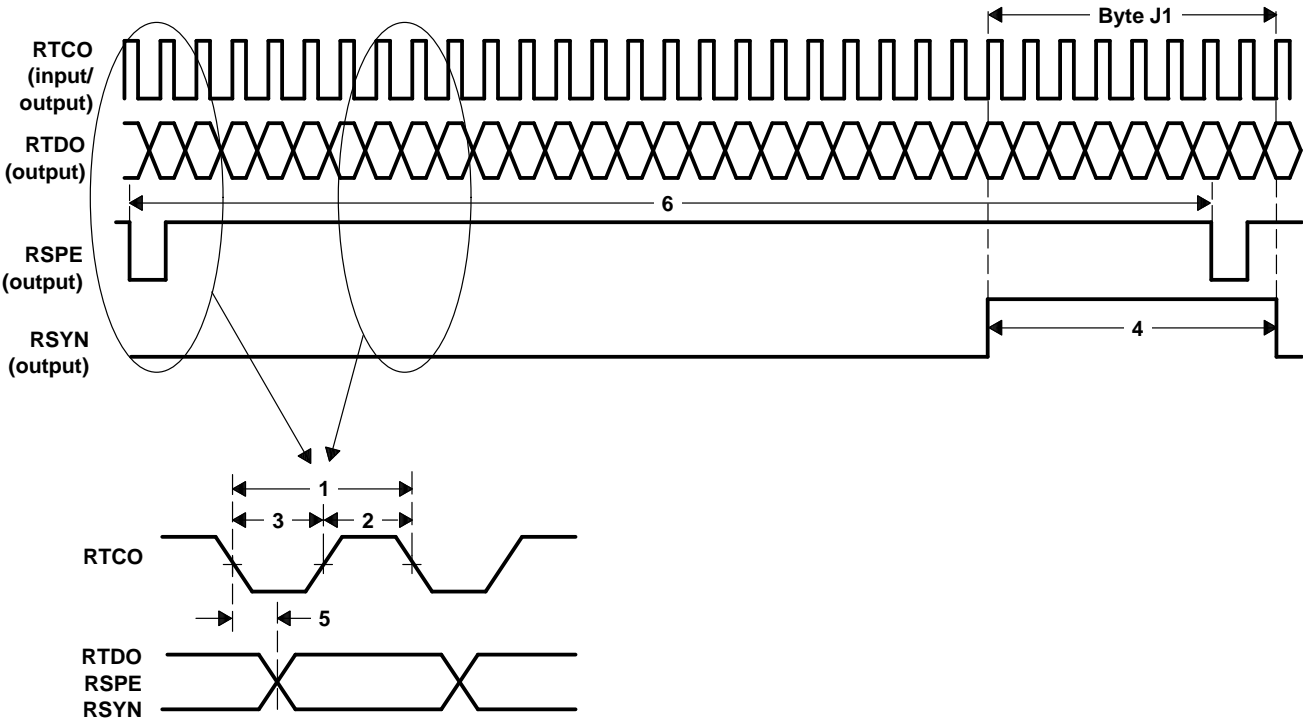


Figure 13. Terminal Serial SPE-Only Output Timing

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timing requirements,  $C_L = 15$  pF (see Note 4 and Figure 14)

| NO. |   | MIN | NOM   | MAX | UNIT          |
|-----|---|-----|-------|-----|---------------|
| 1   | $t_c(\text{TTCI})$ Clock cycle time, TTCI   |     | 19.29 |     | $\mu\text{s}$ |
| 2   | $t_w(\text{TTCIH})$ Pulse duration, TTCI high   |     | 9.65  |     | ns            |
| 3   | $t_w(\text{TTCIL})$ Pulse duration, TTCI low  |     | 9.65  |     | ns            |
| 4   | $t_w(\text{TSYNH})$ Pulse duration, TSYN high   |     |       |     | ns            |
| 5   | $t_{su}(\text{TTDI})$ Setup time, TTDI valid before TTCI $\uparrow$                         |     |       |     | $\mu\text{s}$ |
| 5   | $t_{su}(\text{TSPE})$ Setup time, TSPE valid before TTCI $\uparrow$                         |     |       |     | ns            |
| 5   | $t_{su}(\text{TSYN})$ Setup time, TSYN valid before TTCI $\uparrow$                         |     |       |     | ns            |
| 6   | $t_h(\text{TTDI})$ Hold time, TTDI valid after TTCI $\uparrow$                              |     |       |     | ns            |
| 6   | $t_h(\text{TSPE})$ Hold time, TSPE valid after TTCI $\uparrow$                              |     |       |     | $\mu\text{s}$ |
| 6   | $t_h(\text{TSYN})$ Hold time, TSYN valid after TTCI $\uparrow$                              |     |       |     | ns            |
| 7   | $t_d(\text{TSPE})_{\text{GAP}}$ Delay time, gap from TSPE $\downarrow$ to TSPE $\downarrow$ |     |       |     | ns            |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

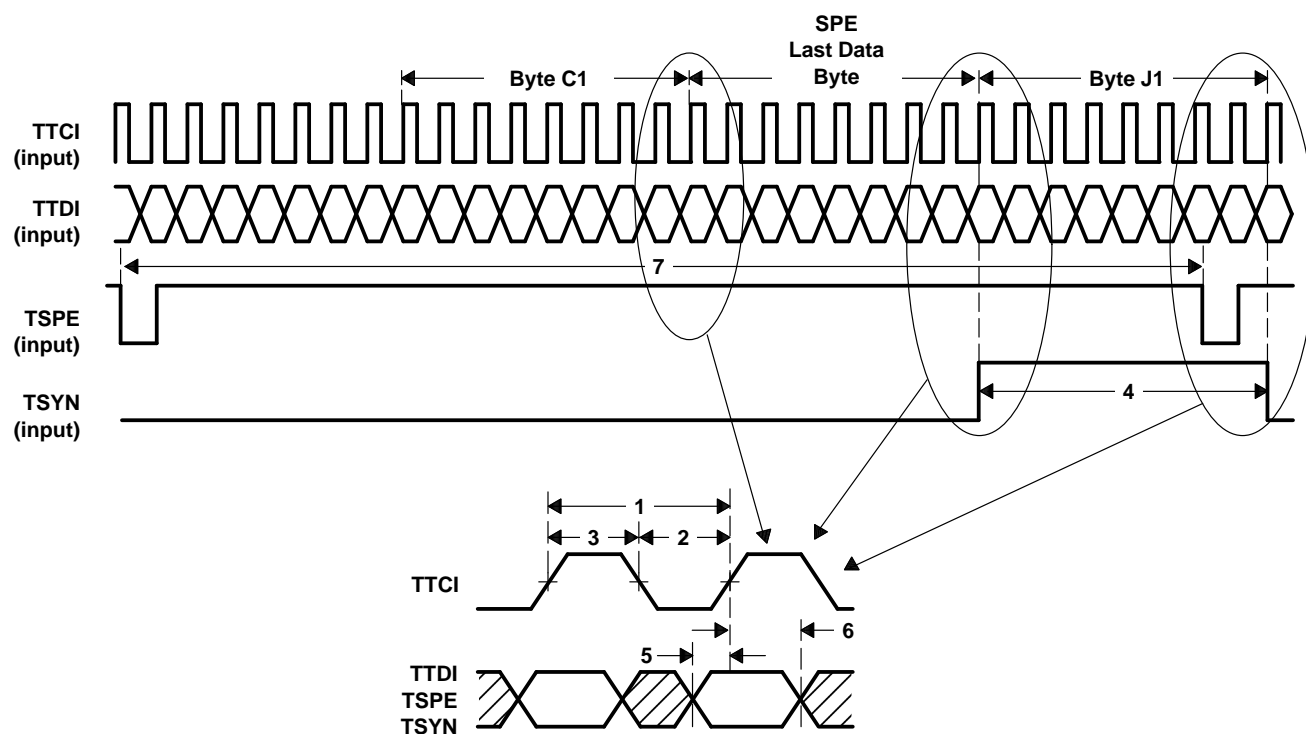


Figure 14. Terminal Serial SPE-Only Input Timing

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operating characteristics,  $C_L = 15\text{ pF}$  (see Note 4 and Figure 15)

| NO. |   | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1   | $t_d(\text{TPCO})$ Delay time, $\text{RTCO}\downarrow$ to $\text{TPCO}\uparrow$ |     |     | ns   |

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

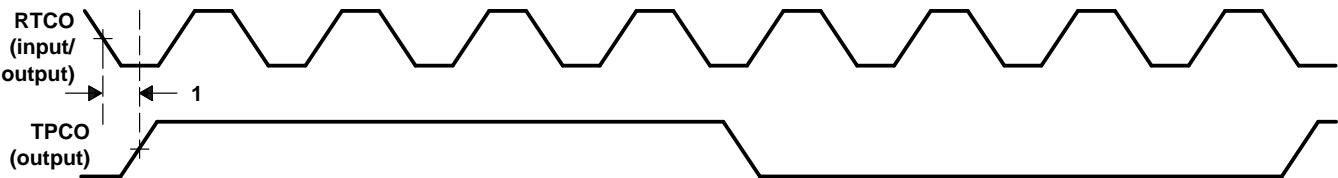


Figure 15. Receive-Terminal-Clock Output Timing

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timing requirements,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 16)

| NO. |   | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1   | $t_{w(\text{ALEH})}$ Pulse duration, ALE high   |     |     | ns   |
| 2   | $t_{w(\text{WRL})}$ Pulse duration, $\overline{\text{WR}}$ low  |     |     | ns   |
| 3   | $t_{su(\text{AD})1}$ Setup time, AD7–AD0 valid before ALE $\downarrow$                                |     |     | ns   |
| 4   | $t_{su(\text{AD})2}$ Setup time, AD7–AD0 valid before $\overline{\text{WR}}\downarrow$                |     |     | ns   |
| 5   | $t_{h(\text{AD})1}$ Hold time, AD7–AD0 valid after ALE $\downarrow$                                   |     |     | ns   |
| 6   | $t_{h(\text{AD})2}$ Hold time, AD7–AD0 valid after $\overline{\text{WR}}\uparrow$                     |     |     | ns   |
| 7   | $t_{d(\text{ALE})}$ Delay time, $\overline{\text{WR}}\uparrow$ to ALE $\uparrow$                      |     |     | ns   |
| 8   | $t_{d(\text{WR})1}$ Delay time, ALE $\downarrow$ to $\overline{\text{WR}}\downarrow$                  |     |     | ns   |
| 9   | $t_{d(\text{WR})2}$ Delay time, $\overline{\text{SEL}}\downarrow$ to $\overline{\text{WR}}\downarrow$ |     |     | ns   |
| 10  | $t_{d(\text{SEL})}$ Delay time, $\overline{\text{WR}}\uparrow$ to $\overline{\text{SEL}}\uparrow$     |     |     | ns   |

† RDY goes low when the address being written to corresponds to a RAM location but remains high during status or control register access.

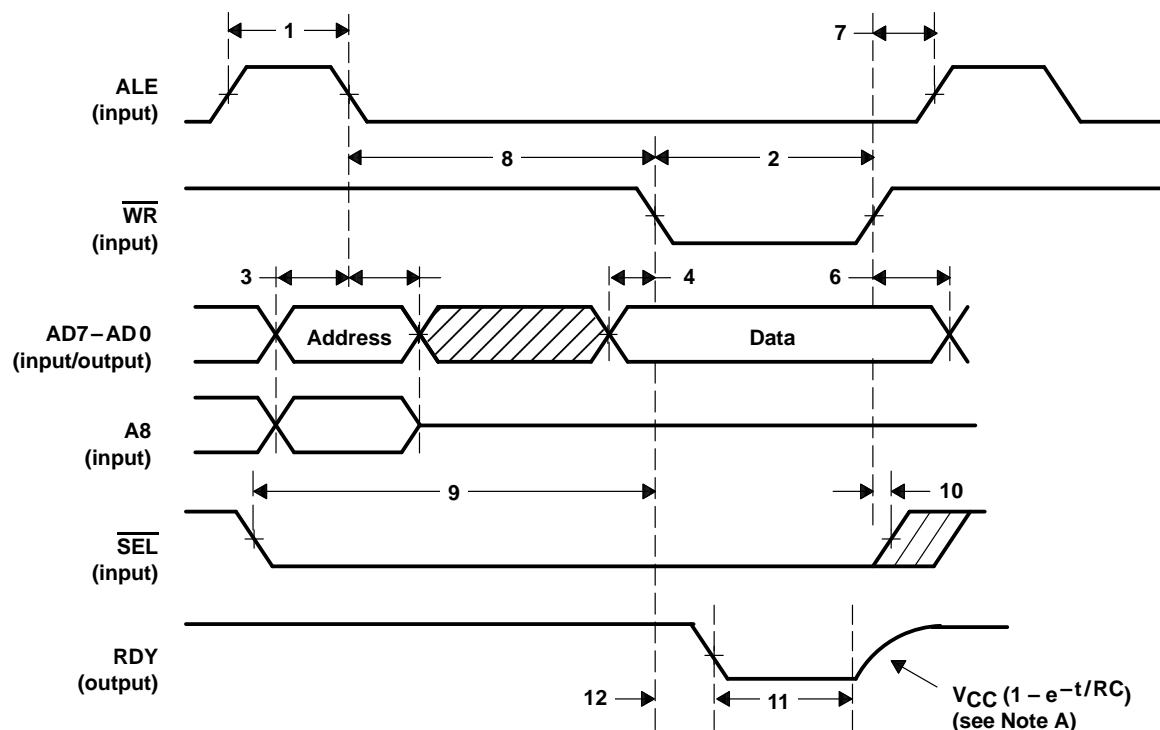
NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

operating characteristics,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 16)

| NO. |  | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 11  | $t_{w(\text{RDYL})}$ Pulse duration, RDY low†  |     |     | ns   |
| 12  | $t_{d(\text{RDY})}$ Delay time, $\overline{\text{WR}}\downarrow$ to RDY $\downarrow$ |     |     | ns   |

† RDY goes low when the address being written to corresponds to a RAM location but remains high during status or control register access.

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.



NOTE A: Open-drain rise time is dependent upon external pullup resistor and load capacitance.

Figure 16. Microprocessor Write-Cycle Timing

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timing requirements,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 17)

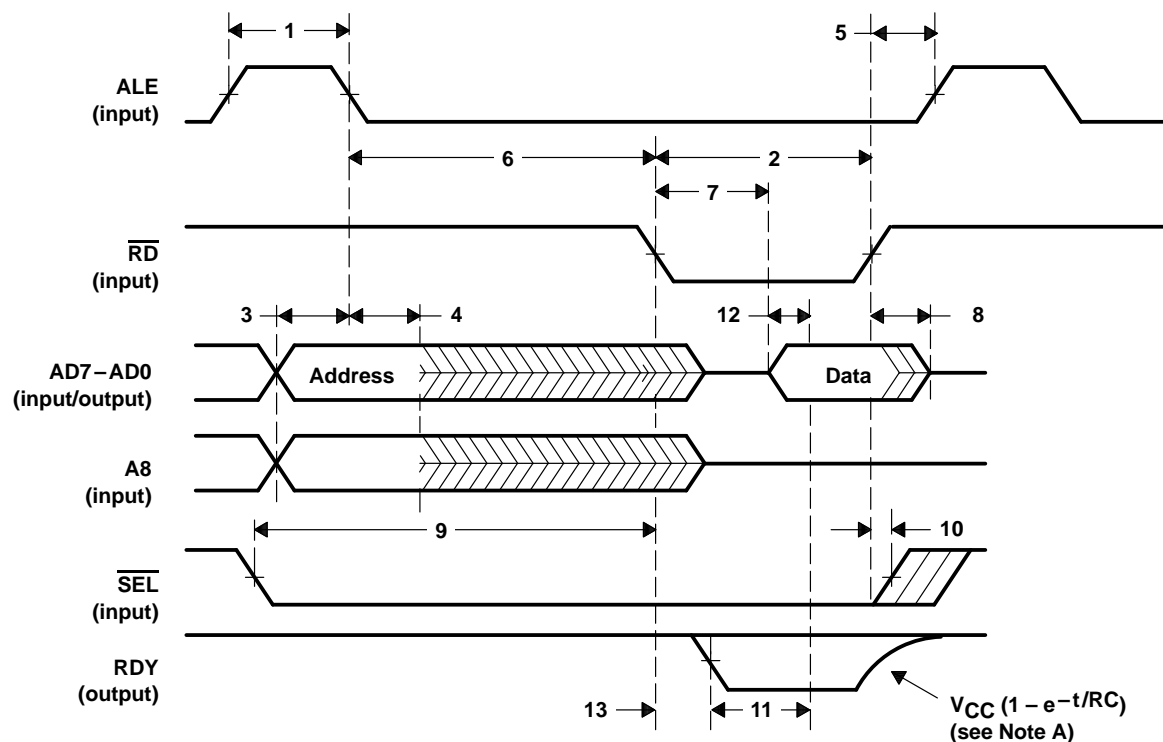
| NO. |   | MIN | MAX | UNIT          |
|-----|---|-----|-----|---------------|
| 1   | $t_{w(ALEH)}$ Pulse duration, ALE high  |     |     | $\mu\text{s}$ |
| 2   | $t_{w(RDL)}$ Pulse duration, $\overline{RD}$ low                              |     |     | ns            |
| 3   | $t_{su(AD)}$ Setup time, AD7–AD0 valid before $\overline{ALE}\downarrow$      |     |     | ns            |
| 4   | $t_h(AD)$ Hold time, AD7–AD0 valid after $\overline{ALE}\downarrow$           |     |     | ns            |
| 5   | $t_d(ALE)$ Delay time, $\overline{RD}\uparrow$ to $\overline{ALE}\uparrow$    |     |     | ns            |
| 6   | $t_d(RD)$ Delay time, $\overline{ALE}\downarrow$ to $\overline{RD}\downarrow$ |     |     | ns            |
| 7   | $t_d(AD)$ Delay time, $\overline{RD}\downarrow$ to AD7–AD0 invalid            |     |     | ns            |
| 8   | $t_d(AD)$ Delay time, $\overline{RD}\uparrow$ to AD7–AD0                      |     |     | ns            |
| 9   | $t_d(RD)$ Delay time, $\overline{SEL}\downarrow$ to $\overline{RD}\downarrow$ |     |     | ns            |
| 10  | $t_d(SEL)$ Delay time, $\overline{RD}\uparrow$ to $\overline{SEL}\uparrow$    |     |     | ns            |

† RDY goes low when the address being written to corresponds to a RAM location but remains high during status or control-register access.

NOTE 4: Timing intervals are measured at  $(V_{OH}-V_{OL})/2$  or  $(V_{IH}-V_{IL})/2$  as applicable.

operating characteristics,  $C_L = 15 \text{ pF}$  (see Note 4 and Figure 17)

| NO. |  | MIN | MAX | UNIT |
|-----|--|-----|-----|------|
| 11  | $t_{w(RDYL)}$ Pulse duration, RDY low†                   |     |     | ns   |
| 12  | $t_d(RDY)$ Delay time, AD7–AD0 to RDY↑                   |     |     | ns   |
| 13  | $t_d(RDY)$ Delay time, $\overline{RD}\downarrow$ to RDY↓ |     |     | ns   |



NOTE A: Open-drain rise time is dependent upon external pullup resistor and load capacitance.

Figure 17. Microprocessor Read-Cycle Timing

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operating characteristics, C<sub>L</sub> = 15 pF (see Note 4 and Figure 18)

| NO. |   | MIN | MAX | UNIT |
|-----|---|-----|-----|------|
| 1   | t <sub>d</sub> (INT)      Delay time, $\overline{RD}\uparrow$ to INT $\downarrow$ |     |     | ns   |

NOTE 4: Timing intervals are measured at (V<sub>OH</sub>–V<sub>OL</sub>)/2 or (V<sub>IH</sub>–V<sub>IL</sub>)/2 as applicable.

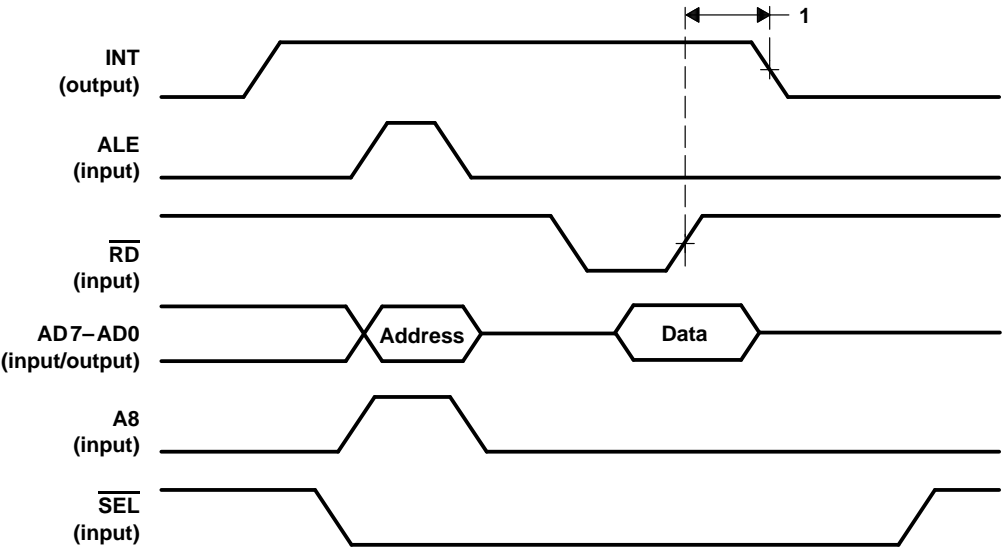


Figure 18. Microprocessor-Interrupt Timing

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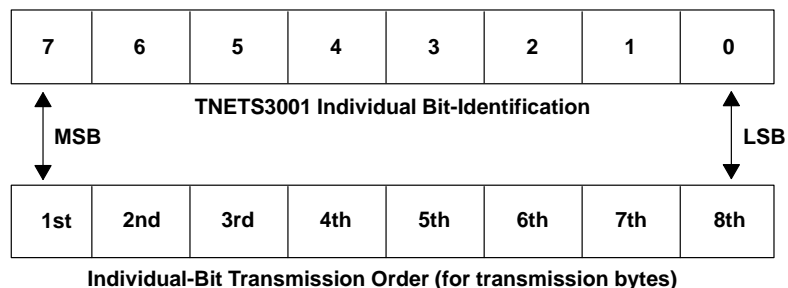
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All address locations are given in hex (h). The relationship between a transmission byte (for example, C1) and TNETS3001 individual bit locations is shown below:



### TNETS3001 register-bit map

| ADDRESS<br>(hex) | MODE† | BIT 7  | BIT 6 | BIT 5 | BIT 4    | BIT 3 | BIT 2    | BIT 1        | BIT 0  | COMMENT‡ |
|------------------|-------|--|-------|-------|----------|-------|----------|--------------|--------|----------|
| 0F0              | R/W   | RLOC   | RNPTR | RPAIS | RLAIS    | RLOP  | RLOF     | ROOF         | RLOS   | SR0      |
| 0F1              | R/W   | Same as 0F0 except does not reset on read; write ones to reset individual bits |       |       |          |       |          |              |        | SR0      |
| 0F2              | R/W   | INT  | RTNEW | RPNEW | RPYE     | RFERF | RAPS     |              |        | SR1      |
| 0F3              | R/W   | Same as 0F2 except does not reset on read; write ones to reset individual bits |       |       |          |       |          |              |        | SR1      |
| 0F4              | R     | Same as 0F0 except unlatched values  |       |       |          |       |          |              |        | SR0      |
| 0F5              | R     | Same as 0F2 except unlatched values  |       |       |          |       |          |              |        | SR1      |
| 0F8              | R/W   | RRSD   | RRLD  | RRE1  | RRE2     | RPATH | RRAPS    | RRPTR        | TRLOOP | CR0      |
| 0F9              | R/W   | RRF1   | RRC1  | RRZ1  | RRZ2     | RRAIS | LTE      | RRFRM        | RRB1   | CR1      |
| 0FA              | R/W   | STS1   | PARA  | HINT  | TRFERF   | ALTOW | TIEN     | PIEN         | –VE    | CR2      |
| 1F0              | R/W   | TLOC   | TNPTR | TPAIS | TLAIS    | TLOP  | TLOF     | TOOF         | TLOS   | SR2      |
| 1F1              | R/W   | Same as 1F0 except does not reset on read; write ones to reset individual bits |       |       |          |       |          |              |        | SR2      |
| 1F4              | R     | Same as 1F0 except unlatched values  |       |       |          |       |          |              |        | SR2      |
| 1F8              | R/W   | TRSD   | TRLD  | TRE1  | TRE2     | TPATH | TRAPS    | EXAPS        | RTLOOP | CR3      |
| 1F9              | R/W   | TRF1   | TRC1  | TRZ1  | TRZ2     | TRAIS | PTE      | <u>RXRTM</u> | RRB2   | CR4      |
| 1FA              | R/W   | SPE  | TCLK  | RCLK  | reserved | TXRTM | reserved | INC          | DEC    | CR5      |
| 1FB              | R/W   | TRFRM  | TRERR | TAIS  | unused   | RE2A  | RA2E     | TE2E         | TA2E   | CR6      |

† Read/write (R/W); Read only (R)

‡ SR = Status Register; CR = Control Register

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## PRINCIPLES OF OPERATION

### register-bit map descriptions

#### control register 0

| ADDRESS<br>(hex) | BIT | NAME   | DESCRIPTION  |   | COMMENTS  |
|------------------|-----|--------|--|---|---|
|                  |     |        | BIT EQUAL TO 1 (HIGH)  | BIT EQUAL TO 0 (LOW)  |   |
| 0F8              | 7   | RRSD   | Receiver terminal-side section-datacom bytes control. Outgoing terminal data has section-datacom bytes from the RAM (D1–D3). | Outgoing terminal data has section-datacom bytes from the receive line.         | See Note 6  |
| 0F8              | 6   | RRLD   | Receiver terminal-side line-datacom bytes control. Outgoing terminal data has line-datacom bytes from the RAM (D4–D12).      | Outgoing terminal data has line-datacom bytes from the receive line.            | See Note 6  |
| 0F8              | 5   | RRE1   | Receiver terminal-side E1 byte control. Outgoing terminal data has section-orderwire byte from the RAM. RA2E must be low.    | Outgoing terminal data has section-orderwire byte from the receive line.        | See Note 6  |
| 0F8              | 4   | RRE2   | Receiver terminal-side E2 byte control. Outgoing terminal data has line-orderwire byte from the RAM.                         | Outgoing terminal data has line-orderwire byte from the receive line.           | See Note 6  |
| 0F8              | 3   | RPATH  | Receiver terminal-side path-overhead control. Outgoing terminal data has path-overhead (except H4) bytes from the RAM.       | Outgoing terminal data has path-overhead bytes from the receive line.           | Multiframe-indicator byte (H4) always passes through  |
| 0F8              | 2   | RRAPS  | Receiver terminal-side APS bytes control. Outgoing terminal data has APS bytes (K1 and K2) from the RAM.                     | Outgoing terminal data has APS bytes (K1 and K2) from the receive line.         | See Note 6  |
| 0F8              | 1   | RRPTR  | Receiver terminal-side pointer control. Outgoing terminal data has pointer bytes (H1 and H2) from the RAM.                   | Outgoing terminal data has pointer bytes from the receive line or recalculated. | See Notes 6 and 7. Only pointer value is introduced.  |
| 0F8              | 0   | TRLOOP | Transmit-receive loopback enable. Line output looped back to receive line input.   | Normal operation  | $\overline{\text{RFRI}}$ is disabled during loopback. |

NOTES: 6. The TOH bytes are inserted into the terminal data only in the pass-through mode. In the receive-retiming and SPE-only modes, all TOH bytes except A1, A2, E1, H1 and H2 are set to zero.

7. This mode does not modify the payload. It inserts H1 and H2 bytes from insert RAM locations and can be used for self test.

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## PRINCIPLES OF OPERATION

### control register 1

| ADDRESS<br>(hex) | BIT | NAME  | DESCRIPTION   |  | COMMENTS   |
|------------------|-----|-------|---|--|--|
|                  |     |       | BIT EQUAL TO 1 (HIGH)   | BIT EQUAL TO 0 (LOW)   |  |
| 0F9              | 7   | RRF1  | Receiver terminal-side F1 byte control. Outgoing terminal data has section-user byte (F1) from the RAM.   | Outgoing terminal data has section-user byte from the receive line.      | See Note 6   |
| 0F9              | 6   | RRC1  | Receiver terminal-side C1 byte control. Outgoing terminal data has STS-1 ID byte (C1) from the RAM.       | Outgoing terminal data has STS-1 ID byte (C1) from the receive line.     | See Note 6   |
| 0F9              | 5   | RRZ1  | Receiver terminal-side Z1 byte control. Outgoing terminal data has growth-byte Z1 from the RAM.           | Outgoing terminal data has growth-byte Z1 from the receive line.         | See Note 6   |
| 0F9              | 4   | RRZ2  | Receiver terminal-side Z2 byte control. Outgoing terminal data has growth-byte Z2 from the RAM.           | Outgoing terminal data has growth-byte Z2 from the receive line.         | See Note 6   |
| 0F9              | 3   | RRAIS | Receiver terminal-side AIS output control. Enables automatic insertion of AIS into outgoing terminal data | Disables automatic insertion of AIS into outgoing terminal data          | See Note 8   |
| 0F9              | 2   | LTE   | Line-terminating-equipment enable. Enables AIS transmission and introduction.                             | Disable line-terminating equipment for AIS transmission and introduction | Section-terminating equipment if LTE = 0 and PTE = 0 |
| 0F9              | 1   | RRFRM | Receive terminal-side framing-byte control. Outgoing terminal data has framing bytes regenerated.         | Outgoing terminal data has framing bytes from the receive line.          |  |
| 0F9              | 0   | RRB1  | Receive terminal-side B1 parity-byte control. Outgoing terminal data has B1 byte recalculated.            | Outgoing terminal data has B1 byte from the receive line.                | See Note 6   |

- NOTES: 6. The TOH bytes are inserted into the terminal data only in the pass-through mode. In the receive-retiming and SPE-only modes, all TOH bytes except A1, A2, E1, H1 and H2 are set to zero.
8. The SPE bytes are set to all ones during the SPE and RX retiming modes. All TOH bytes except A1, A2, E1, H1, and H2 are set to zero.

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## PRINCIPLES OF OPERATION

### control register 2

| ADDRESS<br>(hex) | BIT | NAME   | DESCRIPTION   |  | COMMENTS                                     |
|------------------|-----|--------|---|--|--|
|                  |     |        | BIT EQUAL TO 1 (HIGH)   | BIT EQUAL TO 0 (LOW)   |  |
| 0FA              | 7   | STS1   | STS-1/STS-N mode control, line side in STS-1 mode. Received data is descrambled and transmit data is scrambled. Received B1 contains BIP-8 parity. Transmit B1 is recalculated. | Line-side in STS-N mode. Data is not scrambled. Received B1 byte contains BIP-8 errors. Transmit B1 byte contains error mask.    | Controls both receive and transmit line side |
| 0FA              | 6   | PARA   | Parallel/serial-mode control. Terminal-side interface is parallel. In receive direction, both serial and parallel interfaces are active.  | Terminal-side interface is serial. In receive direction, both serial and parallel interfaces are active except in SPE-only mode. |  |
| 0FA              | 5   | HINT   | Hardware-interrupt enable. Enables hardware interrupt.  | Disables hardware interrupt  |  |
| 0FA              | 4   | TRFERF | Transmit line-side FERF enable. Enables automatic introduction of line FERF into line-side output.  | Disables automatic introduction to line FERF into line-side output   | See Note 9                                   |
| 0FA              | 3   | ALTOW  | Orderwire-mode control. Selects alternate orderwire-interface frame coincident with data MSB.   | Selects normal orderwire-interface frame ahead of data MSB by one bit  | See Figures 3 and 4                          |
| 0FA              | 2   | TIEN   | Transport-layer-interrupt enable. Enables transport-layer interrupt.  | Disables transport-layer interrupt   | See Note 10                                  |
| 0FA              | 1   | PIEN   | Path-layer-interrupt enable. Enables transport-layer interrupt.   | Disables path-layer interrupt  | See Note 11                                  |
| 0FA              | 0   | VE     | Interrupt-edge control. Interrupts on both positive and negative edges of alarm.  | Interrupts only on positive-going edge of alarms   |  |

- NOTES: 9. The conditions for FERF transmission are receive loss of signal, receive loss of frame, and/or receive line AIS.
10. The conditions for transport-layer interrupt are transport-layer alarms (RLOS, ROOF, RLOF, RLAI, RFERF, RPAIS, and RLOP), overflow of transport-layer performance monitors (receive B1 counter, receive B2 counter, transmit B1 counter, and transmit B2 counter), and new debounced values of C1, F1, K1, K2, Z1, and Z2 receive-path-overhead bytes.
11. The conditions for path-layer interrupt are path yellow alarm, overflow of path-layer performance monitors (receive B3 counter, receive FEBE counter, and transmit B3 counter), and new debounced values of C2, F2, Z3, Z4, and Z5 receive-path overhead bytes.

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### PRINCIPLES OF OPERATION

#### control register 3

| ADDRESS<br>(hex) | BIT | NAME   | DESCRIPTION  |  | COMMENTS  |
|------------------|-----|--------|--|--|---|
|                  |     |        | BIT EQUAL TO 1 (HIGH)  | BIT EQUAL TO 0 (LOW)   |   |
| 1F8              | 7   | TRSD   | Transmit line-side section-datacom-bytes control. Outgoing line data has section-datacom bytes from the section-datacom interface (D1 – D3). | Outgoing line data has section-datacom bytes from the terminal.  | See Notes 12, 13, and 15                              |
| 1F8              | 6   | TRLD   | Transmit line-side line-datacom-bytes control. Outgoing line data has line-datacom bytes from the line-datacom interface (D4 – D12).         | Outgoing line data has line-datacom bytes from the terminal.     | See Notes 12, 13, and 15                              |
| 1F8              | 5   | TRE1   | Transmit line-side line E1 byte control. Outgoing line data has section-orderwire byte from the orderwire interface.                         | Outgoing line data has section-orderwire byte from the terminal. | See Notes 12, 13, and 15                              |
| 1F8              | 4   | TRE2   | Transmit line-side E2 byte control. Outgoing line data has line-orderwire byte from the orderwire interface.                                 | Outgoing line data has line-orderwire byte from the terminal.    | See Notes 12, 13, and 15                              |
| 1F8              | 3   | TPATH  | Transmit line-side E2 byte control. Outgoing line data has path-overhead (except H4) bytes from the RAM.                                     | Outgoing line data has path-overhead bytes from the terminal.    | Multiframe-indicator byte (H4) always passes through. |
| 1F8              | 2   | TRAPS  | Transmit line-side APS control. Outgoing line data has APS bytes from the RAM.   | Outgoing line data has APS bytes from the terminal.              | See Notes 13, 14, and 15                              |
| 1F8              | 1   | TRAPS  | External APS-to-RAM enable. APS bytes from the orderwire interface loaded to the RAM every frame.  | RAM location for APS bytes not modified                          | See Notes 13, 14, and 15                              |
| 1F8              | 0   | RTLOOP | Receive-to-transmit loopback enable. Receive terminal output looped back to transmit terminal input.   | Normal operation   |   |

- NOTES: 12. Orderwire or datacom channels can come either from the terminal or the respective serial interface.  
 13. These channels cannot come from the terminal in the SPE-only mode.  
 14. Transmit line APS bytes have three sources: terminal, orderwire interface, or RAM (using microprocessor interface).  
 15. These features are not available in the SPE-only mode.

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### PRINCIPLES OF OPERATION

#### *control register 4*

| ADDRESS<br>(hex) | BIT | NAME                      | DESCRIPTION   |  | COMMENTS  |
|------------------|-----|---------------------------|---|--|---|
|                  |     |                           | BIT EQUAL TO 1 (HIGH)   | BIT EQUAL TO 0 (LOW)   |   |
| 1F9              | 7   | TRF1                      | Transmit line-side F1 byte control. Outgoing line data has section-user byte (F1) from the RAM. | Outgoing line data has section-user byte from the terminal.              | See Note 16   |
| 1F9              | 6   | TRC1                      | Transmit line-side C1 byte control. Outgoing line data has STS-1 ID byte (C1) from the RAM.     | Outgoing line data has STS-1 ID byte (C1) from the terminal.             | See Note 16   |
| 1F9              | 5   | TRZ1                      | Transmit line-side Z1 byte control. Outgoing line data has growth-byte Z1 from the RAM.         | Outgoing line data has growth-byte Z1 from the terminal.                 | See Note 16   |
| 1F9              | 4   | TRZ2                      | Transmit line-side Z2 byte control. Outgoing line data has growth-byte Z2 from the RAM.         | Outgoing line data has growth-byte Z2 from the terminal.                 | See Note 16   |
| 1F9              | 3   | TRAIS                     | Transmit line-side AIS enable. Enables automatic insertion of AIS into outgoing line data.      | Disables automatic insertion of AIS into outgoing line data              |   |
| 1F9              | 2   | PTE                       | Transmit line-side AIS enable. Enables automatic insertion of AIS into outgoing line data.      | Disable path-terminating equipment for AIS transmission and introduction | Section-terminating equipment if LTE = 0 and PTE = 0          |
| 1F9              | 1   | $\overline{\text{RXRTM}}$ | Receive retiming mode control. Disables receive-retiming and SPE-only modes.                    | Enables receive-retiming and SPE-only modes                              | See interfaces and operating modes section of this data sheet |
| 1F9              | 0   | RRB2                      | Receive terminal-side B2 byte control. Outgoing terminal data has B2 byte recalculated.         | Outgoing terminal data has B2 byte from the receive line.                | See Note 17   |

NOTES: 16. These bytes cannot come from the terminal in the SPE-only mode.

17. These features are not available in the receive-retiming and SPE-only modes.

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## PRINCIPLES OF OPERATION

### control register 5

| ADDRESS<br>(hex) | BIT | NAME  | DESCRIPTION  |  | COMMENTS  |
|------------------|-----|-------|--|--|---|
|                  |     |       | BIT EQUAL TO 1 (HIGH)  | BIT EQUAL TO 0 (LOW)   |   |
| 1FA              | 7   | SPE   | SPE-only/STS-1 mode control. <u>SPE</u> -only mode in the terminal side <u>RXRTM</u> bit must be low.    | STS-1 mode in the terminal side  |   |
| 1FA              | 6   | TCLK  | Transmitter clock-source select. TLCO derived from TLCI.   | TLCO is derived from TTCI in serial mode or TPCI in parallel mode.       |   |
| 1FA              | 5   | RCLK  | Receiver clock-source select. <u>RTCO</u> and TPCO are derived from TLCI. <u>RXRTM</u> bit must be low.  | RTCO and TPCO are derived from RLCI.                                     |   |
| 1FA              | 4   |       | Not defined  | Normal operation   | This bit must be set low.   |
| 1FA              | 3   | TXRTM | Transmit-retiming-mode control. Enables automatic pointer justifications by transmit-retiming circuitry. | Disables automatic-pointer justifications by transmit-retiming circuitry | See Note 18   |
| 1FA              | 2   |       | Not defined  | Normal operation   | This bit must be set low.   |
| 1FA              | 1   | INC   | Increment-pointer control. Forces pointer increments in line side.                                       | Normal operation   | These bits must be reset two frames after being set to prevent multiple pointer justifications (see Note 18). |
| 1FA              | 0   | DEC   | Decrement-pointer control. Forces pointer decrements in line side.                                       | Normal operation   |   |

NOTE 18: These bits must be used with caution or an error in transmission can result.

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## PRINCIPLES OF OPERATION

### *control register 6*

| ADDRESS<br>(hex) | BIT | NAME   | DESCRIPTION  |  | COMMENTS   |
|------------------|-----|--------|--|--|--|
|                  |     |        | BIT EQUAL TO 1 (HIGH)  | BIT EQUAL TO 0 (LOW)   |  |
| 1FB              | 7   | TRFRM  | Transmit line-side framing control. Enables automatic generation of the transmit-framing bytes (A1 and A2).                              | Disables automatic generation of the transmit-framing bytes (A1 and A2)                    | See Note 18                                      |
| 1FB              | 6   | TRERR  | Transmit line-side parity-error-mask control. Enables automatic reset of transmit line B1, B2 and B3 error masks after one transmission. | Disables automatic reset of transmit line B1, B2 and B3 error masks after one transmission | See Note 18                                      |
| 1FB              | 5   | TAIS   | Transmit line-side AIS control. Introduces AIS into transmit line.   | Normal operation   | LTE and PTE bits determine line AIS or path AIS. |
| 1FB              | 4   | Unused |  |  |  |
| 1FB              | 3   | RE2A   | Receiver E1-to-AIS mode control. Enables received line E1 byte to be interpreted as AIS-transmission byte.                               | Disables received line E1 byte to be interpreted as AIS-transmission byte                  |  |
| 1FB              | 2   | RA2E   | Receiver E1-to-AIS mode control. Enables received line E1 byte to be interpreted as AIS-transmission byte.                               | Disables AIS transmission using receive terminal E1 byte                                   |  |
| 1FB              | 1   | TE2A   | Transmitter E1-to-AIS mode control. Enables transmit terminal E1 byte to be interpreted as AIS-transmission byte.                        | Disables transmit terminal E1 byte to be interpreted as AIS-transmission byte              |  |
| 1FB              | 0   | TA2E   | Transmitter AIS-to-E1 mode control. Enables AIS transmission using transmit line E1 byte.  | Disables AIS transmission using transmit line E1 byte                                      |  |

NOTE 18: These bits must be used with caution or an error in transmission can result.

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### PRINCIPLES OF OPERATION

*status register 0 (see Notes 19, 20, and 21)*

| ADDRESS<br>(hex) | BIT | SYMBOL | NAME                    | CONDITIONS   |   |
|------------------|-----|--------|-------------------------|--|---|
|                  |     |        |                         | ENTER  | EXIT  |
| 0F0, 0F1,<br>0F4 | 7   | RLOC   | Receive loss of clock   | 200 ns of no transitions in receive-line clock RLCI  | Any transition of the receive-line clock RLCI   |
| 0F0, 0F1         | 6   | RNPTR  | Receive new pointer     | A new-pointer value due to new-data flag or three consecutive frames of different pointer values   | Microprocessor read from address 0F0 or writing 1 to bit 6 of address 0F2   |
| 0F0, 0F1,<br>0F4 | 5   | RPAIS  | Receive path AIS        | Three consecutive frames of all ones in H1 and H2 bytes  | NDF with valid pointer or three successive frames with valid pointer  |
| 0F0, 0F1,<br>0F4 | 4   | RLAIS  | Receive line AIS        | Five consecutive frames of 111 in the bits 2,1,0 (6,7,8 transmission-bit standard) of the K2 byte  | Five consecutive frames of patterns other than 111 in the bits 2,1,0 (6,7,8 transmission-bit standard) of the K2 byte           |
| 0F0, 0F1,<br>0F4 | 3   | RLOP   | Receive loss of pointer | Eight consecutive frames of invalid pointer or NDF   | Three consecutive frames of valid pointer   |
| 0F0, 0F1,<br>0F4 | 2   | RLOF   | Receive loss of frame   | Eight consecutive frames of out-of-frame condition   | Eight consecutive frames of in-frame condition  |
| 0F0, 0F1,<br>0F4 | 1   | ROOF   | Receive out of frame    | Failure to acquire valid framing pattern for four consecutive frames   | Valid framing pattern exactly 6480 bits apart   |
| 0F0, 0F1,<br>0F4 | 0   | RLOS   | Receive loss of signal  | STS-1 mode. 20 $\mu$ s of all zeros in the scrambled data RLDI or RXLOS low.<br>STS-N mode. 6480 bits of all zeros or all ones or RXLOS low. | STS-1 mode. A valid framing pattern in the scrambled data and RXLOS high.<br>STS-N mode. Any transition in RLDI and RXLOS high. |

- NOTES: 19. The address 0F0 contains latched values of these status bits, which reset on read.  
 20. The address 0F1 contains latched values of these status bits, but do not reset on read. Write one to an individual bit to reset. Write back read value to reset the entire register.  
 21. The address 0F4 contains unlatched values of these status bits. The information is transient.

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### PRINCIPLES OF OPERATION

*status register 1 (see Notes 22, 23, and 24)*

| ADDRESS<br>(hex) | BIT | SYMBOL | NAME   | CONDITIONS   |  |
|------------------|-----|--------|--|--|--|
|                  |     |        |  | ENTER  | EXIT   |
| 0F2, 0F3         | 7   | INT    | Interrupt  | Rising-edge/both-edges alarms,<br>new debounced-overhead bytes or<br>performance-monitor overflow                | Microprocessor read from address<br>0F2 or writing one to bit 7 of<br>address 0F3                                      |
| 0F2, 0F3         | 6   | RTNEW  | Receive new<br>debounced-transport-<br>overhead byte | Any new debounced value for the<br>following TOH bytes: C1, F1, K1, K2,<br>Z1, and Z2                            | Microprocessor read from<br>address 0F2 or writing one to<br>bit 6 of address 0F3                                      |
| 0F2, 0F3         | 5   | RPNEW  | Receive new<br>debounced-path-<br>overhead byte      | Any new debounced value for the<br>following POH bytes: C2, F2, Z3, Z4,<br>and Z5                                | Microprocessor read from<br>address 0F2 or writing one to<br>bit 5 of address 0F3                                      |
| 0F2, 0F3,<br>0F5 | 4   | RPYE   | Receive path yellow                                  | Ten consecutive frames of 1 in bit 3<br>(bit 5 transmission-bit standard) of<br>the G1 byte                      | Ten consecutive frames of zero<br>in the bit 3 (bit 5 transmission-bit<br>standard) of the G1 byte                     |
| 0F2, 0F3,<br>0F5 | 3   | RFERF  | Receive FERF   | Five consecutive frames of 110 in the<br>bits 2, 1, 0 (bits 6, 7, 8 transmission-bit<br>standard) of the K2 byte | Five consecutive frames of 000 or<br>111 in the bits 2,1,0 (bits 6,7,8<br>transmission-bit standard) of the<br>K2 byte |
| 0F2, 0F3,<br>0F5 | 2   | RAPS   | Receive APS bytes<br>failure                         | Twelve successive frames with no three<br>consecutive frames containing identical<br>APS bytes                   | Three consecutive frames<br>containing identical APS bytes   |
| 0F2, 0F3,<br>0F5 | 1   | unused |  |  |  |
| 0F2, 0F3,<br>0F5 | 0   | unused |  |  |  |

- NOTES: 22. The address 0F2 contains latched values of these status bits, which reset on read.  
 23. The address 0F3 contains latched values of these status bits, but do not reset on read. Write one to individual bit to reset. Write back read value to reset the entire register.  
 24. The address 0F5 contains unlatched values of these status bits.

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## PRINCIPLES OF OPERATION

*status register 2 (see Notes 25, 26, 27, and 28)*

| ADDRESS<br>(hex) | BIT | SYMBOL | NAME                     | CONDITIONS   |   |
|------------------|-----|--------|--------------------------|--|---|
|                  |     |        |                          | ENTER  | EXIT  |
| 1F0, 1F1,<br>1F4 | 7   | TLOC   | Transmit loss of clock   | 200 ns of no transitions in the clock TTCI   | Any transition of the clock TTCI  |
| 1F0, 1F1,<br>1F4 | 6   | TNPTR  | Transmit new pointer     | A new-pointer value due to new-data flag or three consecutive frames of different pointer values |   |
| 1F0, 1F1,<br>1F4 | 5   | TPAIS  | Transmit path AIS        | Three consecutive frames of all ones in H1 and H2 bytes  | NDF with valid pointer or three successive frames with valid pointer              |
| 1F0, 1F1,<br>1F4 | 4   | TLAIS  | Transmit line AIS        | Five consecutive frames of 111 in bits 6, 7, 8 of the K2 byte                                    | Five consecutive frames of patterns other than 111 in bits 6, 7, 8 of the K2 byte |
| 1F0, 1F1,<br>1F4 | 3   | TLOP   | Transmit loss of pointer | Eight consecutive frames of invalid pointer or NDF   | Three consecutive frames of valid pointer   |
| 1F0, 1F1,<br>1F4 | 2   | TLOF   | Transmit loss of frame   | Eight consecutive frames of out-of-frame condition   | Eight consecutive frames of not out-of-frame condition                            |
| 1F0, 1F1,<br>1F4 | 1   | TOOF   | Transmit out of frame    | Failure to acquire valid framing pattern for four consecutive frames                             | Valid framing pattern exactly 6480 bits apart                                     |
| 1F0, 1F1,<br>1F4 | 0   | TLOS   | Transmit loss of signal  | 6480 bits of all zeros or all ones   | Any transition in TTDI  |

- NOTES: 25. The address 1F0 contains latched values of these status bits, which reset on read.  
 26. The address 1F1 contains latched values of these status bits, but do not reset on read. Write one to an individual bit to reset. Write back read value to reset the entire register.  
 27. The address 1F4 contains unlatched values of these status bits.  
 28. None of these alarms, except TLOS, work in the SPE-only mode.

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## PRINCIPLES OF OPERATION

### memory map

#### receive line-overhead byte locations (in hex)

|         |           |     |     |  |         |
|---------|-----------|-----|-----|--|---------|
| Section | A1        | A2  | C1  |  | J1      |
|         | 016       | 017 | 01C |  | 080-0BF |
|         | B1        | E1  | F1  |  | B3      |
|         | 014       | 018 | 01D |  | 0C0     |
|         | D1        | D2  | D3  |  | C2      |
|         | 005       | 006 | 007 |  | 0C1     |
|         | H1        | H2  | H3  |  | G1      |
|         | 011       | 012 | 013 |  | 0C2     |
|         | B2        | K1  | K2  |  | F2      |
|         | 015       | 01E | 01F |  | 0C3     |
|         | D4        | D5  | D6  |  | H4      |
|         | 008       | 009 | 00A |  | 0C4     |
| Line    | D7        | D8  | D9  |  | Z3      |
|         | 00B       | 00C | 00D |  | 0C5     |
|         | D10       | D11 | D12 |  | Z4      |
|         | 00E       | 00F | 010 |  | 0C6     |
|         | Z1        | Z2  | E2  |  | Z5      |
|         | 01A       | 01B | 019 |  | 0C7     |
|         | Transport |     |     |  | Path    |

#### receive insert-overhead byte locations (in hex)

|         |           |     |     |  |                 |
|---------|-----------|-----|-----|--|-----------------|
| Section | A1†       | A2† | C1  |  | J1              |
|         | 036       | 037 | 03C |  | 080-0BF         |
|         | B1†       | E1  | F1  |  | B3              |
|         | 034       | 038 | 03D |  | 0C8             |
|         | D1        | D2  | D3  |  | C2              |
|         | 025       | 026 | 027 |  | 0C9             |
|         | H1        | H2  | H3  |  | G1              |
|         | 031       | 032 | 033 |  | 0CA             |
|         | B2†       | K1  | K2  |  | F2              |
|         | 035       | 03E | 03F |  | 0CB             |
|         | D4        | D5  | D6  |  | H4              |
|         | 028       | 029 | 02A |  | (not available) |
| Line    | D7        | D8  | D9  |  | Z3              |
|         | 02B       | 02C | 02D |  | 0CD             |
|         | D10       | D11 | D12 |  | Z4              |
|         | 02E       | 02F | 030 |  | 0CE             |
|         | Z1        | Z2  | E2  |  | Z5              |
|         | 03A       | 03B | 039 |  | 0CF             |
|         | Transport |     |     |  | Path            |

† These bytes are optionally regenerated by the TNETS3001.

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## SONET STS-1 OVERHEAD TERMINATOR

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### PRINCIPLES OF OPERATION

#### receive line- and terminal-overhead byte RAM locations

| SYMBOL         | ADDRESS (hex)        |                   | CONTROL BIT†           | DESCRIPTION  |
|----------------|----------------------|-------------------|------------------------|--|
|                | INCOMING             | INSERT‡           |                        |  |
| A1             | 016                  | 036               | RRFRM                  | Framing pattern. The A1 and A2 bytes are automatically regenerated and are stored in insert locations.   |
| A2             | 017                  | 037               |                        |  |
| C1             | 01C<br>05C           | 03C               | RRC1                   | STS-1 signal identifier. The incoming C1 byte is debounced and stored in location 05C.   |
| B1             | 014                  | 034<br>049        | RRB1                   | Section BIP-8 parity. The received B1 byte carries B1 BIP-8 parity in the STS-1 mode and B1 BIP-8 parity-error indications in the STS-N mode. The parity errors are added to the receive B1 counter. The B1 BIP-8 parity for the outgoing terminal data is recalculated and stored in the insert location. |
| E1             | 018                  | 038               | RRE1<br>RE2A‡<br>RA2E‡ | Section-orderwire byte. The incoming E1 byte is also available in the orderwire/APS interface. The E1 byte can be reused for AIS communication between multiple TNETS3001s.  |
| F1             | 01D<br>05D           | 03D               | RRF1                   | Section-user byte. The F1 byte is debounced and stored in location 05D.  |
| D1<br>D2<br>D3 | 005<br>006<br>007    | 025<br>026<br>027 | RRSD                   | Section data-communication channel. The incoming D1, D2, and D3 bytes are available as a single 192-kbit/s serial HDLC channel on the section-datacom interface.   |
| H1<br>H2<br>H3 | 011<br>012<br>013    | 031<br>032<br>033 | RRPTR                  | Payload-pointer and pointer-action bytes. The insert H1, H2, and H3 bytes are inserted into the outgoing terminal data without changing the J1-byte position.  |
| B2             | 015                  | 035<br>051        | RRB2                   | Line BIP-8 bit parity. The received B2 byte carries the B2 BIP-8 parity. The parity errors are added to the B2 counter. The recalculated B2 byte is stored in the insert address.  |
| K1<br>K2       | 01E, 05E<br>01F, 05F | 03E<br>03F        | RRAPS                  | Automatic-protection-switching bytes. The K1 and K2 bytes are debounced and stored in locations 05E and 05F, respectively. The APS bytes are also available in the orderwire/APS interface.  |
| D4–D12         | 008–010              | 028–030           | RRLD                   | Line data-communication channel. The incoming D4 through D12 bytes are available as a single 576-kbit/s serial HDLC channel on the line-datacom interface.   |
| E2             | 019                  | 039               | RRE2                   | Line-orderwire byte. The incoming E2 byte is also available in the orderwire/APS interface.  |
| Z1<br>Z2       | 01A, 05A<br>01B, 05B | 03A<br>03B        | RRZ1<br>RRZ2           | Growth bytes. The Z1 and Z2 bytes are debounced and stored in locations 05A and 05B, respectively.   |

† The insert bytes are multiplexed into the terminal data when the corresponding control bit is set. Otherwise, the incoming bytes are multiplexed into the terminal data. If used, the microprocessor should initialize the insert locations. This feature is available in pass-through mode only. In receive-retiming or SPE-only modes, the terminal data has these bytes as an all-zeros pattern.

‡ The E1 byte can be used for AIS transmission. All ones in the E1 byte indicates an AIS condition; all zeros indicates a non-AIS condition. If the control bit RE2A is set, the TNETS3001 interprets the incoming E1 byte for AIS information. When the control bit RA2E is set, the terminal E1 byte carries AIS information.

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# TNETS3001 SONET STS-1 OVERHEAD TERMINATOR

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## PRINCIPLES OF OPERATION

### receive path-overhead byte RAM locations

| SYMBOL         | ADDRESS (hex)                    |                   | CONTROL BIT† | DESCRIPTION   |
|----------------|----------------------------------|-------------------|--------------|---|
|                | INCOMING                         | INSERT†           |              |   |
| J1             | 080–0BF                          | 080–0BF           |              | Path trace. The incoming message is stored in the RAM locations in a rotating fashion. There is no specified starting point, but any incoming J1 byte is written into the next sequential RAM location. The J1 byte always passes through the TNETS3001 without modification. |
| B3             | 0C0                              | 0C8               | RPATH        | Path BIP-8 parity. The received B3 byte carries the B3 BIP8 parity. The parity errors are added to the B3 counter. The recalculated B3 byte is stored in the insert address.  |
| C2             | 0C1, 0D1                         | 0C9               | RPATH        | Path-signal label. The C2 byte is debounced and stored in location 0D1.   |
| G1             | 0C2                              | 0CA               | RPATH        | Path status. The upper nibble of the G1 byte contains the FEBE count (up to eight per frame) and is added to the receive FEBE counter.  |
| F2             | 0C3, 0D3                         | 0CB               | RPATH        | Path-user channel. This byte provides user information between path-terminating network elements. The F2 byte is debounced and stored in location 0D3.  |
| H4             | 0C4                              | 0CC               |              | Multiframe indicator. The H4 byte always passes through the TNETS3001 without modification.   |
| Z3<br>Z4<br>Z5 | 0C5, 0D5<br>0C6, 0D6<br>0C7, 0D7 | 0CD<br>0CE<br>0CF | RPATH        | Path growth. The Z3, Z4, and Z5 bytes are debounced and stored in locations 0D5, 0D6, and 0D7, respectively.  |

† The insert bytes are multiplexed into the terminal data stream when the corresponding control bit is set. Otherwise, the incoming bytes are multiplexed into the terminal data.

### receive performance-monitor locations‡

| SYMBOL | ADDRESS (hex) | BITS | DISABLE CONDITIONS             | DESCRIPTION   |
|--------|---------------|------|--------------------------------|---|
| B1     | 046           | 7–0  | RLOS, RLOF                     | STS-1 mode. Counts B1 BIP-8 parity errors. STS-N mode Counts ones in the B1 byte. |
| B2     | 047           | 7–0  | RLOS, RLOF, RLAI5              | Counts incoming B2 BIP-8 parity errors  |
| INC    | 045           | 7–4  | RLOS, RLOF, RLAI5, RLOP, RPAIS | Counts incoming pointer increments  |
| DEC    | 045           | 3–0  |                                | Counts incoming pointer decrements  |
| B3     | 0D4           | 7–0  |                                | Counts incoming B3 BIP-8 parity errors  |
| FEBE   | 0D2           | 7–0  |                                | Counts incoming FEBE nibbles  |

‡ All performance monitors saturate at the maximum value and reset to zero on read.

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## SONET STS-1 OVERHEAD TERMINATOR

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### transmit insert-overhead byte locations (in hex)

|           |                       |                       |                      |      |                       |
|-----------|-----------------------|-----------------------|----------------------|------|-----------------------|
| Section   | A1†<br>136            | A2†<br>137            | C1<br>13C            |      | J1<br>180-1BF         |
|           | B1‡<br>134            | E1§<br>138            | F1<br>13D            |      | B3<br>1C8             |
| Line      | D1 Serial I/O<br>125  | D2 Serial I/O<br>126  | D3 Serial I/O<br>127 |      | C2<br>1C9             |
|           | H1<br>(not available) | H2<br>(not available) | H3<br>133            |      | G1<br>1CA             |
|           | B2‡<br>135            | K1§¶<br>13E           | K2 §¶<br>13F         |      | F2<br>1CB             |
|           | D4§<br>128            | D5§<br>129            | D6§<br>12A           |      | H4<br>(not available) |
|           | D7 Serial I/O<br>12B  | D8 Serial I/O<br>12C  | D9§<br>12D           |      | Z3<br>1CD             |
|           | D10§<br>12E           | D11§<br>12F           | D12§<br>130          |      | Z4<br>1CE             |
|           | Z1<br>13A             | Z2<br>13B             | E2§<br>139           |      | Z5<br>1CF             |
|           |                       |                       |                      |      |                       |
| Transport |                       |                       |                      | Path |                       |

† These bytes are optionally regenerated by the TNETS3001.

‡ These bytes are recalculated by the TNETS3001. They are XORED with respective error mask before transmission.

§ These bytes are inserted from the orderwire, APS, and datacom interfaces.

¶ The APS bytes are inserted from the APS or the microprocessor interface.

### transmit terminal-overhead byte RAM locations (in hex)

|           |            |            |            |      |               |
|-----------|------------|------------|------------|------|---------------|
| Section   | A1<br>116  | A2<br>117  | C1<br>11C  |      | J1<br>180-1BF |
|           | B1<br>114  | E1<br>118  | F1<br>11D  |      | B3<br>1C0     |
| Line      | D1<br>105  | D2<br>106  | D3<br>107  |      | C2<br>1C1     |
|           | H1<br>111  | H2<br>112  | H3<br>113  |      | G1<br>1C2     |
|           | B2<br>115  | K1<br>11E  | K2<br>11F  |      | F2<br>1C3     |
|           | D4<br>108  | D5<br>109  | D6<br>10A  |      | H4<br>1C4     |
|           | D7<br>10B  | D8<br>10C  | D9<br>10D  |      | Z3<br>1C5     |
|           | D10<br>10E | D11<br>10F | D12<br>110 |      | Z4<br>1C6     |
|           | Z1<br>11A  | Z2<br>11B  | E2<br>119  |      | Z5<br>1C7     |
|           |            |            |            |      |               |
| Transport |            |            |            | Path |               |

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# TNETS3001 SONET STS-1 OVERHEAD TERMINATOR

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## PRINCIPLES OF OPERATION

### transmit terminal- and line-overhead byte RAM locations

| SYMBOL         | ADDRESS (hex)     |                   | CONTROL BIT†           | DESCRIPTION   |
|----------------|-------------------|-------------------|------------------------|---|
|                | INCOMING          | INSERT‡           |                        |   |
| A1             | 116               | 136               |                        | Framing pattern. The outgoing A1 and A2 bytes are stored in insert locations and automatically inserted into the outgoing line data. The A1 and A2 bytes are regenerated every frame when the control bit TRFRM = 1.  |
| A2             | 117               | 137               |                        |   |
| C1             | 11C               | 13C               | TRC1                   | STS-1 signal identifier. Normal operation.  |
| B1             | 114               | 134<br>149        | TRERR¶                 | Section BIP-8 parity/error mask. B1 errors are added to the transmit B1 counter. The outgoing B1 BIP-8 parity is recalculated and stored in insert location 134. In the STS-1 mode, the recalculated B1 is XORed with the B1 error mask from location 149 before transmission. In the STS-N mode, the B1 error mask from location 149 is transmitted. |
| E1             | 118               | 138               | TRE1<br>TE2A§<br>TA2E§ | Section-orderwire byte. The E2 byte from the orderwire interface is stored in the insert location. The E1 byte is optionally reused for AIS communication between TNETS3001s.   |
| F1             | 11D               | 13D               | TRF1                   | Section-user byte. Normal operation.  |
| D1<br>D2<br>D3 | 105<br>106<br>107 | 125<br>126<br>127 | TRSD                   | Section data-communication channel. The section-datacom bytes, D1 – D3, from the section-datacom interface are stored in the insert location.   |
| H1<br>H2<br>H3 | 111<br>112<br>113 | 133               |                        | Payload-pointer and pointer-action bytes. The TNETS3001 automatically recalculates the outgoing pointer. The H3 byte is inserted from RAM location 133.   |
| B2             | 115               | 135<br>151        | TRERR¶                 | Line BIP-8 bit parity. The B2 errors are added to the transmit B2 counter. The outgoing B2 BIP-8 parity is recalculated and stored in the insert location 135. The recalculated B2 is XORed with the B2 error mask from location 151 before transmission.   |
| K1<br>K2       | 11E<br>11F        | 13E<br>13F        | TRAPS<br>EXAPS         | Automatic-protection-switching bytes. If EXAPS is set, the APS bytes from the orderwire interface are stored in the insert RAM locations.   |
| D4–D12         | 108–110           | 128–130           | TRLD                   | Line data-communication channel. The line-datacom bytes, D4–D12, from the section-datacom interface are stored in the insert location.  |
| E2             | 119               | 139               | TRE2                   | Line-orderwire byte. The E2 byte from the orderwire interface is stored in the insert location.   |
| Z1<br>Z2       | 11A<br>11B        | 13A<br>13B        | TRZ1<br>TRZ2           | Growth bytes. Normal operation.   |

† The insert bytes are multiplexed into the line data when the corresponding control bit is set. If used, the microprocessor initializes the insert locations.

‡ In SPE-only modes, the incoming terminal data has these bytes as an all-zeros pattern.

§ The E1 byte can be used for AIS transmission. All ones in the E1 byte indicates an AIS condition; all zeros indicates a non-AIS condition. If the control bit TE2A is set, the TNETS3001 interprets the incoming E1 byte for AIS information. When the control bit TA2E is set, the line E1 byte carries AIS information.

¶ If TRERR is set, the error masks are reset after transmission; otherwise, error is transmitted continuously.

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# TNETS3001 SONET STS-1 OVERHEAD TERMINATOR

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## PRINCIPLES OF OPERATION

### transmit path-overhead byte RAM locations

| SYMBOL         | ADDRESS (hex)     |                   | CONTROL BIT†    | DESCRIPTION  |
|----------------|-------------------|-------------------|-----------------|--|
|                | INCOMING          | INSERT†           |                 |  |
| J1             | 180-1BF           | 180-1BF           | TPATH           | Path trace. The incoming/outgoing message is stored into/extracted from the RAM locations in a rotating fashion. There is no specified starting point, but any incoming J1 byte is written to/read from the next sequential RAM location.  |
| B3             | 1C0               | 1C8               | TPATH<br>TRERR‡ | Path BIP-8 parity. The parity errors are added to the B3 counter. The recalculated B3 byte is stored in the insert address. The recalculated B3 is XORed with the B3 error mask from location 1D0 before transmission.   |
| C2             | 1C1               | 1C9               | TPATH           | Path-signal label. Normal operation.   |
| G1             | 1C2               | 1CA               | TPATH           | Path status. If TPATH is set, the TNETS3001 sends a FEBE indication in the upper nibble of the outgoing G1 byte automatically. A path-yellow indication can be sent by setting bit 3 to one. The path-yellow indication should be sent 2-3 seconds after the following receive alarms are active: RLOS, RLOF, RLAI, RLOP and RPAIS; and it should be removed 10–20 seconds after the receive alarms are cleared. |
| F2             | 1C3               | 1CB               | TPATH           | Path-user channel. Normal operation.   |
| H4             | 1C4               | 1CC               |                 | Multiframe indicator. The H4 byte always passes through the TNETS3001 without modification.  |
| Z3<br>Z4<br>Z5 | 1C5<br>1C6<br>1C7 | 1CD<br>1CE<br>1CF | TPATH           | Path growth. Normal operation.   |

† The insert bytes are multiplexed into the line data stream when the corresponding control bit is set. Otherwise, the incoming bytes are multiplexed into the line data stream.

‡ If TRERR is set, the error masks are reset after transmission; otherwise, error is transmitted continuously.

### transmit performance-monitor locations§

| SYMBOL | ADDRESS (hex) | BITS | DISABLE CONDITIONS                | DESCRIPTION                            |
|--------|---------------|------|-----------------------------------|--|
| B1     | 146           | 7–0  | TLOS, TLOF                        | Counts B1 BIP-8 parity errors          |
| B2     | 147           | 7–0  | TLOS, TLOF, TLAIS                 | Counts incoming B2 BIP-8 parity errors |
| INC    | 145           | 7–4  | TLOS, TLOF, TLAIS,<br>TLOP, TPAIS | Counts incoming pointer increments     |
| DEC    | 145           | 3–0  |                                   | Counts incoming pointer decrements     |
| B3     | 1D4           | 7–0  |                                   | Counts incoming B3 BIP-8 parity errors |

† The insert bytes are multiplexed into the line data stream when the corresponding control bit is set. Otherwise, the incoming bytes are multiplexed into the line data stream.

§ All performance monitors saturate at the maximum value and reset to zero on read.

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## PRINCIPLES OF OPERATION

receive transport-overhead RAM contents summary†

| ADDRESS | _0      | _1      | _2       | _3       | _4       | _5          | _6         | _7         | _8     | _9      | _A       | _B       | _C       | _D       | _E       | _F       |
|---------|---------|---------|----------|----------|----------|-------------|------------|------------|--------|---------|----------|----------|----------|----------|----------|----------|
| 00_     | Spare   | Spare   | Spare    | Spare    | Spare    | In D1       | In D2      | In D3      | In D4  | In D5   | In D6    | In D7    | In D8    | In D9    | In D10   | In D11   |
| 01_     | In D12  | In H1   | In H2    | In H3    | In B1    | In B2       | In A1      | In A2      | In D4  | In E2   | In Z1    | In Z2    | In C1    | In F1    | In K1    | In K2    |
| 02_     | Spare   | Spare   | Spare    | Spare    | Spare    | Out D1      | Out D2     | Out D3     | Out D4 | Out D5  | Out D6   | Out D7   | Out D8   | Out D9   | Out D10  | Out D11  |
| 03_     | Out D12 | Spare   | Spare    | Spare    | Out B1   | Out B2      | Out A1     | Out A2     | Out E1 | Out E2  | Out Z1   | Out Z2   | Out C1   | Out F1   | Out K1   | Out K2   |
| 04_     | Spare   | Spare   | Spare    | Spare    | Spare    | PJC counter | B1 counter | B2 counter | Spare  | B1 mask | F[-1] Z1 | F[-1] Z2 | F[-1] C1 | F[-1] F1 | F[-1] K1 | F[-1] K2 |
| 05_     | Spare   | B2 mask | F[-2] Z1 | F[-2] Z2 | F[-2] C1 | F[-2] F1    | F[-2] K1   | F[-2] K2   | Spare  | Spare   | Deb Z1   | Deb Z2   | Deb C1   | Deb F1   | Deb K1   | Deb K2   |

receive path-overhead RAM contents summary†

| ADDRESS | _0           | _1           | _2           | _3           | _4           | _5           | _6           | _7           | _8           | _9           | _A           | _B           | _C           | _D           | _E           | _F           |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 08_     | F[-8] In J1  | F[-7] In J1  | F[-6] In J1  | F[-5] In J1  | F[-4] In J1  | F[-3] In J1  | F[-2] In J1  | F[-1] In J1  | In J1        | F[-63] In J1 | F[-62] In J1 | F[-61] In J1 | F[-60] In J1 | F[-59] In J1 | F[-58] In J1 | F[-57] In J1 |
| 09_     | F[-56] In J1 | F[-55] In J1 | F[-54] In J1 | F[-53] In J1 | F[-52] In J1 | F[-51] In J1 | F[-50] In J1 | F[-49] In J1 | F[-48] In J1 | F[-47] In J1 | F[-46] In J1 | F[-45] In J1 | F[-44] In J1 | F[-43] In J1 | F[-42] In J1 | F[-41] In J1 |
| 0A_     | F[-40] In J1 | F[-39] In J1 | F[-38] In J1 | F[-37] In J1 | F[-36] In J1 | F[-35] In J1 | F[-34] In J1 | F[-33] In J1 | F[-32] In J1 | F[-31] In J1 | F[-30] In J1 | F[-29] In J1 | F[-28] In J1 | F[-27] In J1 | F[-26] In J1 | F[-25] In J1 |
| 0B_     | F[-24] In J1 | F[-23] In J1 | F[-22] In J1 | F[-21] In J1 | F[-20] In J1 | F[-19] In J1 | F[-18] In J1 | F[-17] In J1 | F[-16] In J1 | F[-15] In J1 | F[-14] In J1 | F[-13] In J1 | F[-12] In J1 | F[-11] In J1 | F[-10] In J1 | F[-9] In J1  |
| 0C_     | In B3        | In C2        | In G1        | In F2        | In H4        | In Z3        | In Z4        | In Z5        | Out B3       | Out C2       | Out G1       | Out F2       | Spare        | Out Z3       | Out Z4       | Out Z5       |
| 0D_     | B3 mask      | Deb C2       | FEBE counter | Deb F2       | B3 counter   | Deb Z3       | Deb Z4       | Deb Z5       | Spare        | F[-1] C2     | Spare        | F[-1] F2     | Spare        | F[-1] Z3     | F[-1] Z4     | F[-1] Z5     |
| 0E_     | Spare        | F[-2] C2     | Spare        | F[-2] F2     | Spare        | F[-2] Z3     | F[-2] Z4     | F[-2] Z5     |              |              |              |              |              |              |              |              |

† In: Incoming-overhead byte

Out: Insert-overhead byte

F[-n]: Overhead byte from previous nth frame

Deb: Debounced-overhead byte

## TNETS3001 SONET STS-1 OVERHEAD TERMINATOR

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### PRINCIPLES OF OPERATION

transmit transport-overhead RAM contents summary†

| ADDRESS | _0           | _1      | _2    | _3    | _4     | _5          | _6         | _7         | _8         | _9        | _A      | _B      | _C      | _D      | _E       | _F           |
|---------|--------------|---------|-------|-------|--------|-------------|------------|------------|------------|-----------|---------|---------|---------|---------|----------|--------------|
| 10_     | Spare        | Spare   | Spare | Spare | Spare  | In D1       | In D2      | In D3      | In D4      | In D5     | In D6   | In D7   | In D8   | In D9   | In D10   | In D11       |
| 11_     | In D12       | In H1   | In H2 | In H3 | In B1  | In B2       | In A1      | In A2      | In E1      | In E2     | In Z1   | In Z2   | In C1   | In F1   | In K1    | In K2        |
| 12_     | Spare        | Spare   | Spare | Spare | Spare  | SDCC D1     | SDCC D2    | SDCC D3    | LDCC D4    | LDCC D5   | LDCC D6 | LDCC D7 | LDCC D8 | LDCC D9 | LDCC D10 | LDCC D11     |
| 13_     | LDCC D12     | Spare   | Spare | Spare | Out B1 | Out B2      | Out A1     | Out A2     | Order W E1 | OrderW E2 | Out Z1  | Out Z2  | Out C1  | Out F1  | APS K1   | APS K2       |
| 14_     | Spare        | Spare   | Spare | Spare | Spare  | PJC counter | B1 counter | B2 counter | Spare      | B1 mask   | Spare   | Spare   | Spare   | Spare   | Spare    | Internal use |
| 15_     | Internal use | B2 mask | Spare | Spare | Spare  | Spare       | Spare      | Spare      | Spare      | Spare     | Spare   | Spare   | Spare   | Spare   | Spare    | Spare        |

transmit path-overhead RAM contents summary†

| ADDRESS | _0            | _1            | _2            | _3            | _4            | _5            | _6            | _7            | _8            | _9            | _A            | _B            | _C            | _D            | _E            | _F            |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| 18_     | F[-8] Out J1  | F[-7] Out J1  | F[-6] Out J1  | F[-5] Out J1  | F[-4] Out J1  | F[-3] Out J1  | F[-2] Out J1  | F[-1] Out J1  | Out J1        | F[-63] Out J1 | F[-62] Out J1 | F[-61] Out J1 | F[-60] Out J1 | F[-59] Out J1 | F[-58] Out J1 | F[-57] Out J1 |
| 19_     | F[-56] Out J1 | F[-55] Out J1 | F[-54] Out J1 | F[-53] Out J1 | F[-52] Out J1 | F[-51] Out J1 | F[-50] Out J1 | F[-49] Out J1 | F[-48] Out J1 | F[-47] Out J1 | F[-46] Out J1 | F[-45] Out J1 | F[-44] Out J1 | F[-43] Out J1 | F[-42] Out J1 | F[-41] Out J1 |
| 1A_     | F[-40] Out J1 | F[-39] Out J1 | F[-38] Out J1 | F[-37] Out J1 | F[-36] Out J1 | F[-35] Out J1 | F[-34] Out J1 | F[-33] Out J1 | F[-32] Out J1 | F[-31] Out J1 | F[-30] Out J1 | F[-29] Out J1 | F[-28] Out J1 | F[-27] Out J1 | F[-26] Out J1 | F[-25] Out J1 |
| 1B_     | F[-24] Out J1 | F[-23] Out J1 | F[-22] Out J1 | F[-21] Out J1 | F[-20] Out J1 | F[-19] Out J1 | F[-18] Out J1 | F[-17] Out J1 | F[-16] Out J1 | F[-15] Out J1 | F[-14] Out J1 | F[-13] Out J1 | F[-12] Out J1 | F[-11] Out J1 | F[-10] Out J1 | F[-9] Out J1  |
| 1C_     | In B3         | In C2         | In G1         | In F2         | In H4         | In Z3         | In Z4         | In Z5         | Out B3        | Out C2        | Out G1        | Out F2        | Spare         | Out Z3        | Out Z4        | Out Z5        |
| 1D_     | B3 mask       | Spare         | Spare         | Spare         | B3 counter    | Spare         | Spare         | Spare         | Spare         | Spare         | Spare         | Spare         | Spare         | Spare         | Spare         | Spare         |

† In: Incoming-overhead byte

Out: Insert-overhead byte

F[-n]: Overhead byte from previous nth frame

Deb: Debounced-overhead byte

# TNETS3001 SONET STS-1 OVERHEAD TERMINATOR

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## PRINCIPLES OF OPERATION

### interfaces and operating modes

The control bits used for various modes are summarized below in the following table:

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0FA     | STS-1 | PARA  |       |       | ALTOW |       |       |       |
| 1F9     |       |       |       |       |       |       | RXRTM |       |
| 1FA     | SPE   | TCLK  | RCLK  |       |       |       |       |       |

### line-side interface

In the receive direction, the line-side interface consists of the incoming 51.84-MHz clock (RLCI), the incoming STS-1 data (RLDI), and the optional frame pulse ( $\overline{\text{RFRI}}$ ). When used,  $\overline{\text{RFRI}}$  allows exit from the OOF state within 125  $\mu\text{s}$ . The transmit-line interface consists of the reference 51.84-MHz clock (TLCI), the optional frame reference ( $\overline{\text{TFRI}}$ ), the outgoing clock (TLCO), and the outgoing STS-1 data (TLDO). The line-side interface supports either the STS-1 mode or the STS-N mode as summarized in the following table:

| MODE  | SELECTION | DESCRIPTION   |
|-------|-----------|---|
| STS-1 | STS-1 = 1 | Both incoming and outgoing line data are scrambled. The chip descrambles RLDI and scrambles TLDO.   |
|       |           | The receive B1 byte contains B1 BIP-8 parity. The chip compares the incoming B1 byte to calculated B1 and adds the parity errors to the receive B1 counter.   |
|       |           | The transmit B1 byte is the outgoing B1 BIP-8 parity. The chip calculates the outgoing B1 parity, exclusive-ORs the result with the outgoing B1 error mask from RAM location 149, and transmits the result on the line. |
| STS-N | STS-1 = 0 | Both incoming and outgoing line data are not scrambled.   |
|       |           | The receive B1 byte contains B1 BIP-8 parity-error indications. The chip adds the ones in the incoming B1 byte to the receive B1 counter.   |
|       |           | The transmit B1 byte contains the B1 error mask from RAM location 149.  |

The clock selection bit (TCLK) allows TLCO to be derived from the following sources:

| TCLK | SPE | PARA | SOURCE OF TLCO   |
|------|-----|------|--|
| 0    | 0   | 0    | TTCl. $\overline{\text{TFRI}}$ cannot be used in this mode.  |
| 0    | 0   | 1    | TPC1. $\overline{\text{TFRI}}$ cannot be used in this mode.  |
| 1    | 0   | 0    | TLCl. $\overline{\text{TFRI}}$ can be used in this mode.   |
| 1    | 0   | 1    | TPC1. $\overline{\text{TFRI}}$ can be used in this mode.   |
| 0,1  | 1   | 0    | TLCl. $\overline{\text{TFRI}}$ can be used in this mode, (SPE only <sup>†</sup> ) and serial only. |

<sup>†</sup> The SPE-only mode can be used only if the control bit RXRTM = 0

### terminal-side interface

The receive-direction terminal-side interface consists of the 51.84-MHz serial clock (RTCO), the serial data (RTDO), the payload indicator (RSPE), the C1J1 indicator (RSYN), the 6.48-MHz parallel clock (TPCO), and the parallel data (TPDO7–TPDO0). The transmit terminal-side interface consists of the 51.84-MHz serial clock (TTCl), the serial data (TTDI), the payload indicator (TSPE), the C1J1 or J1 indicator (TSYN), the 6.48-MHz parallel clock (TPC1), and the parallel data (TPDI7–TPDI0).

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### PRINCIPLES OF OPERATION

#### terminal-side interface (continued)

The terminal-side interface supports the following modes:

| MODE                       | SELECTION                                       | DESCRIPTION  |
|----------------------------|---|--|
| Serial STS1 pass through   | PARA = 0<br>RXRTM = 1<br>SPE = 0<br>RCLK = 0, 1 | RTDO is serial nonretimed STS-1 data with all TOH bytes from the line input or RAM.  |
|                            |   | TPDO7 – TPDO0 is parallel STS-1 data with all TOH bytes from the line input or RAM.  |
|                            |   | RSPE is nominally: low width = 24, high width = 696; increment: low width = 32, high width = 688; decrement: low width = 16, high width = 704.         |
|                            |   | RSYN is high during the C1 and J1 bytes. Numbers are clock periods.  |
|                            |   | TTCI and TTDI are used as terminal STS-1 inputs in the transmit direction.   |
|                            |   | TPCI and TPDI 7 – TPDI0 are ignored.   |
|                            |   | TSPE and TSYN are ignored.   |
|                            |   | All TOH bytes can be inserted to/extracted from the terminal.  |
|                            |   | The E1 byte can be used for AIS communication.   |
|                            |   | Transmit-side alarms and performance monitors are enabled.   |
|                            |   | RTCO and TPCO are derived from RLCI.   |
| Parallel STS1 pass through | PARA = 1<br>RXRTM = 1<br>SPE = 0<br>RCLK = 0, 1 | RTDO is serial nonretimed STS-1 data with all TOH bytes from the line input or RAM.  |
|                            |   | TPDO7 – TPDO0 is parallel STS-1 data with all TOH bytes from the line input or RAM.  |
|                            |   | RSPE is nominally: low width = 3, high width = 87; increment: low width = 4, high width = 86; decrement: low width = 2, high width = 88.               |
|                            |   | RSYN is high during the C1 and J1 bytes. Numbers are clock periods.  |
|                            |   | TTCI and TTDI are ignored.   |
|                            |   | TPCI and TPDI 7 – TPDI0 are used as terminal STS-1 inputs in the transmit direction.   |
|                            |   | TSPE and TSYN are ignored.   |
|                            |   | All TOH bytes can be inserted to/extracted from the terminal.  |
|                            |   | The E1 byte can be used for AIS communication.   |
|                            |   | Transmit-side alarms and performance monitors are enabled.   |
|                            |   | RTCO and TPCO are derived from RLCI.   |
| Serial SPE only            | PARA = 0<br>RXRTM = 0<br>SPE = 1                | RTDO is serial retimed SPE-only data with only the A1, A2, E1, H1, and H2 bytes inserted into the terminal data.                                       |
|                            |   | TPDO7 – TPDO0 consists of all zeros data.  |
|                            |   | RSPE is nominally: low width = 1, high width = 29; increment: low width = 1, high width = 45; decrement: low width = 1, high width = alternate 22, 23. |
|                            |   | RSYN is high during the J1 byte. Numbers are clock periods.  |
|                            |   | TTCI, TTDI, TSPE, and TSYN are used as the terminal SPE-only inputs.   |
|                            |   | TPCI and TPDI 7 – TPDI0 are ignored.   |
|                            |   | TSPE and TSYN are used.  |
|                            |   | No TOH byte can be inserted to/extracted from the terminal.  |
|                            |   | The terminal E1 byte can be used for AIS communication only.   |
|                            |   | Transmit-side alarms and performance monitors are disabled.  |
|                            | RCLK = 0  | RTCO and TPCO are derived from RLCI.   |
|                            | RCLK = 1  | RTCO and TPCO are derived from TLCI.   |

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## PRINCIPLES OF OPERATION

### microprocessor interface

The microprocessor interface consists of multiplexed address/data bus (AD7–AD0), address bit (A8), address latch enable (ALE), chip select ( $\overline{SEL}$ ), read enable ( $\overline{RD}$ ), write enable ( $\overline{WR}$ ), and interrupt (INT) signals. In addition, the TNETS3001 provides both software- and hardware-interrupt capability based on the status of the receive and transmit transport- and path-overhead alarms.

### orderwire/APS interface

In the receive direction, the section-orderwire byte (E1), the line-orderwire byte (E2) and the APS bytes (K1 and K2) are multiplexed to form a 576-kbit/s bit-serial stream. This interface consists of the multiplexed 576-kbit/s data signal (ORDO), a clock signal (ORCO), and three framing pulses: a section-framing pulse (SRFR), a line-framing pulse (LRFR) and an APS-framing pulse ( $\overline{RAP}$ ).

The transmit-side orderwire/APS interface is similar. The section-orderwire byte (E1), the line-orderwire byte (E2) and the APS bytes (K1 and K2) are demultiplexed from a 576-kbit/s bit-serial stream. This interface consists of the multiplexed 576-kbit/s data signal (OTDI), a clock signal (OTCO), and three framing pulses: a section-orderwire-framing pulse (STFR), a line-orderwire-framing pulse (LTFR), and an APS-framing pulse ( $\overline{TAP}$ ).

The orderwire interface supports two modes:

| MODE                          | SELECTION | DESCRIPTION   |
|-------------------------------|-----------|---|
| Normal-orderwire interface    | ALTOW = 0 | SRFR occurs one ORCO clock cycle before MSB of E1 byte in ORDO.             |
|                               |           | LRFR occurs one ORCO clock cycle before MSB of E2 byte in ORDO.             |
|                               |           | STFR occurs one ORCI clock cycle before MSB of E1 byte is expected in OTDI. |
|                               |           | LTFR occurs one ORCI clock cycle before MSB of E2 byte is expected in OTDI. |
| Alternate-orderwire interface | ALTOW = 1 | SRFR occurs coincident with the MSB of E1 byte in ORDO.                     |
|                               |           | LRFR occurs coincident with the MSB of E2 byte in ORDO.                     |
|                               |           | STFR occurs coincident with the MSB of E1 byte is expected in OTDI.         |
|                               |           | LTFR occurs coincident with the MSB of E2 byte is expected in OTDI.         |

### datacom interfaces

In the receive direction, the section-overhead data-communication channel interface consists of a receive data-out signal (SRDO) and a clock-out signal (SRCO). The line-overhead data-communication interface consists of a receive data-out signal (LRDO) and a clock-out signal (LRCO).

In the transmit direction, the section-overhead data-communication channel interface consists of a data-in signal (STDI) and a clock-out signal (STCO). The line-overhead data-communication channel interface consists of a data-in signal (LTDI) and a clock-out signal (LTCO).

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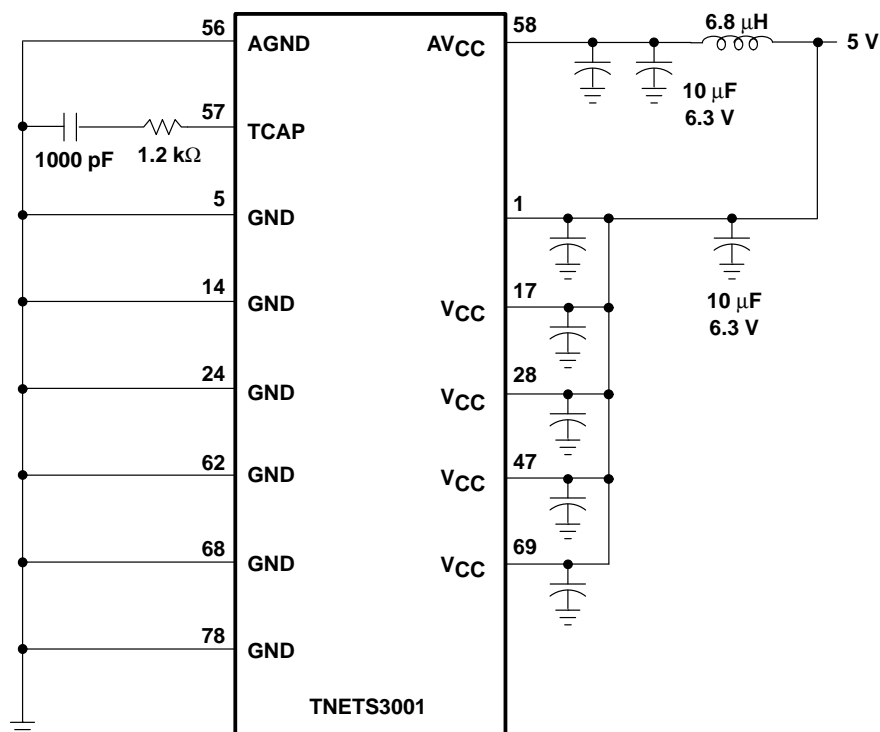
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## PRINCIPLES OF OPERATION

### power and ground interfaces with recommended external components

Figure 19 shows the recommended power and ground connections for the TNETS3001 device. Separate planes should be employed for  $V_{CC}$  and GND. Bypass networks consist of 10- $\mu$ F capacitors in parallel with 0.1- $\mu$ F capacitors as shown. These 0.1- $\mu$ F capacitors should be RF quality and closely connected to each of the device voltage leads to decouple them to ground. A Fair-Rite Products #2743002111 or equivalent ferrite bead is recommended in the  $AV_{CC}$  supply-voltage path.



NOTE A: All capacitors are 0.1  $\mu$ F unless otherwise specified.

Figure 19. TNETS3001 Power-Supply Connections

### throughput delays

The TNETS3001 throughput delays below are listed in terms of STS-1 bit times (1 bit = 19.29 ns nominal):

- The throughput delay from the terminal-side input to the line-side transmit output is from 65 to 113 bits.
- The throughput delay from the line-side receive input to the terminal-side output is from 65 to 133 bits in the receive-retiming mode or is a fixed 25 bits when not in the receive-retiming mode (see bit 1 of register 1F9H).

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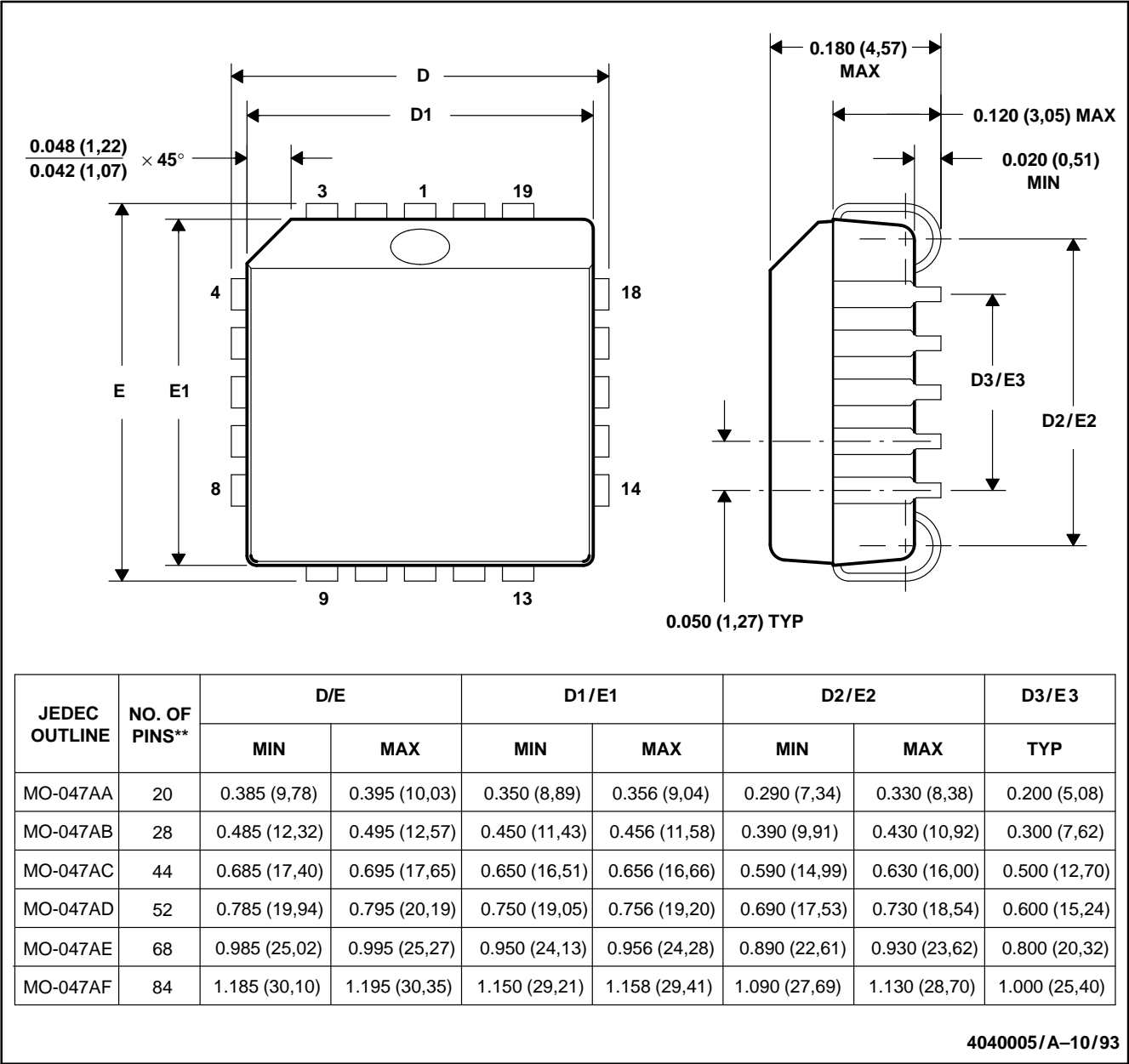
TNETS3001  
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MECHANICAL DATA

FN/S-PQCC-J\*\*  
20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER



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- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Dimensions D1 and E1 do not include mold flash or protrusion. Protrusion shall not exceed 0.010 (0,25) on any side.  
D. Falls within JEDEC MO-047  
E. Maximum deviation from coplanarity is 0.004 (0,10).





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