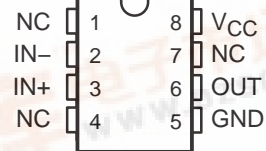


TL714C HIGH-SPEED DIFFERENTIAL COMPARATOR

SLCS015A – DECEMBER 1988 – REVISED AUGUST 2003

- Operates From a 5-V Supply
- Self-Biasing Inputs
- Hysteresis . . . 10 mV Typ
- Response Time . . . 6 ns Typ
- Maximum Operating Frequency . . . 50 MHz Typ

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics.

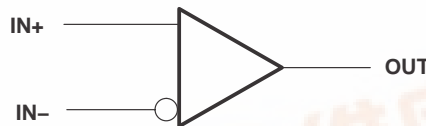
The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

ORDERING INFORMATION

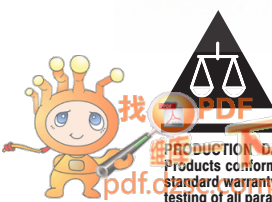
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL714CP	TL714CP
	SOIC (D)	Tube of 75	TL714CD	TL714C
		Reel of 2500	TL714CDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

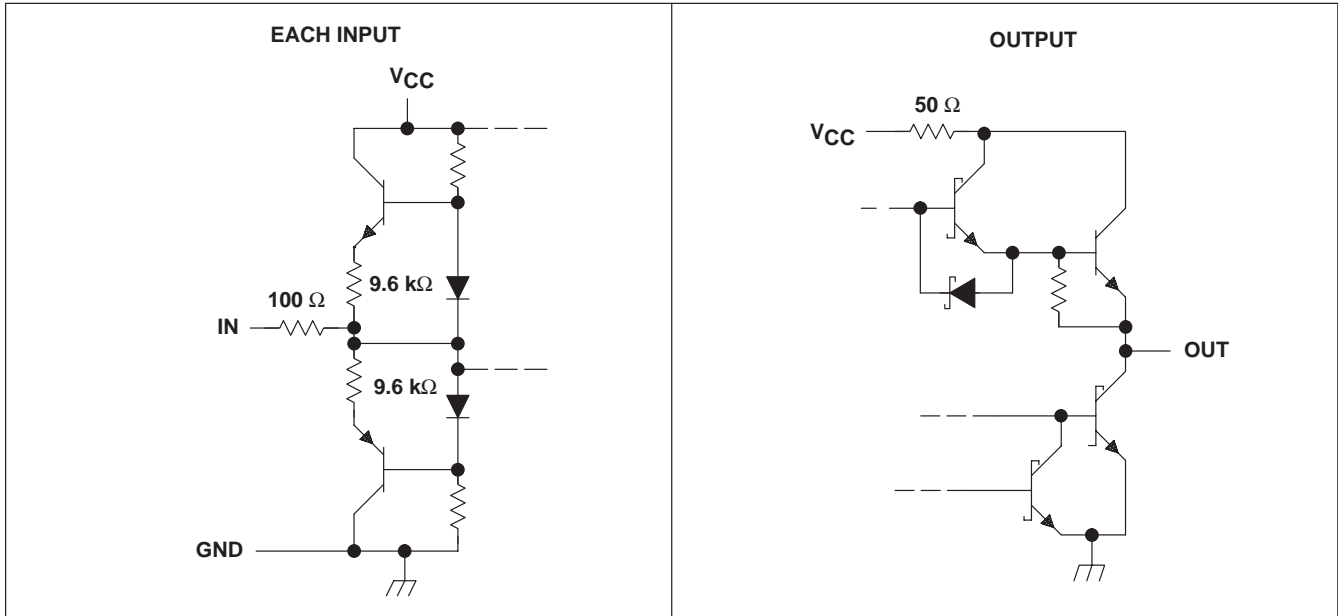


PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TL714C HIGH-SPEED DIFFERENTIAL COMPARATOR

SLCS015A – DECEMBER 1988 – REVISED AUGUST 2003

schematic of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Differential input voltage, V_{ID} (see Note 2)	± 5 V
Input voltage range, V_I	V_{CC} to GND
Low-level output current, I_{OL}	40 mA
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package	97°C/W
P package	85°C/W
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values, except differential voltage, are with respect to the network ground.
 - Differential voltage values are at $IN+$ with respect to $IN-$.
 - Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.75	5.25	V
V_{IC} Common-mode input voltage	1.4 to $V_{CC}-1.4$		V
I_{OH} High-level output current		-1	mA
I_{OL} Low-level output current		16	mA
T_A Operating free-air temperature	0	70	°C

TL714C HIGH-SPEED DIFFERENTIAL COMPARATOR

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electrical characteristics over free-air operating temperature range, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	$V_{IC} = 1.4\text{ V to } 3.6\text{ V}$	-75‡		75	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)		2	10	30	mV
V_{OH}	High-level output voltage	$V_{ID} = 100\text{ mV}$, $I_{OH} = -1\text{ mA}$	2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{ID} = -100\text{ mV}$, $I_{OL} = 16\text{ mA}$		0.4	0.5	V
I_{OS}	Short-circuit output current		-30		-110	mA
r_i	Differential input resistance		2.9			k Ω
I_{CC}	Supply current	$V_{ID} = -100\text{ mV}$, $I_O = 0$		7	12	mA

† All typical values are at $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}	Maximum operating frequency	$V_{ID} = \pm 250\text{ mV}$, $C_L = 25\text{ pF}$, $t_r = t_f = 4\text{ ns}$, Input duty cycle = 50%		50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{ID} = \pm 100\text{ mV}$, $C_L = 25\text{ pF}$, See Figures 1 and 2		6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			6	12	ns
t_r	Rise time	$V_{ID} = \pm 100\text{ mV}$, $C_L = 25\text{ pF}$, See Figure 3		4	8	ns
t_f	Fall time			4	8	ns

† All typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

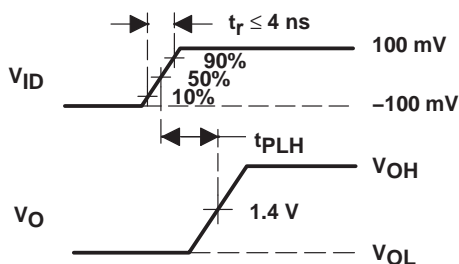


Figure 1. Propagation Delay Time, Low to High (t_{PLH})

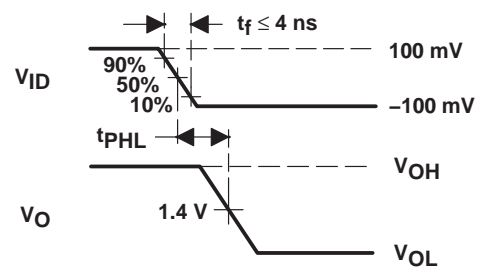


Figure 2. Propagation Delay Time, High to Low (t_{PHL})

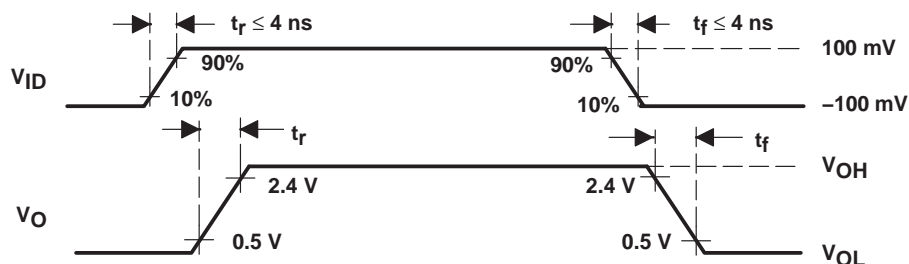


Figure 3. Rise and Fall Times (t_r , t_f)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL714CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL714CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL714CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL714CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL714CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL714CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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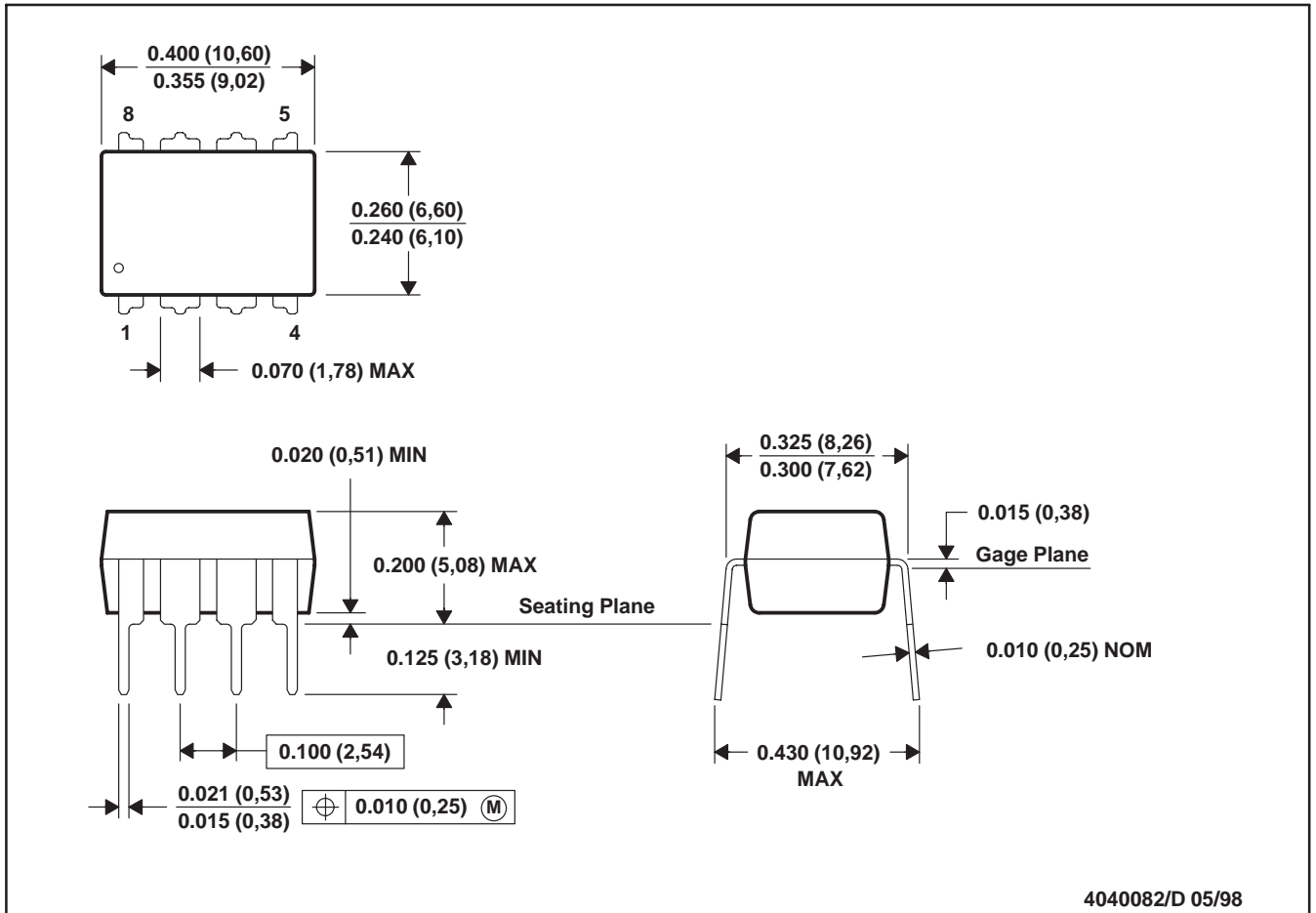
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MECHANICAL DATA

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



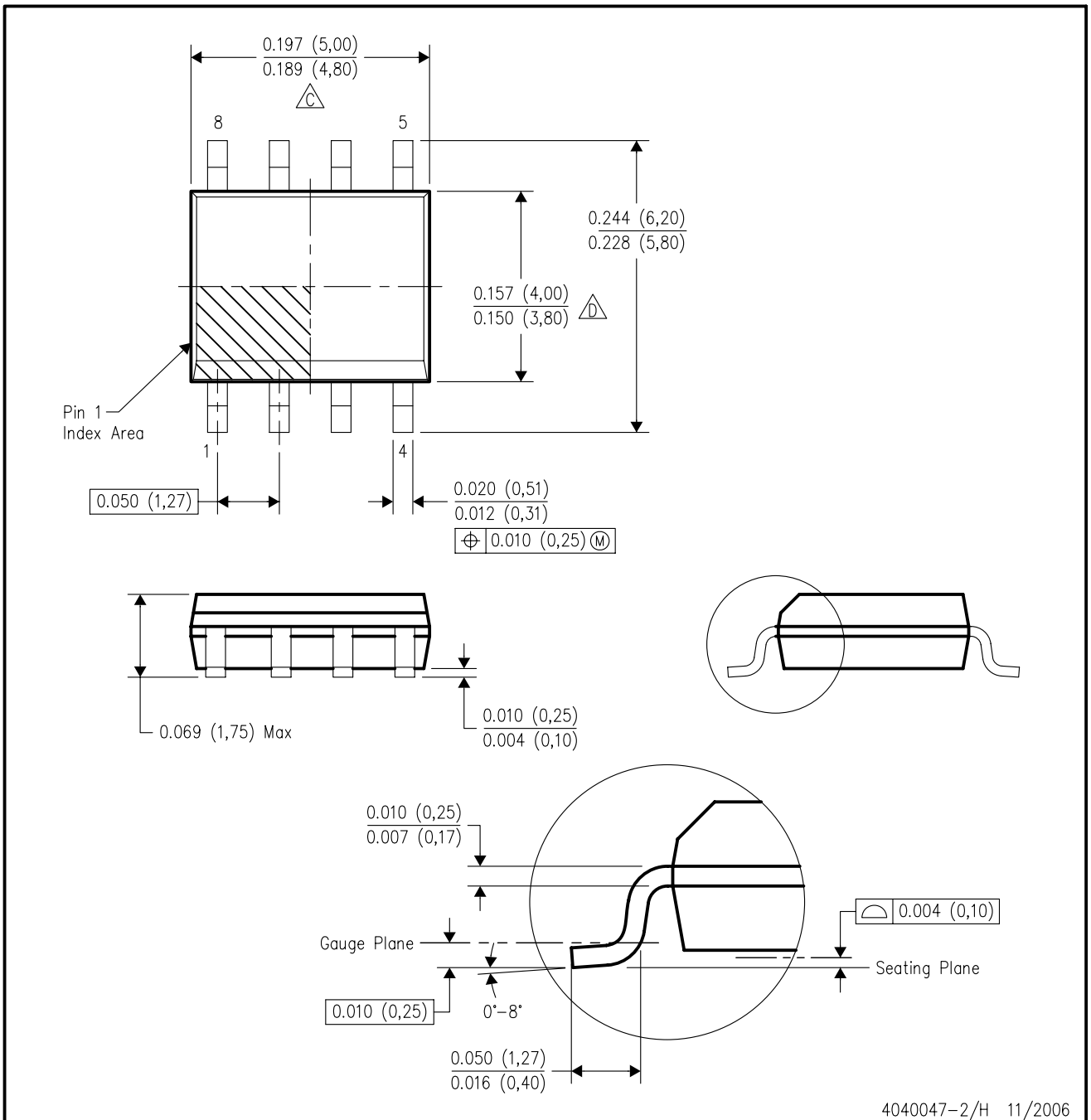
4040082/D 05/98

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

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