TEXAS INSTRUMENTS

THS0842 EVM

User's Guide

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Preface

Read This First

About This Manual

This document presents a description of the THS0842 evaluation module.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Overview
- Chapter 2 – Circuit Functionality
- Chapter 3 – Layout, Decoupling, and Grounding Considerations
- Chapter 4 – PC Board and Bill of Materials
- Appendix A – Schematics

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Chapter 1

Overview

This chapter gives a general overview of the THS0842 evaluation module (EVM), and describes some of the factors that must be considered in using the module.

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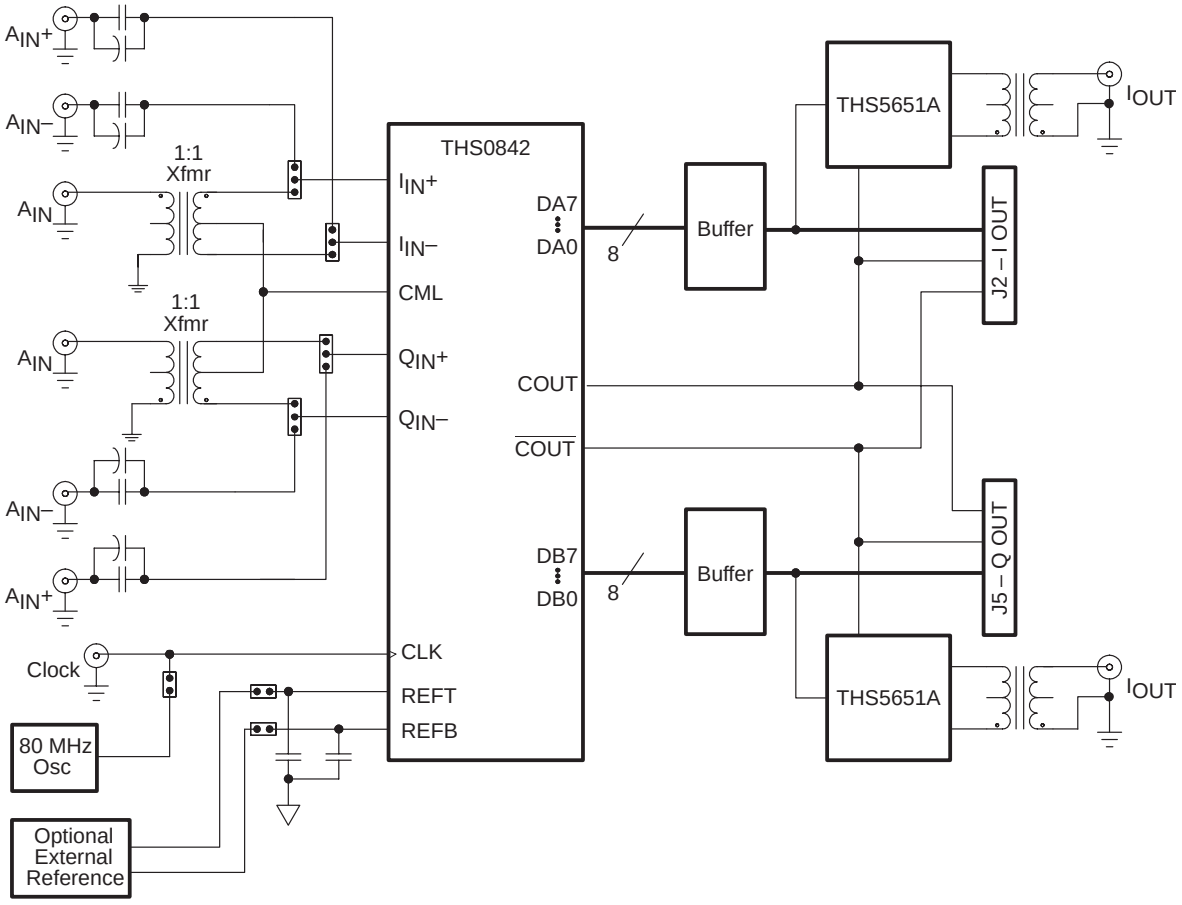
1.1 Purpose

The THS0842 evaluation module (EVM) provides a platform for evaluating the THS0842 analog-to-digital converter (ADC) under various signal, reference, and supply conditions. The system block diagram is shown below. This illustration provides a general indication of the features and functions available. It should be read in combination with the circuit schematic supplied.

Figure 1–1. Block Diagram



1.2 EVM Basic Function

Analog inputs to the ADC are provided via six external SMB connectors. Two pairs of SMB connectors provide true differential inputs, or two individual SMB connectors provide single-ended transformer-coupled signals to the inputs of the device.

The EVM provides an external SMB connection for input of the ADC clock. A crystal oscillator is provided on the board to perform this function and can be used when required. Refer to the section on clocking for correct provisioning.

Digital output from the EVM is via two 25-pin connectors. The digital lines from the ADC are buffered before going to the connectors. More information on these connectors can be found in the ADC output section.

Analog output from the EVM is via two SMB connectors (J1 and J3). A pair of THS5651 10-bit DACS are used to recreate the analog signal from the ADC's digital data. More information on this can be found in the ADC analog output section.

Power connections to the EVM are via a pair of screw-down connectors. Separate input connectors are provided for the analog and digital supplies.

1.3 Power Requirements

The EVM is powered directly through independent 3.3-V analog and digital supplies.

1.3.1 Voltage Limits

Exceeding the 3.3-V maximum can damage EVM components. Under voltage may cause improper operation of some or all of the EVM components.

1.4 THS0842 EVM Operational Procedure

The THS0842 EVM provides a flexible means of evaluating the THS0842 in a number of modes of operation. A basic setup procedure that can be used as a board confidence check follows:

1) Verify all jumper settings against the schematic jumper list in Table 1–1:

Table 1–1. Jumper List Table

Jumper	Function	Installed	Removed	Default
W1	Reserved for future use	Required	Do not use	Installed
W2	Reserved for future use	Required	Do not use	Installed
W3	Oscillator power down	Power down	Active	Installed
W4	Reference select	Internal	External	Installed
W5	THS0842 standby	Active	Power down	Installed
W6	Select clock source	Onboard	Offboard	Removed
W7	Digital bus output enable	3-state bus	Active	Removed
W8	Single/dual bus mode	Dual mode	Single mode	Installed
W9	External REFB source	1–2 onboard	2–3 offboard	1–2
W10	External REFB feed	External	Internal	Removed
W11	External REFT feed	External	Internal	Removed
W12	Q+ Input select	1–2 differential	2–3 single-ended	2–3
W13	Q– Input select	1–2 differential	2–3 single-ended	2–3
W14	I+ Input select	1–2 differential	2–3 single-ended	2–3
W15	I– Input select	1–2 differential	2–3 single-ended	2–3
W16	External REFT source	1–2 onboard	2–3 offboard	1–2

Table 1–2. Default Jumper Positions

EVM	Jumper Table (connection)
THS0842	W1, W2, W3, W4, W5, W7, W9 (1–2), W12 (2–3), W13 (2–3), W14(2–3), W15 (2–3), W16(1–2)

1) Set both dc power supplies to read 3.3 V at the output terminals. Connect GND of the first power supply to the AGND(J6–2) terminal on the EVM, and GND of the other power supply to the DGND(J7–2) terminal on the EVM. Then connect the first power supply's 3.3-V output to the AVDD power (J6–1) terminal of the EVM, and the other power supply's 3.3-V output to the DVDD(J7–1) terminal of the EVM.

2) Switch power supplies on.

3) Set function generator number one to output a square wave at a frequency of 80 MHz, 0-V offset, and an amplitude of 3.3 V on the 50-Ω output.

4) Use a 50-Ω coaxial cable with BNC/SMB connectors to connect generator number 1 to J4 (clock input).

5) Set function generator number 2 to output a sine wave at a frequency of 1 MHz, 0-V offset, and an amplitude of 0.8 Vp-p on the 50-Ω output.

6) Use a 50-Ω coaxial cable with BNC/SMB connectors to connect generator number 2 to J8 (Q input). Use a T-splitter to connect the test signal to channel 1 of the oscilloscope.

7) Use a 50-Ω coaxial cable with BNC/SMB connectors to connect the second channel of the oscilloscope to J3 (Q-output). The two sine waves should have the same period (their amplitudes may differ).

8) Repeat Step 5 with the SMB connected to J11 (I-input).

9) Repeat Step 6, except connect to J1 (I-output).

Chapter 2

Circuit Functionality

This chapter describes the digital interface-master clock, ADC data, and power supply.

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2.1 Circuit Function

The following sections describe the function of individual circuits. Refer to the relevant data sheet for device operating characteristics.

2.2 Analog Inputs

The ADC has either transformer-coupled single-ended or differential-analog inputs. These are provided on the EVM via SMB connectors J8 and J11 for single-ended inputs, or J9/J10 and J12/J13 for differential inputs, and can be configured in two ways, as discussed in Sections 2.2.1 and 2.2.2.

2.2.1 Single-Ended Transformer Coupled Interface

Connectors J8 (Q) and J11 (I) are single-ended inputs that use a 1:1 transformer to provide differential analog inputs to the I+/I– and Q+/Q– inputs of U11 (THS0842). The signal input is nominally 0.89 Vpp.

W12, W13, W14, and W15 should be strapped across pins 2 and 3. The inputs have 50-Ω terminators.

2.2.2 Differential Interface

Connectors J9 (Q+), J10 (Q–), J12 (I–), and J13 (I+) are used to connect ac-coupled differential signals directly to U11 (THS0842). The signal input is nominally a 0.44 Vpp.

W12, W13, W14, and W15 should be strapped across pins 1 and 2.

2.3 Digital Inputs

The THS0842 EVM utilizes jumpers for all digital inputs, with the exception of the external clock. There are no connectors for setting the digital inputs. Refer to the jumper table (Table 1–1) for a description of the jumpers and their function.

2.3.1 Internal Clock

The EVM provides flexibility as to the source of the ADC's conversion clock. This clock can come from an external signal generator, as described in Section 2.3.2, or by enabling onboard 80-MHz oscillator X1. Removing the shorting bar from W3 will enable oscillator X1. Adding a shorting bar to jumper pins W6 will direct clock oscillations from oscillator X1 to buffer amplifier U10A and to the rest of the circuit. The EVM is shipped with external clock selected, W6 open, and W3 shorted.

Note:

R49 must be removed to avoid loading the output of X1.

2.3.2 External Clock

SMB Connector J4 can be used to input a clock signal to the board from an external source. The input source should be a 50-Ω LVTTL square wave signal with an amplitude of 3.3 V referenced to digital ground. This is the default setup for the EVM.

2.4 Analog Output

The ADC digital data is buffered and sent to a pair of THS5651A DACs. The 5651 DACs latch the THS0842 data on COUT (Q-DAC) or /COUT (I-DAC). An analog signal is generated on J1 for the I-output and J3 for the Q-output. The DAC outputs can only be used when the THS0842 EVM is set up for dual-bus mode (W8 installed, SELB low). For further information on the THS5651A, please refer to the product folder on TI's website:

http://www.ti.com/sc/docs/products/analog/ths5651a.html.

2.5 Digital Output

The digital-output codes of the ADC are made available on two 26-pin headers along with COUT and $\overline{\text{COUT}}$. J2 provides access to the data from the I-input and J5 provides access to the data from the Q-input. The output is 3.3 V TTL-compatible.

Table 2–1. Daughtercard Connector J2

J2 Pin	Name	Function	J2 Pin	Name	Function
1	DA0	$I_{OUT}0$	2	DGND	Ground
3	DA1	$I_{OUT}1$	4	DGND	Ground
5	DA2	$I_{OUT}2$	6	DGND	Ground
7	DA3	$I_{OUT}3$	8	DGND	Ground
9	DA4	$I_{OUT}4$	10	DGND	Ground
11	DA5	$I_{OUT}5$	12	DGND	Ground
13	DA6	$I_{OUT}6$	14	DGND	Ground
15	DA7	$I_{OUT}7$	16	DGND	Ground
17	RSVD	NC	18	DGND	Ground
19	RSVD	NC	20	DGND	Ground
21	$\overline{\text{COUT}}$	$\overline{\text{COUT}}$ clock	22	DGND	Ground
23	COUT	COUT clock	24	DGND	Ground
25	80 MHz	80-MHz clock	26	DGND	Ground

Table 2–2. Daughtercard Connector J5

J2 Pin	Name	Function	J2 Pin	Name	Function
1	DB0	$Q_{OUT}0$	2	DGND	Ground
3	DB1	$Q_{OUT}1$	4	DGND	Ground
5	DB2	$Q_{OUT}2$	6	DGND	Ground
7	DB3	$Q_{OUT}3$	8	DGND	Ground
9	DB4	$Q_{OUT}4$	10	DGND	Ground
11	DB5	$Q_{OUT}5$	12	DGND	Ground
13	DB6	$Q_{OUT}6$	14	DGND	Ground
15	DB7	$Q_{OUT}7$	16	DGND	Ground
17	RSVD	NC	18	DGND	Ground
19	RSVD	NC	20	DGND	Ground
21	$\overline{\text{COUT}}$	$\overline{\text{COUT}}$ clock	22	DGND	Ground
23	COUT	COUT clock	24	DGND	Ground
25	80 MHz	80-MHz clock	26	DGND	Ground

2.6 References

The EVM can use either the THS0842 internal reference, a tunable external reference generated on the EVM board, or a customer-provided external reference.

The THS0842's input range is determined by the voltages on its V_{REFB} and V_{REFT} pins. Since the part has an internal-voltage reference generator, it must be powered down (W4 removed) before applying an external voltage to the REFT and REFB pins. It is advantageous to have a wider analog input range, especially at higher sampling rates. This can be achieved by using external voltage references. For example, at AV_{DD} = 3.3 V, the full-scale range can be extended from 1 Vpp (internal reference) to 1.3 Vpp (external reference), as shown in Table 3–3. These voltages should *not* be derived from a power-supply source via a voltage divider. Use instead a bandgap-derived voltage reference to derive both references via an operational-amplifier circuit. Refer to the schematic of the THS0842 evaluation module for an example circuit.

The full-scale ADC input range and its dc position can be adjusted when using external references. The full-scale ADC range is always equal to V_{REFT} – VREFB. The maximum full-scale range is dependent on AVDD, as shown in the THS0842 data sheet specifications section. Aside from the constraint on their difference, there are limitations on the useful range of V_{REFT} and V_{REFB} individually, depending on the value of AV_{DD}. Table 3–3 summarizes these limits for three cases.

Table 2–3. Minimum/Maximum Reference Input Levels

AV_{DD}	$V_{REFB(min)}$	$V_{REFB(max)}$	$V_{REFT(min)}$	$V_{REFT(max)}$	$[V_{REFT}–V_{REFB}]_{max}$
3.0 V	0.8 V	1.2 V	1.8 V	2.2 V	1.0 V
3.3 V	0.8 V	1.2 V	2.1 V	2.5 V	1.3 V
3.6 V	0.8 V	1.2 V	2.4 V	2.8 V	1.6 V

2.7 Power

Power is supplied to the EVM via screw-down connectors. For best performance use a separate low-noise analog power supply connected to J6–1 (+3.3 V) and J6–2 (GND). Use a separate low-noise digital power supply connected to J7–1 (+3.3 V) and J7–2 (GND). The positive side is marked by a + on the EVM's silkscreen placed next to the connectors themselves.

Chapter 3

Layout, Decoupling, and Grounding Considerations

Proper grounding and layout of the PCB is essential to achieve the stated performance. It is advised to use separate analog and digital ground planes that are spliced underneath the device. The THS0842 has digital and analog terminals on opposite sides of the package to make this easier. Since there is no internal connection between analog and digital grounds, they have to be joined on the PCB. This should be done at one point in close proximity to the THS0842.

Separate analog and digital power-supply terminals are provided on the device (AV_{DD} /DV_{DD}). The supply to the digital-output drivers (DRV_{DD}) is also kept separate. Lowering the voltage on this supply to 3 V instead of the nominal 3.3 V improves performance due to the lower switching noise caused by the output buffers.

Because of the high sampling rate and switched-capacitor architecture, the THS0842 generates transients on the supply and reference lines. Proper decoupling of these lines is essential. Decoupling as shown in the schematic of the THS0842 EVM is recommended.

Chapter 4

PC Board and Bill of Materials

This chapter presents the PC board design and a listing of the parts required to build this evaluation module

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4.1 Printed-Circuit Board

This section presents the printed-circuit board for the THS0842 EVM.

Figure 4–1. Printed-Circuit Board (Top)

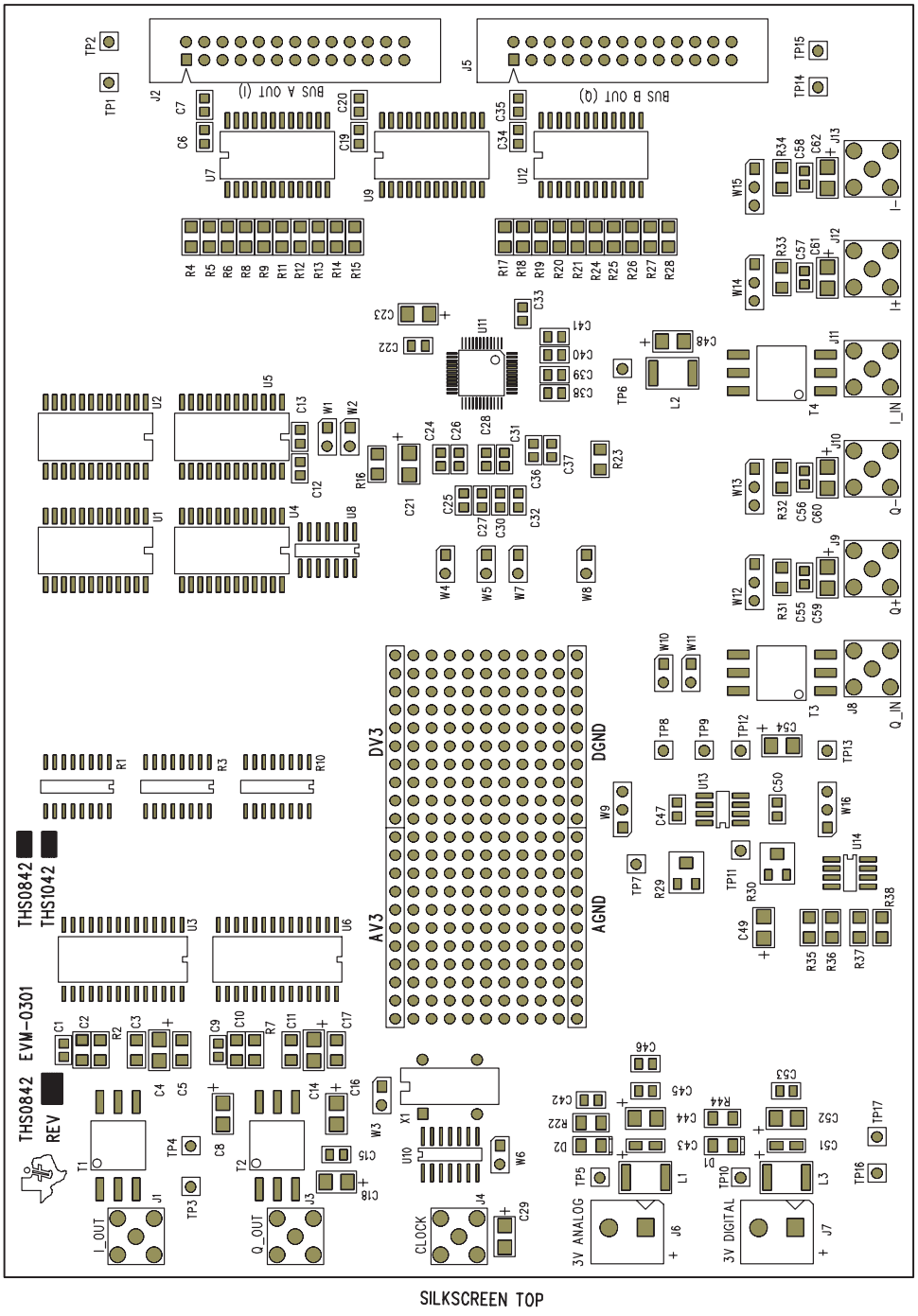
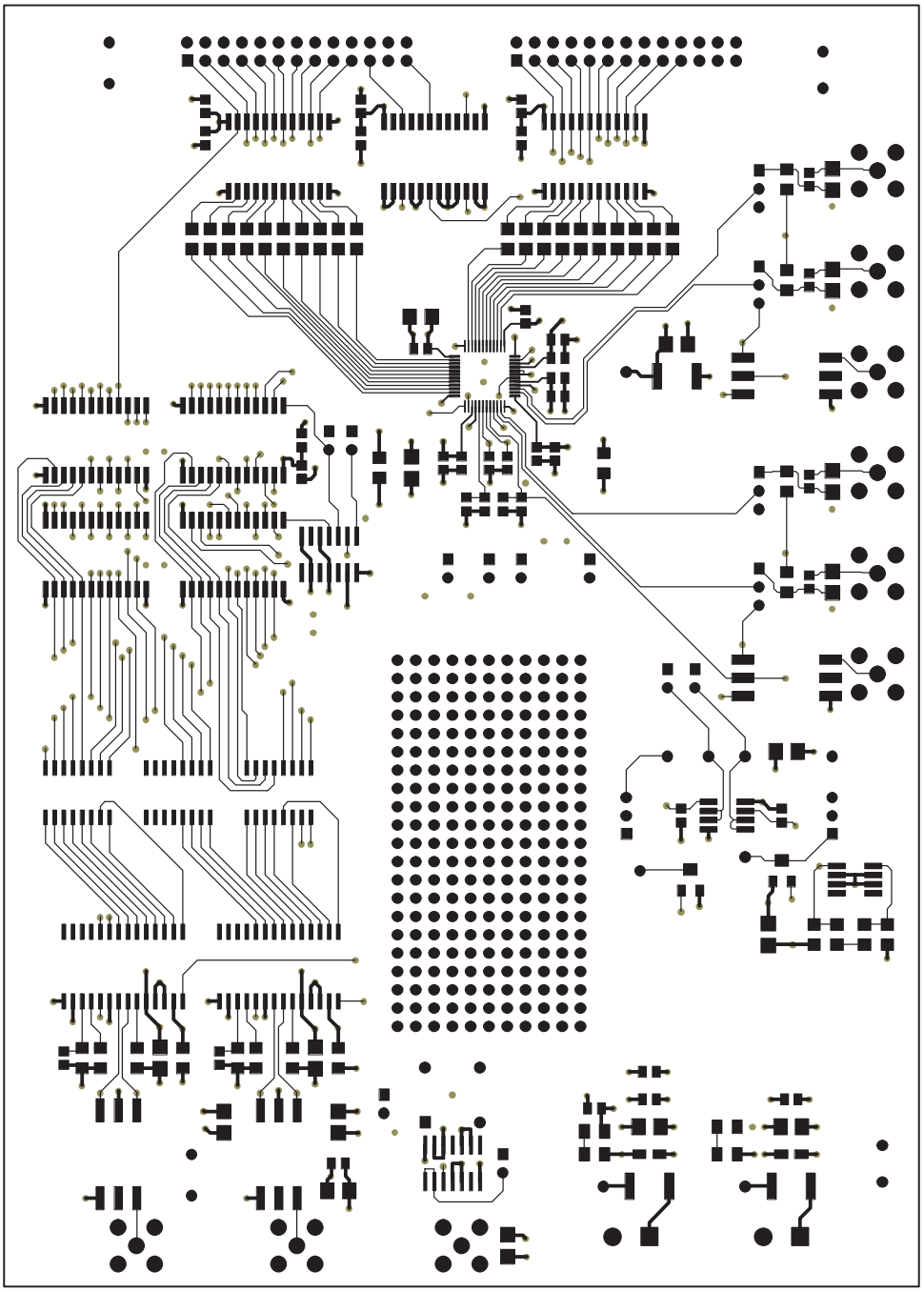


Figure 4–2. Printed-Circuit Board Layer 1



LAYER 1 – COMPONENT SIDE (TOP)

Figure 4–3. Printed-Circuit Board Layer 2

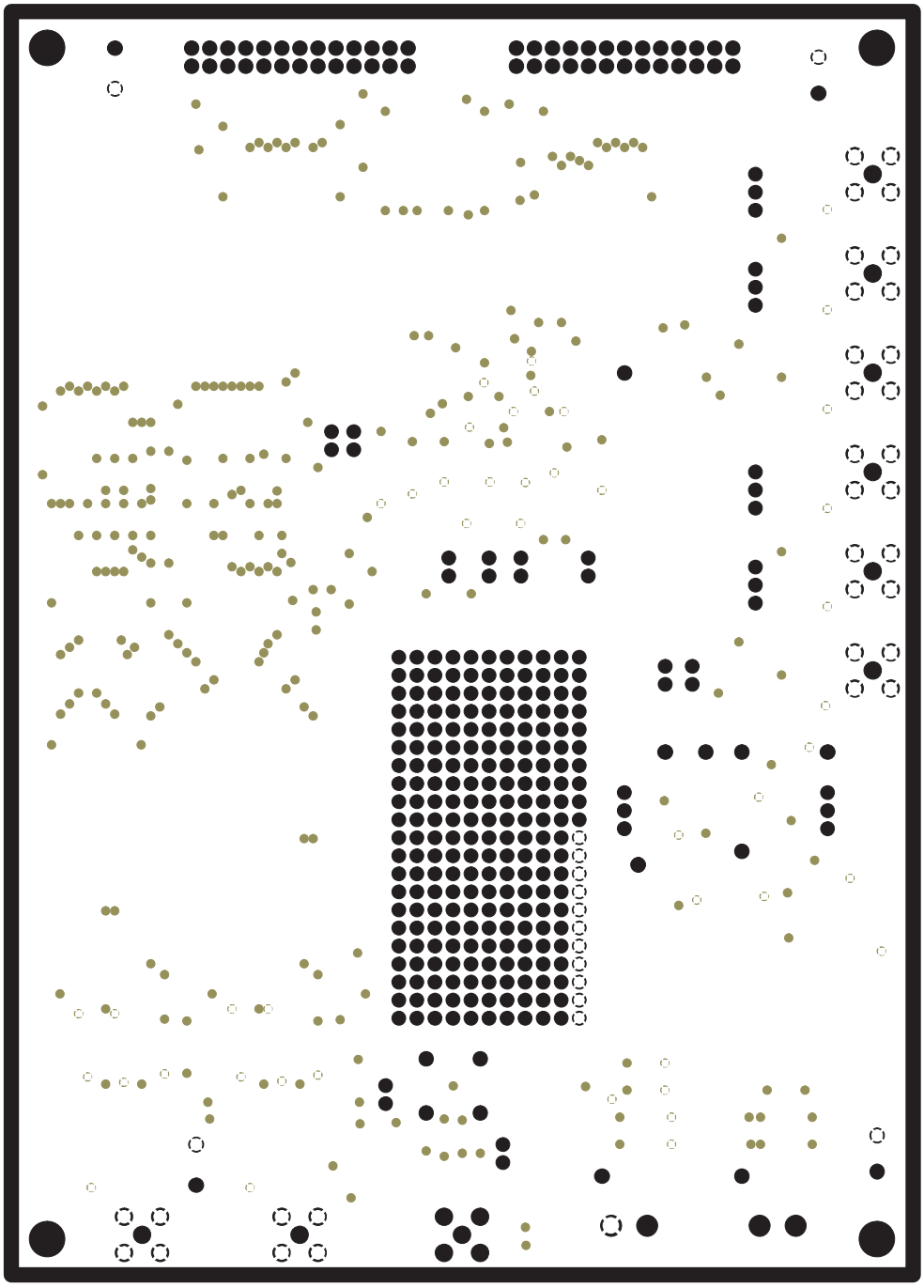


Figure 4–4. Printed-Circuit Board Layer 3

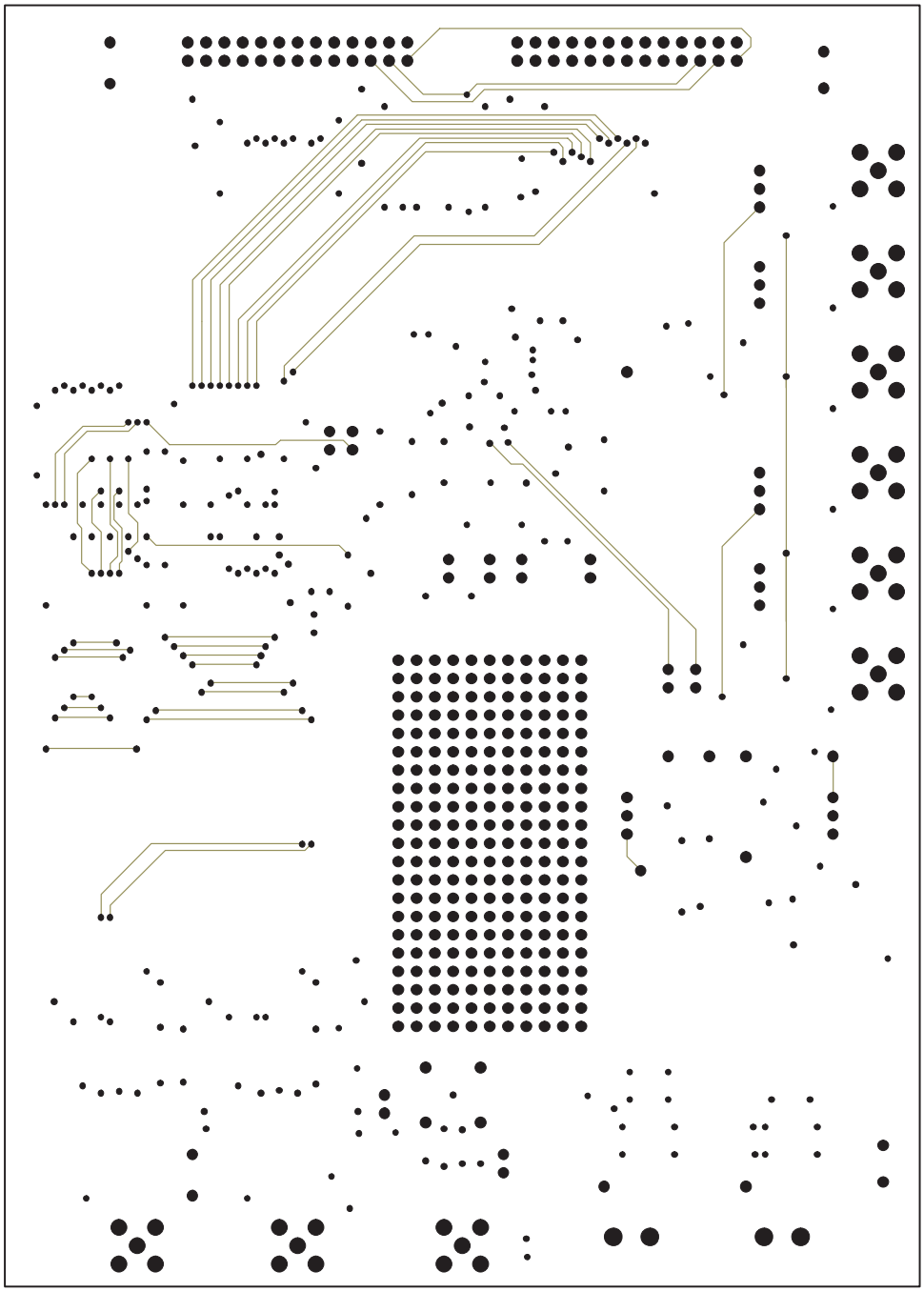


Figure 4–5. Printed-Circuit Board Layer 4

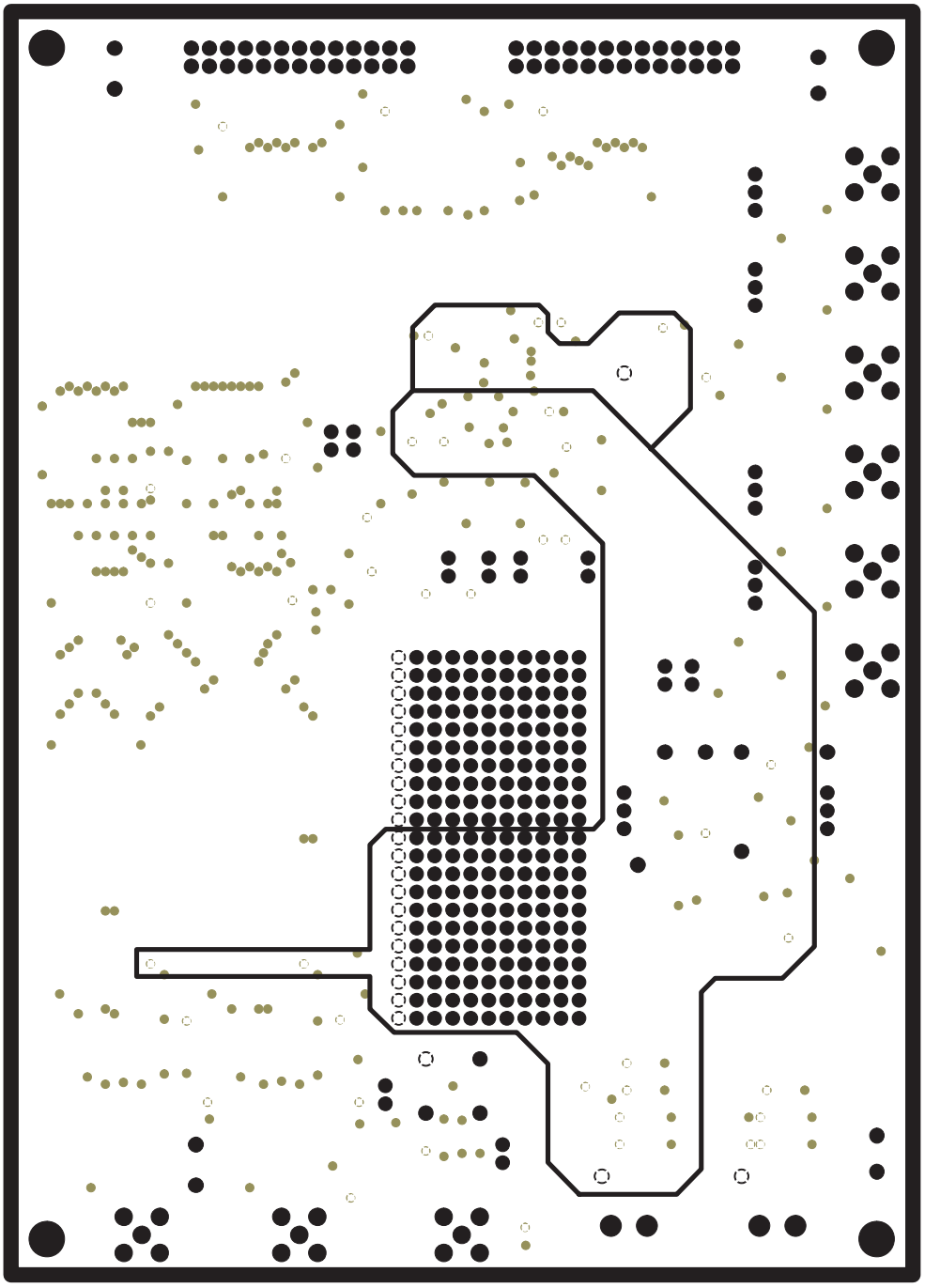


Figure 4–6. Printed-Circuit Board Layer 5

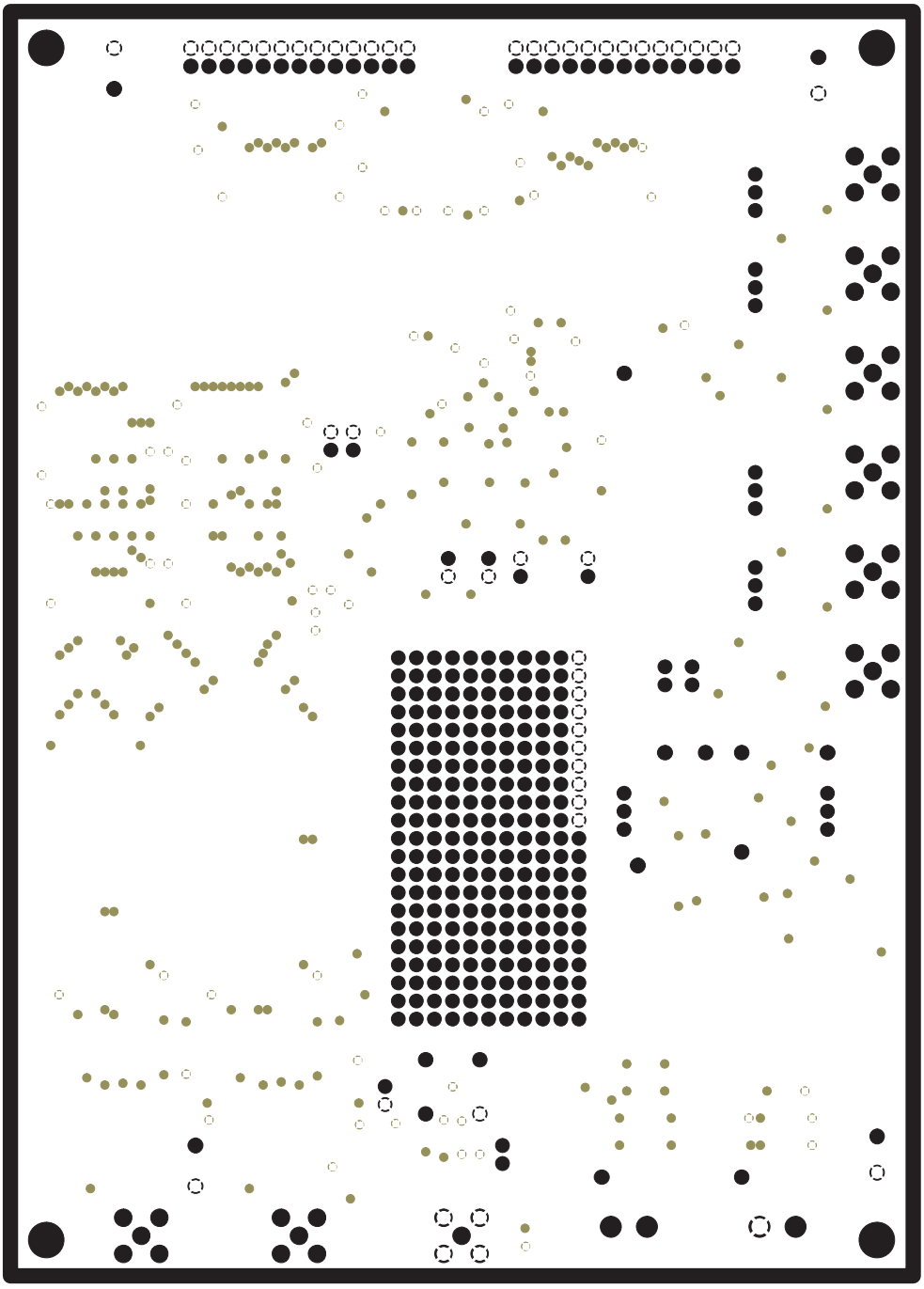


Figure 4–7. Printed-Circuit Board Layer 6

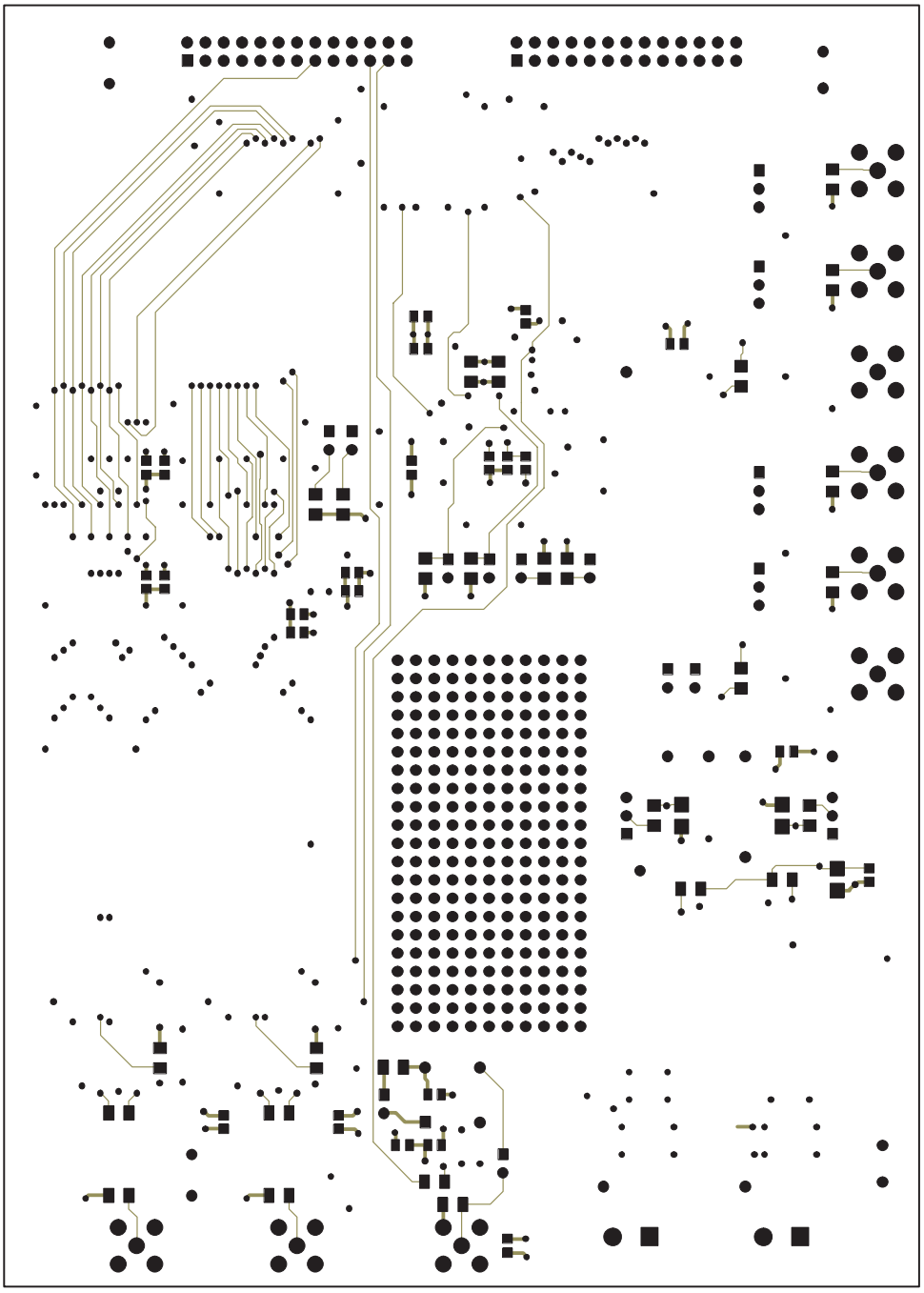
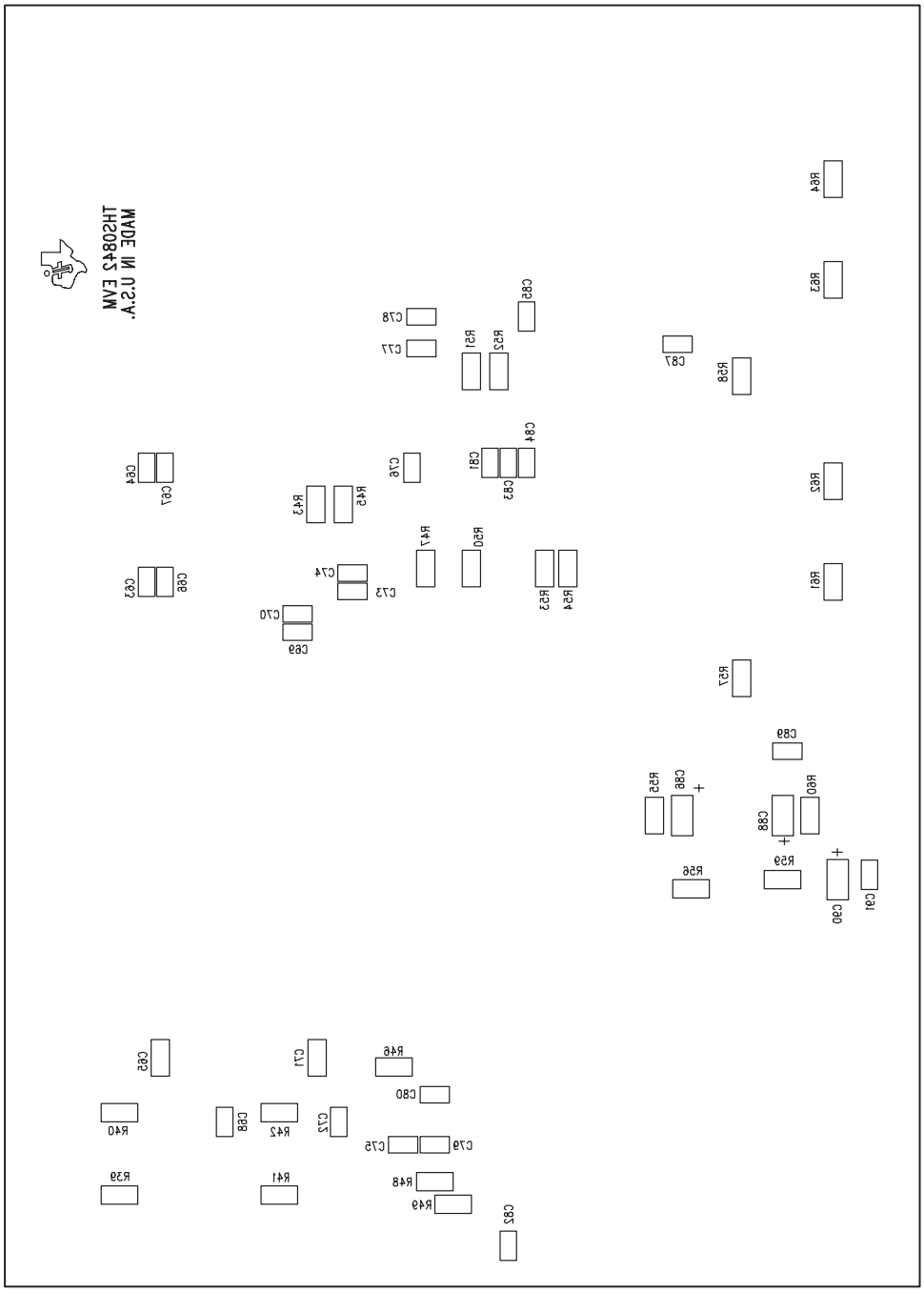


Figure 4–8. Printed-Circuit Board (Bottom)



4.2 Bill of Materials

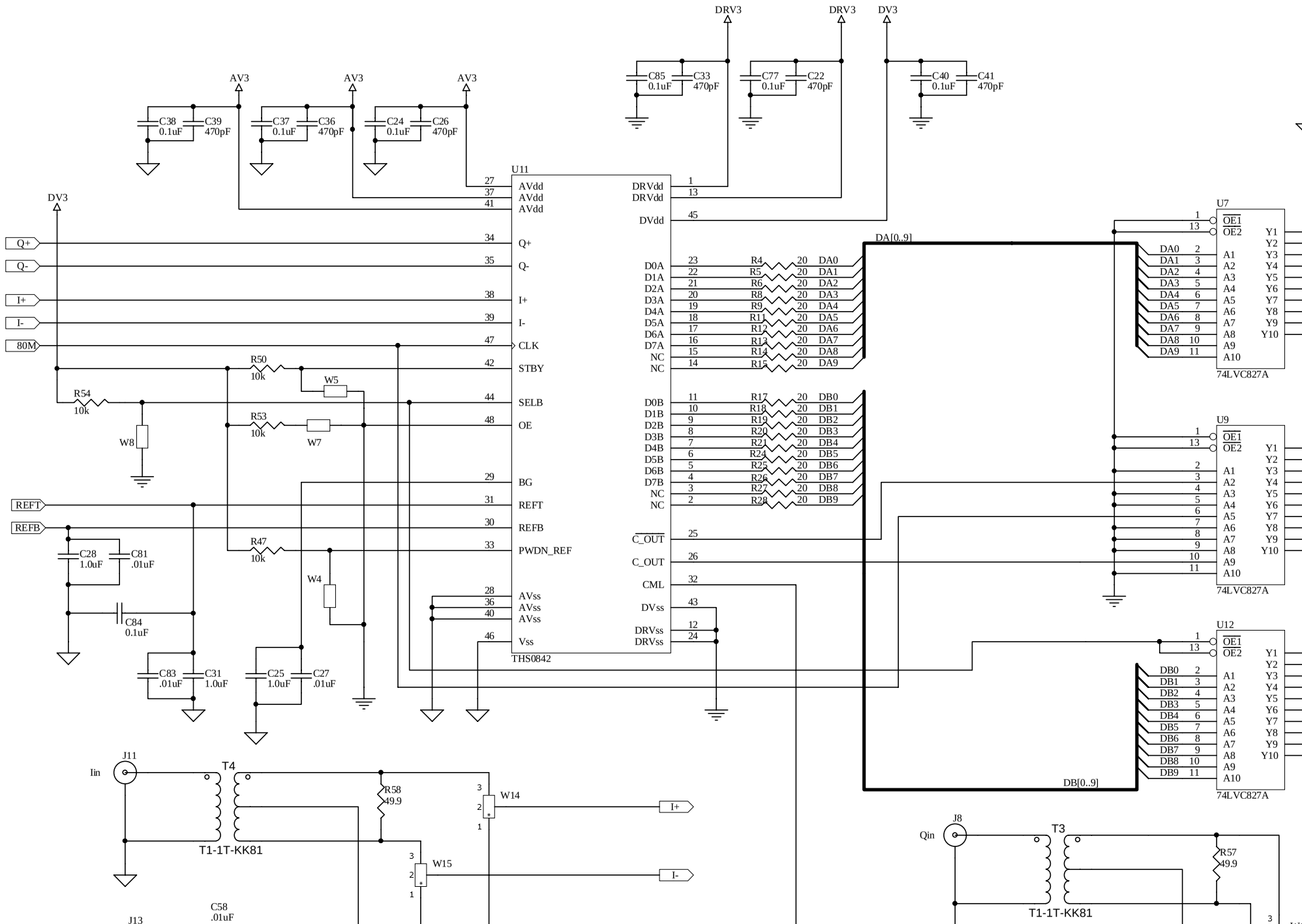
Part Type	Designator	Footprint	Description	Manufacturer	Part Number
10 µF	C4, C8, C12, C14, C16, C18, C21, C23, C29, C44, C48, C49, C52, C54, C59, C60, C61, C62, C86, C88, C90	3528	Low profile tantalum capacitor	Digikey	PCS1156CT–ND
0.1 µF	C2, C3, C5, C10, C11, C17, C65, C71	1206	Multilayer ceramic – variable footprint	Mouser	77–VJ12U50V104M
0.1 µF	C6, C13, C15, C19, C24, C34, C37, C38, C40, C42, C45, C46, C47, C50, C53, C63, C67, C68, C69, C72, C73, C75, C76, C77, C78, C80, C82, C84, C85, C87, C89, C91	805	Multilayer ceramic	Mouser	77–VJ08Y50V104K
4.7 µF	C43, C51	3216	Low profile tantalum capacitor	Digikey	PCS1475CT–ND
470 pF	C7, C12, C20, C22, C26, C33, C35, C36, C39, C41, C64, C66, C70, C74, C79	805	Multilayer ceramic	Mouser	77–VJ08A100V471J
1.0 µF	C25, C28, C31, C32	805	Multilayer ceramic	Digikey	PCC1807CT–ND
0.01 µF	C1, C9, C27, C30, C55, C56, C57, C58, C81, C83	805	Multilayer ceramic	Mouser	77–VJ08Y50V103K
GREEN LED	D1, D2	LED–1206	LED with LENS	Lumex	67–1357–1
SMA JACK	J3	SMA_JACK	PCB mount SMA jack	Johnson Components	142–0701–206
KRMZ2	J6, J7	2term_screw_con	2 Terminal screw connector		506–5ULV02
SMA	J1, J4, J8, J9, J10, J11, J12, J13	SMA_JACK	PCB mount SMA jack	Johnson Components	142–0701–206
26PIN_IDC	J2, J5	13×2×0.1	26 Pin header		TSW–113–07–L–D
4.7 µH	L1, L3	DO1608C	DO1608C-Series – Coil Craft		
1.0 µH	L2	DO1608C	DO1608C-Series – Coil Craft		
20	R4, R5, R6, R8, R9, R11, R12, R13, R14, R15, R17, R18, R19, R20, R21, R24, R25, R26, R27, R28, R48	1206		Mouser	263–20
49.9	R39, R40, R41, R42, R49, R57, R58, R61, R62, R63, R64	1206	1/4W 1210 Chip resistor	Mouser	290–49.9

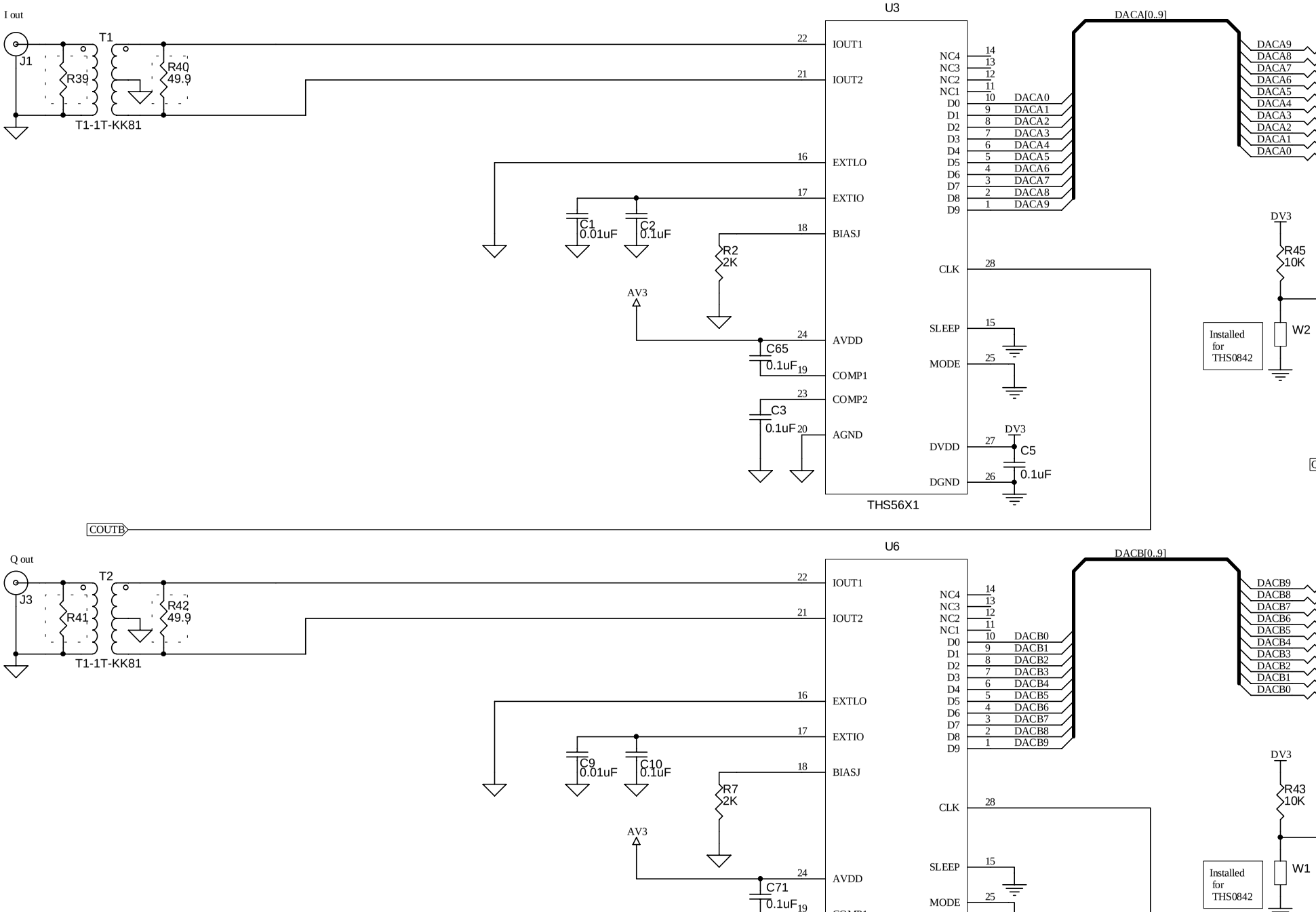
Part Type	Designator	Footprint	Description	Manufacturer	Part Number
750	R36	1206	1/4W 1206 Chip resistor 1%	Mouser	290–750
0 Ω	R16, R23, R35, R37, R51, R52	1206	1/4W 1206 Chip resistor	Mouser	263–0
2.49K 1%	R38	1206	1/4W 1206 Chip resistor	Mouser	263–2.49K
1.0 K	R22, R44, R56, R59	1206	1/4W 1206 Chip resistor	Mouser	263–1K
2K POT	R29, R30	BOURNS		Digikey	3214W–202ECT–ND
33 Ω	R1, R3, R10	2NBS16	Bourns 2NBS Series		4816P–1–330
2K	R2, R7	1206	1/4W 1206 Chip resistor	Mouser	263–2.00K
10K	R31, R32, R33, R34, R43, R45, R46, R47, R50, R53, R54, R55, R60,	1206	1/4W 1206 Chip resistor	Mouser	263–10K
1.0K	R44	1206	1/4W 1206 Chip resistor	Mouser	263–1K
T1–1T–KK81	T1, T2, T3, T4	MC_KK81	RF transformer MINI-circuits T1–1T–KK81		
TSW–101–07–LS	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP9, TP10, TP11, TP12, TP14, TP15, TP16, TP17	test_point2	Turret terminal test point	Samtec	TSW–101–07–LS
REF– REF+	TP8 TP13	test_point2	Turret terminal test point	Samtec	TSW–101–07–LS
74LVC827A	U1, U2, U4, U5, U7, U9, U12	24 SOP (DW)	10-Bit bus interface FF 3SO	TI	SN74LVC827ADW
SN74HC04D	U8	14–SOP(D)	Hex inverter	TI	SN74HC04D
SN74LVC08A	U10	14–SOP(D)	Quad NAND gate	TI	SN74LVC08AD
TL1431CD	U14	8–SOP(D)	Precision programmable reference	TI	TL1431QD
TLV2772	U13	8–SOP(D)	Dual op amp in 8 pin SOP package	TI	TLV2772ID
THS0842	U11	48–TQFP(PFB)	THS0842	TI	THS0842IPFB
THS56X1	U3, U6	28–SOIC(DW)	2.7–5.5V, 10 bit, 125 MHz, communications DAC	TI	THS5651IDW
TSW–102–07–LS	W1, W2, W3, W4, W5, W6, W7, W8, W9, W10, W11	2pos_jump	2 Position jumper _ 0.1” spacing	Samtec	TSW–102–07–L–S
3POS_JUMPER	W9, W12, W13, W14, W15, W16	3pos_jump	3 Position jumper _ 0.1” spacing		TSW–103–07–L–S
XTAL	X1	4PIN_XTL_DC	Crystal oscillator 80 MHz	Digikey	SG–8002DC–SCC–80.00 MHz

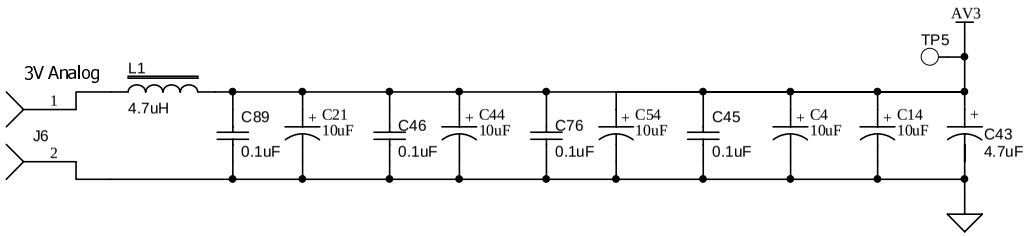
Appendix A

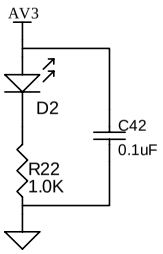
Schematics

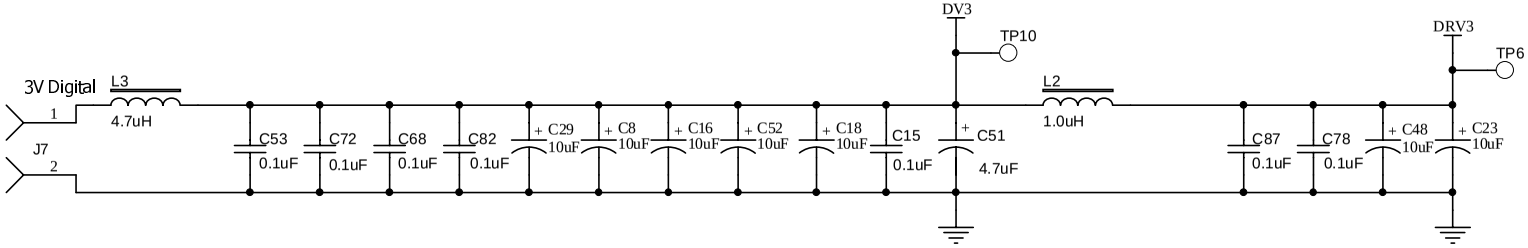
This Appendix contains the THS0842 EVM schematics.

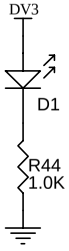

1
2
3
4
D
C
B
DRV3
DRV3
DV3
AV3
AV3
AV3
C85 0.1uF
C33 470pF
C77 0.1uF
C22 470pF
C40 0.1uF
C41 470pF
C38 0.1uF
C39 470pF
C37 0.1uF
C36 470pF
C24 0.1uF
C26 470pF
U11
27 AVdd
37 AVdd
41 AVdd
DRVdd 1
DRVdd 13
DVdd 45
Q+ 34 Q+
Q- 35 Q-
I+ 38 I+
I- 39 I-
80M 47 CLK
42 STBY
44 SELB
48 OE
29 BG
31 REFT
30 REFB
33 PWDN_REF
28 AVss
36 AVss
40 AVss
46 Vss
THS0842
D0A 23 R4 20 DA0
D1A 22 R5 20 DA1
D2A 21 R6 20 DA2
D3A 20 R8 20 DA3
D4A 19 R9 20 DA4
D5A 18 R11 20 DA5
D6A 17 R12 20 DA6
D7A 16 R13 20 DA7
NC 15 R14 20 DA8
NC 14 R15 20 DA9
DA[0..9]
D0B 11 R17 20 DB0
D1B 10 R18 20 DB1
D2B 9 R19 20 DB2
D3B 8 R20 20 DB3
D4B 7 R21 20 DB4
D5B 6 R24 20 DB5
D6B 5 R25 20 DB6
D7B 4 R26 20 DB7
NC 3 R27 20 DB8
NC 2 R28 20 DB9
C_OUT 25
C_OUT 26
CML 32
DVss 43
DRVss 12
DRVss 24
R50 10k
R54 10k
R53 10k
R47 10k
W5
W7
W8
W4
C28 1.0uF
C81 .01uF
C84 0.1uF
C83 .01uF
C31 1.0uF
C25 1.0uF
C27 .01uF
REFT
REFB
U7
U9
U12
74LVC827A
DB[0..9]
J11
Iin
T4
T1-1T-KK81
R58 49.9
W14
W15
I+
I-
J13
C58 .01uF
J8
Qin
T3
R57 49.9

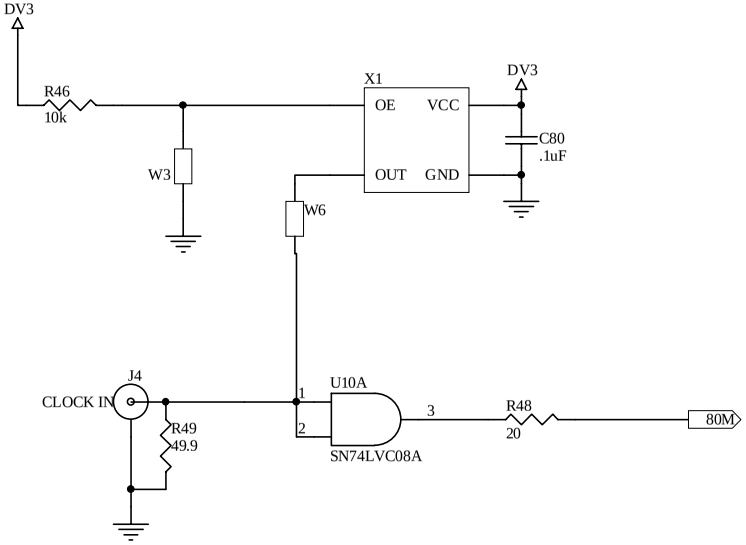

I out
T1
J1
R39
R40
49.9
T1-1T-KK81
U3
IOUT1
IOUT2
EXTLO
EXTIO
BIASJ
AVDD
COMP1
COMP2
AGND
NC4
NC3
NC2
NC1
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
CLK
SLEEP
MODE
DVDD
DGND
THS56X1
DACA[0..9]
DACA0
DACA1
DACA2
DACA3
DACA4
DACA5
DACA6
DACA7
DACA8
DACA9
C1
0.01uF
C2
0.1uF
R2
2K
AV3
C65
0.1uF
C3
0.1uF
DV3
R45
10K
W2
Installed for THS0842
C5
0.1uF
COUTB
Q out
T2
J3
R41
R42
49.9
T1-1T-KK81
U6
DACB[0..9]
DACB0
DACB1
DACB2
DACB3
DACB4
DACB5
DACB6
DACB7
DACB8
DACB9
C9
0.01uF
C10
0.1uF
R7
2K
C71
0.1uF
R43
10K
W1
Installed for THS0842

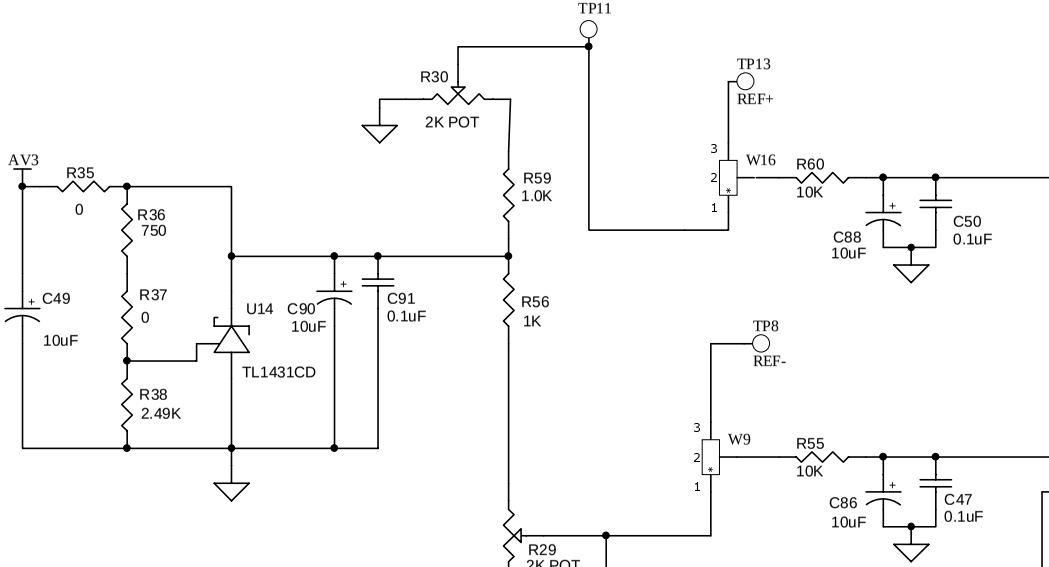

3V Analog
L1
4.7uH
J6
C89
0.1uF
C21
10uF
C46
0.1uF
C44
10uF
C76
0.1uF
C54
10uF
C45
0.1uF
C4
10uF
C14
10uF
C43
4.7uF
AV3
TP5

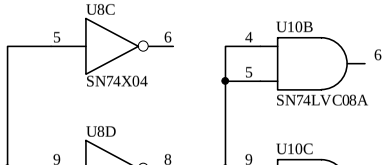

AV3
D2
C42
0.1uF
R22
1.0K


3V Digital
L3
4.7uH
J7
C53
0.1uF
C72
0.1uF
C68
0.1uF
C82
0.1uF
C29
10uF
C8
10uF
C16
10uF
C52
10uF
C18
10uF
C15
0.1uF
C51
4.7uF
DV3
TP10
L2
1.0uH
C87
0.1uF
C78
0.1uF
C48
10uF
C23
10uF
DRV3
TP6


DV3
D1
R44
1.0K


DV3
R46
10k
W3
W6
X1
OE
VCC
OUT
GND
DV3
C80
.1uF
J4
CLOCK IN
R49
49.9
U10A
SN74LVC08A
R48
20
80M


TP11
R30
2K POT
AV3
R35
0
R36
750
R37
0
R38
2.49K
C49
10uF
U14
TL1431CD
C90
10uF
C91
0.1uF
R59
1.0K
R56
1K
R29
2K POT
TP13
REF+
W16
R60
10K
C88
10uF
C50
0.1uF
TP8
REF-
W9
R55
10K
C86
10uF
C47
0.1uF


U8C
SN74X04
U8D
U10B
SN74LVC08A
U10C