

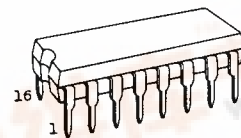
C<sup>2</sup>MOS DIGITAL INTEGRATED CIRCUIT  
SILICON MONOLITHIC

# TC40175BP/BF

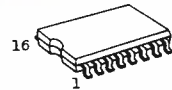
TC40175BP/TC40175BF QUAD D-TYPE FLIP-FLOP

TC40175BP/TC40175BF contains four circuits of D type flip-flop having common clock terminal and clear terminal. The logical input applied to D<sub>n</sub> input is transferred to Q<sub>n</sub> output by the rising edge of CLOCK input.

$\overline{\text{RESET}}$  input is active with "L" level. This has the same functions as TTL 54175/74175 and the pin assignment is also same.



DIP 16(3D16A-P)

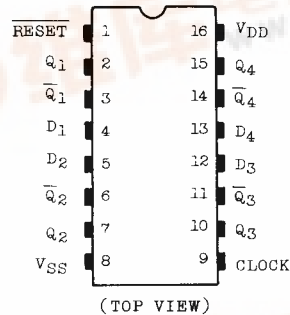


MFP 16(F16GC-P)

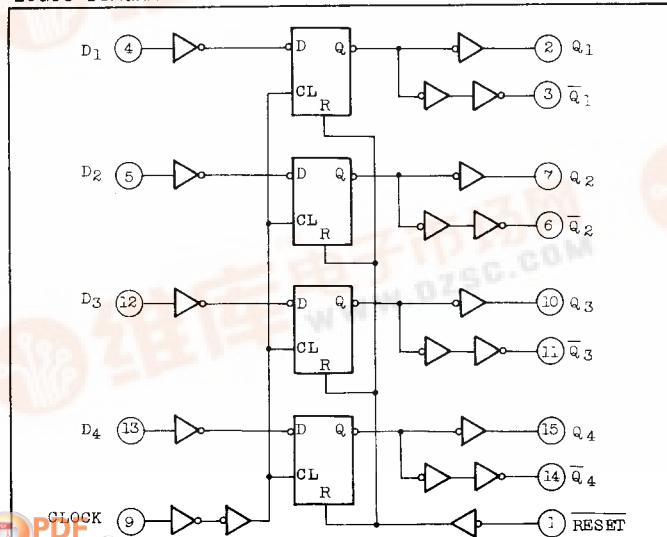
### MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.5 ~ V <sub>SS</sub> +20	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V
DC Input Current	I <sub>IN</sub>	±10	mA
Power Dissipation	P <sub>D</sub>	300(DIP)/180(MFP)	mW
Operating Temperature Range	T <sub>A</sub>	-40 ~ 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temp./Time	T <sub>sol</sub>	260°C · 10sec	

### PIN ASSIGNMENT



### LOGIC DIAGRAM



### TRUTH TABLE

INPUTS			OUTPUTS	
CLOCK $\Delta$	D <sub>n</sub>	$\overline{\text{RESET}}$	Q <sub>n+1</sub>	$\overline{\text{Q}}_{n+1}$
$\downarrow$	H	H	H	L
$\downarrow$	L	H	L	H
$\downarrow$	*	H	Q <sub>n</sub> '	$\overline{\text{Q}}_{n}$ '
*	*	L	L	H

$\Delta$ : Level change

' : No change

\* : Don't care



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## RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V <sub>DD</sub>	3	-	18	V
Input Voltage	V <sub>IN</sub>	0	-	V <sub>DD</sub>	V

## STATIC ELECTRICAL CHARACTERISTICS (V<sub>SS</sub>=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	4.95	-	4.95	5.00	-	4.95	-	V	
			10	9.95	-	9.95	10.00	-	9.95	-		
			15	14.95	-	14.95	15.00	-	14.95	-		
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OUT</sub>   < 1μA V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-	0.05	-	0.00	0.05	-	0.05	V	
			10	-	0.05	-	0.00	0.05	-	0.05		
			15	-	0.05	-	0.00	0.05	-	0.05		
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> =4.6V V <sub>OH</sub> =2.5V V <sub>OH</sub> =9.5V V <sub>OH</sub> =13.5V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA	
			5	-2.5	-	-2.1	-4.0	-	-1.7	-		
			10	-1.5	-	-1.3	-2.2	-	-1.1	-		
			15	-4.0	-	-3.4	-9.0	-	-2.8	-		
			5	0.61	-	0.51	1.5	-	0.42	-		
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> =0.4V V <sub>OL</sub> =0.5V V <sub>OL</sub> =1.5V V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub>	10	1.5	-	1.3	3.8	-	1.1	-		
			15	4.0	-	3.4	15.0	-	2.8	-		
			5	3.5	-	3.5	2.75	-	3.5	-		
			10	7.0	-	7.0	5.5	-	7.0	-		
Input High Voltage	V <sub>IH</sub>	V <sub>OUT</sub> =0.5V, 4.5V V <sub>OUT</sub> =1.0V, 9.0V V <sub>OUT</sub> =1.5V, 13.5V  I <sub>OUT</sub>   < 1μA	15	11.0	-	11.0	8.25	-	11.0	-		
			5	-	1.5	-	2.25	1.5	-	1.5		
			10	-	3.0	-	4.5	3.0	-	3.0		
Input Low Voltage	V <sub>IL</sub>	V <sub>OUT</sub> =0.5V, 4.5V V <sub>OUT</sub> =1.0V, 9.0V V <sub>OUT</sub> =1.5V, 13.5V  I <sub>OUT</sub>   < 1μA	15	-	4.0	-	6.75	4.0	-	4.0		
			5	-	1.5	-	2.25	1.5	-	1.5		
			10	-	3.0	-	4.5	3.0	-	3.0		
			15	-	4.0	-	6.75	4.0	-	4.0		
Input Current	"H" Level	I <sub>IH</sub>	V <sub>IH</sub> =18V	18	-	0.1	-	10 <sup>-5</sup>	0.1	-	1.0	μA
	"L" Level	I <sub>IL</sub>	V <sub>IL</sub> =0V	18	-	-0.1	-	-10 <sup>-5</sup>	-0.1	-	-1.0	

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### STATIC ELECTRICAL CHARACTERISTICS ( $V_{SS}=0V$ )

CHARACTERISTIC	SYM-BOL	TEST CONDITION	$V_{DD}$ (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	$I_{DD}$	$V_{IN}=V_{SS}, V_{DD}$ *	5	-	1	-	0.005	1	-	30	A
			10	-	2	-	0.010	2	-	60	
			15	-	4	-	0.015	4	-	120	

\* All valid input combinations.

### DYNAMIC ELECTRICAL CHARACTERISTICS ( $T_a=25^\circ C$ , $V_{SS}=0V$ , $C_L=50pF$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{DD}$ (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	$t_{TLH}$		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	$t_{THL}$		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$		5	-	170	340	ns
			10	-	70	140	
			15	-	50	100	
Propagation Delay Time (RESET - Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$		5	-	190	380	ns
			10	-	80	160	
			15	-	55	110	
Min. Clock Pulse Width	$t_w$		5	-	55	130	ns
			10	-	20	60	
			15	-	15	40	
Min. Pulse Width (RESET)	$t_{WL}$		5	-	40	100	ns
			10	-	20	50	
			15	-	15	40	
Max. Clock Frequency	$f_{CL}$		5	3.5	9	-	MHz
			10	6	25	-	
			15	8	34	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	$t_{rCL}$ $t_{fCL}$		5	20	-	-	$\mu s$
			10	15	-	-	
			15	15	-	-	

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DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V<sub>SS</sub>=0V, C<sub>L</sub>=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	MIN.	TYP.	MAX.	UNIT
Min. Set-up Time (DATA - CLOCK)	t <sub>SU</sub>		5	-	30	60	ns
			10	-	15	30	
			15	-	10	20	
Min. Hold Time (DATA - CLOCK)	t <sub>H</sub>		5	-	-5	80	ns
			10	-	0	40	
			15	-	3	30	
Min. Removal Time (RESET - CLOCK)	t <sub>rem</sub>		5	-	7	40	ns
			10	-	4	20	
			15	-	3	15	
Input Capacitance	C <sub>IN</sub>			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

