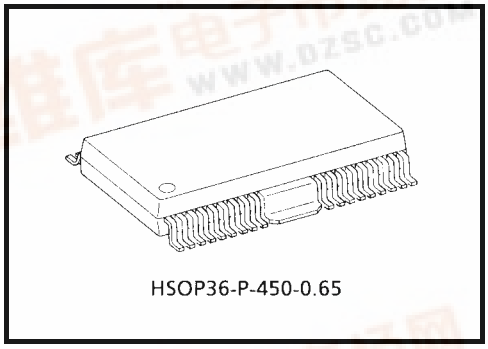
TOSHIBA BiCD IC Silicon Monolithic

TB62300FG

Dual Full-Bridge Driver for DC Motor

The TB62300FG is a dual brushed DC motors driver IC employing a chopper-based forward/reverse full-bridge mechanism. It controls two brushed DC motors at high precision. The motor supply voltage is up to 40 V and the V_{DD} supply voltage is 5.0 V.



HSOP36-P-450-0.65

Weight: 0.79 g (typ.)

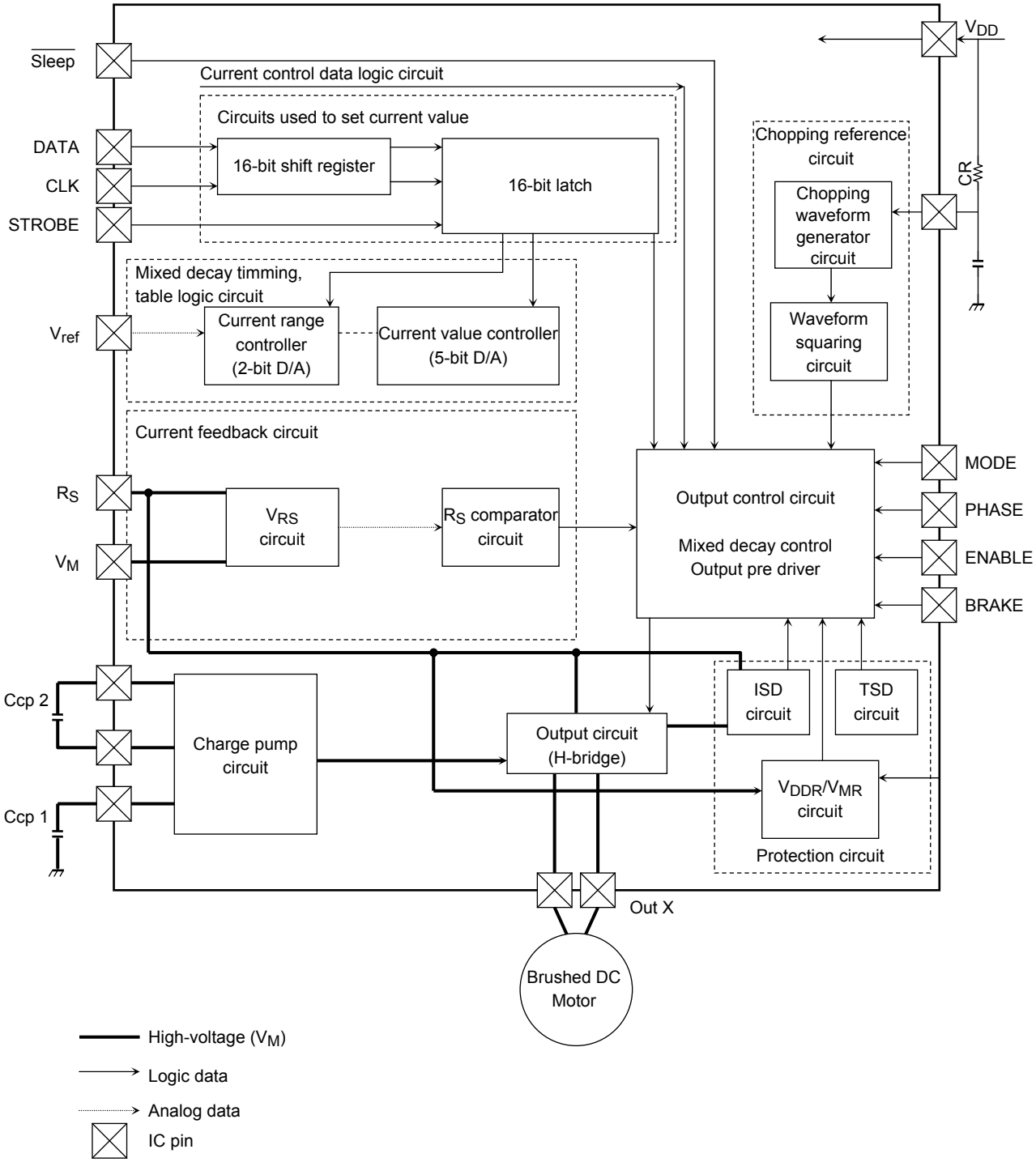
Features

- A single IC can drive two brushed DC motors.
- Monolithic Bi-CMOS IC
- Low ON-resistance (R_{on}) = 0.3 Ω (T_j = 25°C at 2.0 A typ.)
- Selectable current control: PWM current control using the PHASE pin or serial control
- 5-bit DA converter for specifying current value and 2-bit DA converter for determining torque
- MIXED DECAY mode enables specification of current decay rate in four steps.
- Self-oscillation chopping frequency with external resistor and capacitor
- High-speed chopping at 100 kHz or higher
- ISD, TSD, and POR (V_{DD}/V_M) protection circuits
- Charge pump circuit (two external capacitors) for driving output
- 36-pin package: HSOP36 with heat sink
- Output voltage: 40 V (max)
- Output current: 2.5 A max (in steady-state phase) or 8 A max (pulsed output)

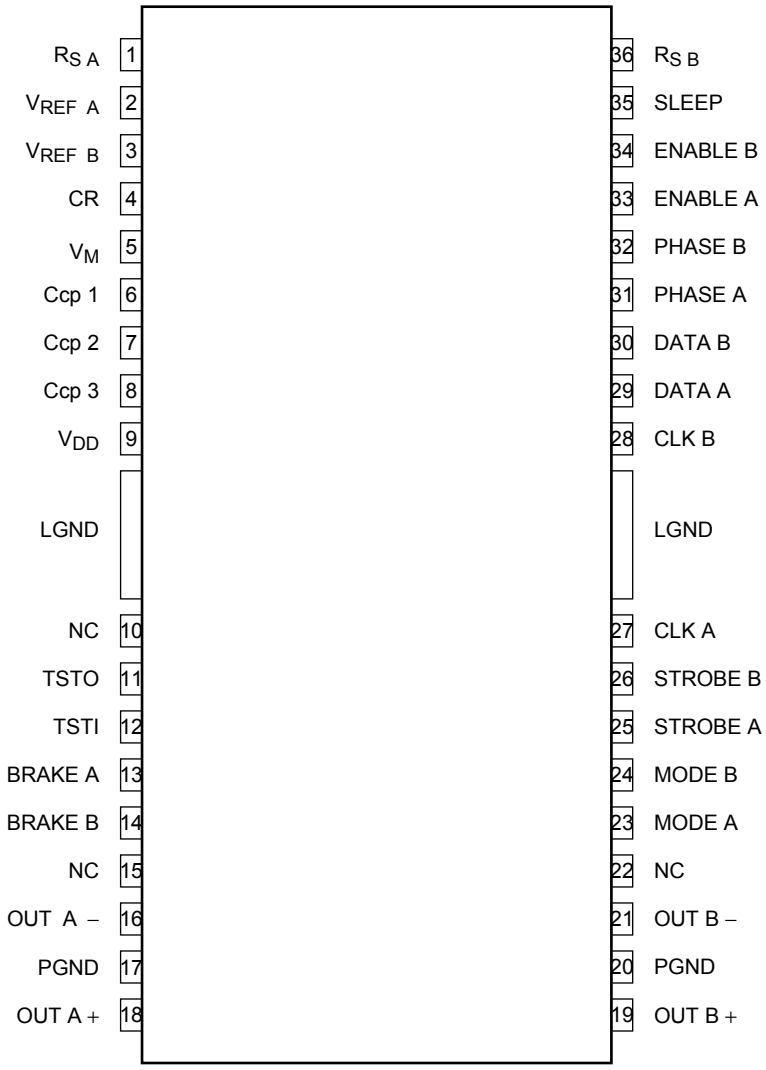
Note: The values specified in this document are designed values, which are not guaranteed.

Block Diagram

1. Overview (for single axis)



Pin Assignment



Note: When designing a ground line, make sure that all ground pins are connected to the same ground trail and remember to take heat radiation into account.
When pins that are used to toggle between modes are controlled by a switch, pull up or down the pins to avoid high impedance.
The IC may be destroyed due to short circuit between outputs, to supply, or to ground. Design output lines, V_{DD} (V_M) lines and ground lines with great care.
When power supply pins (V_M, R_S, OUT, P-GND, V_{SS} and C_{CP}) that are exposed to high current, or logic input pins are not connected correctly, excessive current or malfunction may cause the IC to break down.

Pin Description

Pin Number	Symbol	Function	Remarks
1	$R_{S\ A}$	A-ch output power supply pin (current detection pin)	Reference pin for A-axis supply voltage
2	$V_{REF\ A}$	A-ch reference voltage input pin	Reference power supply pin for A-axis current
3	$V_{REF\ B}$	B-ch reference voltage input pin	Reference power supply pin for B-axis current
4	CR	External chopping reference pin	Pin used to set the chopping frequency
5	V_M	Supply voltage monitor pin	Monitor (reference) pin for motor supply voltage
6	Ccp 1	Charge pump capacitor pin	Pin for connecting a charge pump capacitor
7	Ccp 2	Charge pump capacitor pin	Pin for connecting a charge pump capacitor
8	Ccp 3	Charge pump capacitor pin	Pin for connecting a charge pump capacitor
9	V_{DD}	Logic power supply	Logic supply current input pin
10	NC	NC pin	Note: Usually, leave this pin open.
11	TSTO	Test pin (usually not used)	Note: Usually, leave this pin open.
12	TSTI	Test pin (usually not used)	Note: Usually, connect this pin to LGND.
13	BRAKE A	A-ch brake mode pin	Forced brake mode
14	BRAKE B	B-ch brake mode pin	Forced brake mode
15	NC	NC pin	Note: Usually, leave this pin open.
16	OUT A –	A-ch negative output pin	A – output pin
17	PGND	V_M ground	Power ground
18	OUT A +	A-ch positive output pin	A + output pin
19	OUT B +	B-ch positive output pin	B + output pin
20	PGND	V_M ground	Power ground
21	OUT B –	B-ch negative output pin	B – output pin
22	NC	NC pin	Note: Usually, leave this pin open.
23	MODE A	A-ch data mode switching pin	Pin used to toggle between serial input and PWM control
24	MODE B	B-ch data mode switching pin	Pin used to toggle between serial input and PWM control
25	STROBE A	A-ch latch signal input pin	Data input: latched on rising edge
26	STROBE B	B-ch latch signal input pin	Data input: latched on rising edge
27	CLK A	A-ch clock input pin	Data input: referred to rising edge
28	CLK B	B-ch clock input pin	Data input: referred to rising edge
29	DATA A	A-ch data input pin	Data input:
30	DATA B	B-ch data input pin	Data input:
31	PHASE A	A-ch phase switching pin	PWM signal input pin:
32	PHASE B	B-ch phase switching pin	PWM signal input pin::
33	ENABLE A	A-ch output forced OFF pin	L: output stopped
34	ENABLE B	B-ch output forced OFF pin	L: output stopped
35	SLEEP	Operation stopped mode	Internal logic cleared and charge pump stopped
36	$R_{S\ B}$	B-ch output power supply pin (current detection pin)	Reference pin for B-axis supply voltage
FIN1	LGND	Logic ground	Logic ground
FIN2	LGND	Logic ground	Logic ground

Pin Description (Supplementary)

Pull-up/pull-down status and operation within the IC for input pins

Pin Number	Symbol	Internal Pull-up/down	Output Operation at High	Output Operation at Low
10	NC	Open	Does not affect normal operation of the IC.	Does not affect normal operation of the IC.
11	TSTO	Output pin (usually low)	Does not affect normal operation of the IC (with the same withstand voltage as for V_{DD}).	Does not affect normal operation of the IC.
12	TSTI	Input pin (no pull-up or down)	Toshiba test mode	Normal operation mode
13	BRAKE A	No pull-up or down		
14	BRAKE B	No pull-up or down		
15	NC	Open	Does not affect normal operation of the IC.	Does not affect normal operation of the IC.
22	NC	Open	Does not affect normal operation of the IC.	Does not affect normal operation of the IC.
23	MODE A	No pull-up or down		
24	MODE B	No pull-up or down		
25	STROBE A	No pull-up or down		
26	STROBE B	No pull-up or down		
27	CLK A	No pull-up or down		
28	CLK B	No pull-up or down		
29	DATA A	No pull-up or down		
30	DATA B	No pull-up or down		
31	PHASE A	No pull-up or down		
32	PHASE B	No pull-up or down		
33	ENABLE A	No pull-up or down		
34	ENABLE B	No pull-up or down		
35	SLEEP	Pull-down with a 50-kΩ resistor		

Truth Table (1)

Pin logic overview

Pin Number	Symbol	Function	Logic
23	MODE A	A-ch data mode switching pin	H : Serial signal input control L : PWM control Note: When PWM control is selected, serial data bits D0 to D6 are valid while D7 to D13 are invalid.
24	MODE B	B-ch data mode switching pin	
25	STROBE A	A-ch latch signal input pin	H : Latched on rising edge
26	STROBE B	B-ch latch signal input pin	L : Pass-through
31	PHASE A	A-ch phase switching pin	H : Positive phase
32	PHASE B	B-ch phase switching pin	L : Negative phase
35	SLEEP	Operation stopped mode	H : Sleep released L : Sleep state All internal circuits, including charge pumps, are stopped.
33	ENABLE A	A-ch output forced OFF pin	H : Output enabled Output transistors turned on
34	ENABLE B	B-ch output forced OFF pin	L : Output disabled Output transistors turned off
13	BRAKE A	A-ch brake mode pin	H : Brake applied PHASE and ENABLE pins disabled
14	BRAKE B	B-ch brake mode pin	L : Brake released

Truth Table (2)

Overall logic

External Pins					Serial	Status
SLEEP	ENABLE A/B	BRAKE A/B	MODE A/B	PHASE A/B	PHASE	
0	X	X	X	X	X	Sleep mode
1	0	X	X	X	X	Disable mode
	1	1	X	X	X	Breake ON
		0	0	1	X	Forward
			0	0	X	Reverse
			1	X	1	Forward
			1	X	0	Reverse

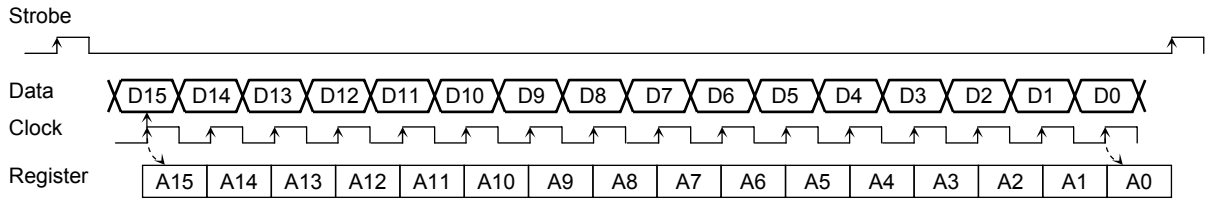
IC State for Each Function

Function	Internal Logic	Output	Charge Pump	OSC	Recovery Time
SLEEP	Reset	OFF	OFF	OFF	t_{ONG} = 2.0 ms (typ.)/4.0 ms (max)
ENABLE	Maintained	OFF	Operating	Operating	N/A
POR	Reset	OFF	OFF	OFF	t_{ONG} = 2.0 ms (typ.)/4.0 ms (max)
ISD	Reset	OFF	OFF	OFF	t_{ONG} = 2.0 ms (typ.)/4.0 ms (max)
TSD	Reset	OFF	OFF	OFF	t_{ONG} = 2.0 ms (typ.)/4.0 ms (max)

Serial Input Signals

Order of data input

Data Bit	Name	Function	Initial Value	Initial State	When PWM is Operating
0	TBlank 0	Set blanking time to prevent false detection due to noise	0	1 ÷ fchop ÷ 16 × 7	Enabled
1	TBlank 1		1		
2	TBlank 2		1		
3	Torque 0	Set current range	0	25%	Enabled
4	Torque 1		0		
5	Decay mode 0	Set decay mode	1	Mixed decay mode (37.5%)	Enabled
6	Decay mode 1		0		
7	Current 0	Set current	1	100%	Disabled
8	Current 1		1		
9	Current 2		1		
10	Current 3		1		
11	Current 4		1		
12	Phase	Switch phase	0	Negative	Disabled
13	—	—	—	—	—
14	—	—	—	—	—
15	—	—	—	—	—



Notes on TBlank Setting

When using PWM control and serial control simultaneously, constant-current chopping may be disabled depending on the TBlank setting. Using constant-current chopping requires the following phase width in Fast Decay mode:

(TBlank setting + 2/fcr) × 2

Setting Table (1): D0, D1, D2

Blanking time settings

Data Bit	Name	Function	TBlank 2	TBlank 1	TBlank 0	Setting TBlank (typ.)
0	TBlank 0	Set blanking time to prevent false detection due to noise	0	0	0	$1 \div f_{Chop} \div 16 \times 1$
1	TBlank 1		0	0	1	$1 \div f_{Chop} \div 16 \times 2$
2	TBlank 2		0	1	0	$1 \div f_{Chop} \div 16 \times 3$
			0	1	1	$1 \div f_{Chop} \div 16 \times 4$
			1	0	0	$1 \div f_{Chop} \div 16 \times 5$
			1	0	1	$1 \div f_{Chop} \div 16 \times 6$
			1	1	0	$1 \div f_{Chop} \div 16 \times 7$
			1	1	1	$1 \div f_{Chop} \div 16 \times 8$

Setting Table (2): D3, D4

Torque settings

Data Bit	Name	Function	Torque 1	Torque 0	Setting Torque (typ.)
3	Torque 0	Set current range	0	0	25%
4	Torque 1		0	1	50%
			1	0	75%
			1	1	100%

Setting Table (3): D5, D6

Decay mode settings

Data Bit	Name	Function	Torque Mode 1	Torque Mode 0	Setting Decay Mode
5	Decay mode 0	Set decay mode	0	0	Slow decay mode
6	Decay mode 1		0	1	Mixed decay mode: 37.5%
			1	0	Mixed decay mode: 75.0%
			1	1	Fast decay mode

Setting Table (4): D7, D8, D9, D10, D11

Current settings

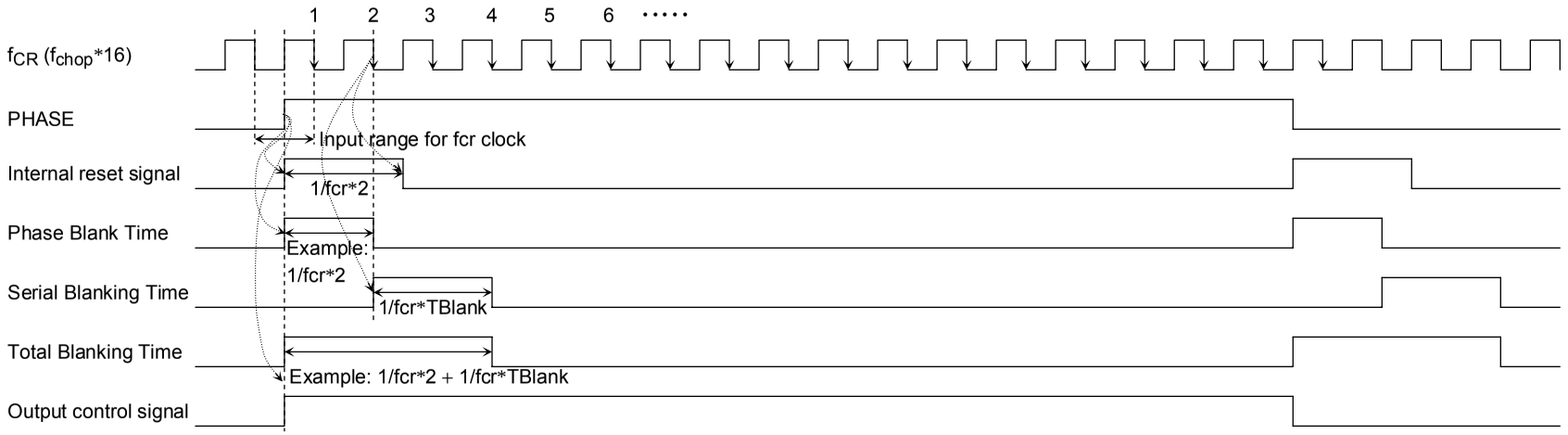
Data Bit	Name	Function	Current 4	Current 3	Current 2	Current 1	Current 0	Setting Current
7	Current 0	Set current	0	0	0	0	0	0%
8	Current 1		0	0	0	0	1	3%
9	Current 2		0	0	0	1	0	6%
10	Current 3		0	0	0	1	1	9%
11	Current 4		0	0	1	0	0	12%
			0	0	1	0	1	16%
			0	0	1	1	0	19%
			0	0	1	1	1	22%
			0	1	0	0	0	25%
			0	1	0	0	1	29%
			0	1	0	1	0	32%
			0	1	0	1	1	35%
			0	1	1	0	0	38%
			0	1	1	0	1	41%
			0	1	1	1	0	45%
			0	1	1	1	1	48%
			1	0	0	0	0	51%
			1	0	0	0	1	54%
			1	0	0	1	0	58%
			1	0	0	1	1	61%
			1	0	1	0	0	64%
			1	0	1	0	1	67%
			1	0	1	1	0	70%
			1	0	1	1	1	74%
			1	1	0	0	0	77%
			1	1	0	0	1	80%
			1	1	0	1	0	83%
			1	1	0	1	1	87%
			1	1	1	0	0	90%
			1	1	1	0	1	93%
			1	1	1	1	0	96%
			1	1	1	1	1	100%

Setting Table (5): D12

Phase settings

Data Bit	Name	Function	Phase	Setting Phase
12	Phase	Switch phase	0	Negative
			1	Positive

PWM Operation



Notes: ・f_{cr} is 16 times the f_{chop} frequency.
・PHASE is an external signal.
・The internal reset signal resets the internal clocks and counters.
・Phase Blank Time is time between either edge of the external PHASE signal and the leading edge of serial blanking time.

Description

The output H bridge is driven by an external PHASE signal.
It, however, also uses the fcr signal, generated with external CR, to generate blanking time and Mixed Decay time. The above logic is configured to handle the two signals, PHASE and fcr, which are asynchronous to each other. The logic generates internal reset signal edges from external PHASE edges, resulting in the width equal to two fcr cycles.
The fcr-based counter assumes the first fcr falling edge following the PHASE edge as the first count. The maximum phase difference between the PHASE and fcr signals is, therefore, one fcr cycle.

The serial blanking time starts at the second count based on the fcr clock (The first three samples of serial blanking time signal must be 000).
The last stage output is switched by the edge of the external PHASE signal. That means there is an interval of two fcr cycles before the set blanking time starts.
To cover the interval, the logic generates the time between the PHASE signal edge and blanking time start as phase blank time, during which comparison is masked off in the same way as in blanking time.
Consequently, the blanking time as viewed from outside the IC is within the range from one fcr cycle (TBlank (000)) to eight fcr cycles (TBlank (111)) + I phase difference between PHASE and fcr (up to two fcr cycles).

Absolute Maximum Ratings (T_{opr} = 25°C)

Characteristics	Symbol	Test Condition	Rating	Unit
Logic supply voltage	V_{DD}	—	−0.4 to 7.0	V
Maximum output voltage	V_M	—	40	V
Peak output current (Note: preliminary specification)	$I_{OUT\ (Peak)}$	$t_W \leq 500$ ns	8.0	A
Continuous output current	$I_{OUT\ (Cont)}$	—	2.5	A
Logic input voltage	V_{IN}	—	−0.5 to V_{DD}	V
Current detection pin voltage	V_{RS}	—	$V_M \pm 4.5$ V	V
Power dissipation	P_D	IC alone	1.4	W
		When mounted on a board (Note)	3.2	W
Operating temperature	T_{opr}	—	−40 to 85	°C
Storage temperature	T_{stg}	—	−55 to 150	°C
Junction temperature	T_j	—	150	°C

Note: When T_{opr} = 45°C, T_j = 150°C and θja = 32°C

Recommended Operating Conditions (T_{opr} = 0 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply voltage (Note 1)	V_{DD}	—	4.5	5.0	5.5	V
Output voltage (Note 1)	V_M	V_{DD} = 5.0 V	18.0	24.0	33.0	V
Output current (Note: preliminary specification)	$I_{OUT\ (Peak)}$	V_M = 33.0 V, $t_w \leq 500$ ns	—	6.4	7.2	A
	$I_{OUT\ (Cont)}$	V_M = 33.0 V	—	1.5	1.8	A
Logic input voltage range	V_{IN}	—	0	—	V_{DD}	V
Clock frequency	f_{CLK}	V_{DD} = 5.0 V	1.0		25.0	MHz
Chopping frequency	f_{chop}	V_{DD} = 5.0 V	20	30	150	kHz
V_{ref} reference voltage	V_{ref}	V_M = 24.0 V, T_{ORQUE} = 100%	2.0	3.0	V_{DD}	V
Current detection pin voltage	V_{RS}	V_{DD} = 5.0 V	0	±1.0	±1.5	V
Junction temperature	T_j	—	—	—	120	°C
Oscillator capacitor	C_{OSC}	—	—	270	—	pF
Oscillator resistor	R_{OSC}	—	—	3.9	—	kΩ
Charge pump capacitor A	C_{CPA}	—	—	0.22	—	μF
Charge pump capacitor B	C_{CPB}	—	—	0.022	—	μF
Input rise and fall rate (Note 2)	tri/tfi	—	—	0.1	5.0	μs

Note 1: Do not reduce V_{DD} to 0 V (ground) while V_M voltage is applied. Such an attempt may damage the IC because there is a current path from the V_M pin to V_{DD} pin and the internal logic is undefined when V_{DD} is not applied. Leaving V_{DD} open (Hi-Z) is less likely to damage the IC, although it is not recommended.

Note 2: The circuit configuration of this IC cannot handle extremely slow data input (on pins BREAK A, BREAK B, SLEEP, ENABLE A, ENABLE B, PHASE A, PHASE B, DATA A, DATA B, CLK A, CLK B, STROBE A, STROBE B, MODE A, and MODE B). Applying a slow signal having a period longer than 5 μs may cause the IC to oscillate.

(1) Calculating the current
$I_{OUT} = 1/3 \times V_{ref}$ (V) × (Torque (%) ÷ R_{RS} (Ω)) × Current (%)
where 1/3 is the V_{ref} (GAIN):V_{ref} attenuation ratio.

(2) Calculating the oscillation frequency
$f_{CR} = 1/(KA) \times (C \times R + KB \times C)) \times$ [Hz]
KA = 0.523, KB = 600, $f_{chop} = f_{CR}/16$ [Hz]

[Example] When C_{OSC} = 270 pF and R_{OSC} = 3.9 kΩ: f_{CR} = 1.57 MHz and f_{chop} = 1.57/16 = 98.4 kHz

Electrical Characteristics 1

DC Characteristics (unless otherwise specified, V_M = 24 V, V_{DD} = 5.0 V, T_{opr} = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	V_{IH}	DC	CLK, STROBE, DATA, MODE, PHASE, ENABLE and PHASE pins	2.0	—	—	V
	Low	V_{IL}			—	—	0.8	
Input current		I_{IH1}	DC	CLK, STROBE, DATA, MODE, PHASE, ENABLE and PHASE pins	—	—	1.0	μA
		I_{IL1}			—	—	1.0	
		I_{IH2}		SLEEP pin	—	—	200.0	μA
		I_{IL2}			—	—	1.0	
Current consumed by logic power supply		I_{DD1}	DC	V_{DD} = 5.0 V, fcr stopped	—	3.0	4.5	mA
		I_{DD2}		In SLEEP mode		0.3	1.0	
V_M current consumption		I_{M1}	DC	Output open, f_{CLK} = 1 kHz, logic operating, V_{DD} = 5 V, V_M = 24 V, all output stages stopped, charge pump charged	—	4.3	7.0	mA
		I_{M2}		Output open, f_{CLK} = 4 kHz, internal logic operating (100-kHz chopping), output stages operating without load, charge pump charged	—	20.0	28.0	
		I_{M3}		In SLEEP mode	—	0.5	1.0	
Output standby current	Upper	I_{OH}	DC	V_{RS} = V_M = 24 V, V_{out} = 0 V, ENABLE = Low, DATA = All low	–400	—	—	μA
Output bias current	Upper	I_{OB}		V_{RS} = V_M = 24 V, V_{out} = 24 V, ENABLE = Low, DATA = All low	–200	—	—	
Output leakage current	Lower	I_{OL}		V_{RS} = V_M = Ccp A = V_{out} = 24 V, SLEEP= Low	—	—	1.0	
Comparator reference voltage ratio	High	$V_{RS\ (H)}$	DC	V_{ref} = 3.0 V, V_{ref} (gain) = 1/3.0 TORQUE = 11 = 100% set	—	100	—	%
	Mid High	$V_{RS\ (MH)}$		V_{ref} = 3.0 V, V_{ref} (gain) = 1/3.0 TORQUE = 10 = 75% set	73	75	77	
	Mid Low	$V_{RS\ (ML)}$		V_{ref} = 3.0 V, V_{ref} (gain) = 1/3.0 TORQUE = 01 = 50% set	48	50	52	
	Low	$V_{RS\ (L)}$		V_{ref} = 3.0 V, V_{ref} (gain) = 1/3.0 TORQUE = 00 = 25% set	23	25	27	

Electrical Characteristics 2

DC Characteristics (unless otherwise specified, V_M = 24 V, V_{DD} = 5.0 V, T_{opr} = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current interchannel error	ΔI_{OUT1}	DC	Error in output current between channels (I_{OUT} = 1.5 A)	−5.0	—	5.0	%
Output current setting error	ΔI_{OUT2}	DC	I_{OUT} = 1.5 A	−5.0	—	5.0	%
RS pin current	I_{RS}	DC					μA
Output transistor drain-source ON-resistance	RON1	DC	I_{OUT} = 1.5 A, V_{DD} = 5.0 V, T_j = 25 °C, forward direction	—	0.3	0.4	Ω
	RON1		I_{OUT} = 1.5 A, V_{DD} = 5.0 V, T_j = 25 °C, reverse direction	—	0.3	0.4	
	RON2		I_{OUT} = 1.5 A, V_{DD} = 5.0 V, T_j = 105 °C, forward direction	—	0.4	0.55	
	RON2		I_{OUT} = 1.5 A, V_{DD} = 5.0 V, T_j = 105 °C, reverse direction	—	0.4	0.55	
V_{REF} input voltage	V_{ref}	DC	V_M = 24 V, V_{DD} = 5.0 V, ENABLE, output operation	2.0	—	V_{DD}	V
V_{REF} input current	I_{ref}	DC	V_{ref} = 3.0 V, V_M = 24 V, V_{DD} = 5.0 V, SLEEP	—	—	100	μA
V_{REF} attenuation ratio	V_{ref} (GAIN)	DC	V_{ref} = 3.0 V, V_M = 24 V, V_{DD} = 5.0 V, SLEEP	1/2.82	1/3	1/3.18	—
TSD operating temperature (Note 1)	T_jTSD	DC	V_{DD} = 5 V, V_M = 24 V	130	—	170	°C
Overcurrent protection circuit operating current	ISD	DC	V_{DD} = 5 V, V_M = 24 V	—	6.0	—	A
Output OFF mode supply voltage	Vpor (V_{DD})	DC	V_M = 24 V	—	3.0	—	V
	Vpor (V_M)	DC	V_{DD} = 5 V	—	15.0	—	

Note 1: Thermal shutdown (TSD) circuit

When the IC junction temperature reaches the specified value and the TSD circuit is activated, the internal reset circuit turns output off. The TSD activation temperature can be set within the range from 130°C (min) to 170°C (max). Once the TSD circuit is activated, output is stopped until a pulse (L to H to L) is subsequently applied to the SLEEP pin. The charge pump is halted while the TSD circuit is active.
The TSD circuit does not include hysteresis. Applying a pulse (L to H to L) to the SLEEP pin deactivates the circuit.

Note 2: Overcurrent protection circuit (ISD)

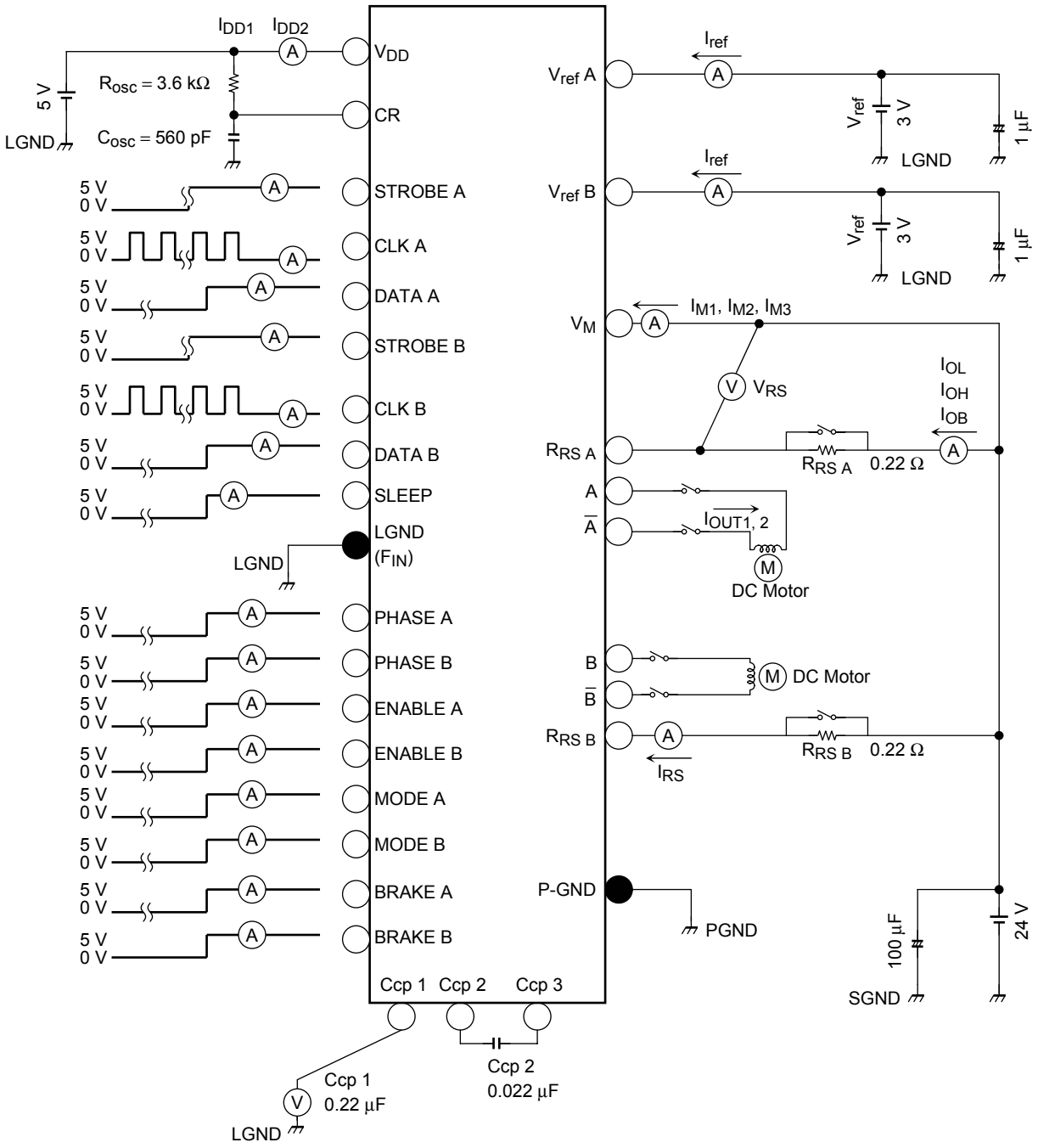
This circuit is activated when a current pulse exceeding the specified output value is applied for a period of $1/2f_{CHOP}$ (min) to f_{CHOP} (max).
The circuit activates the internal reset circuit to turn output off.
Once it is activated, output is stopped until a pulse (L to H to L) is subsequently applied to the SLEEP pin.
While the ISD circuit is active, the IC is placed in SLEEP mode with the charge pump halted.

AC Characteristics (T_{opr} = 25°C, V_M = 24 V, V_{DD} = 5 V with load of 6.8 mH/5.7 Ω)

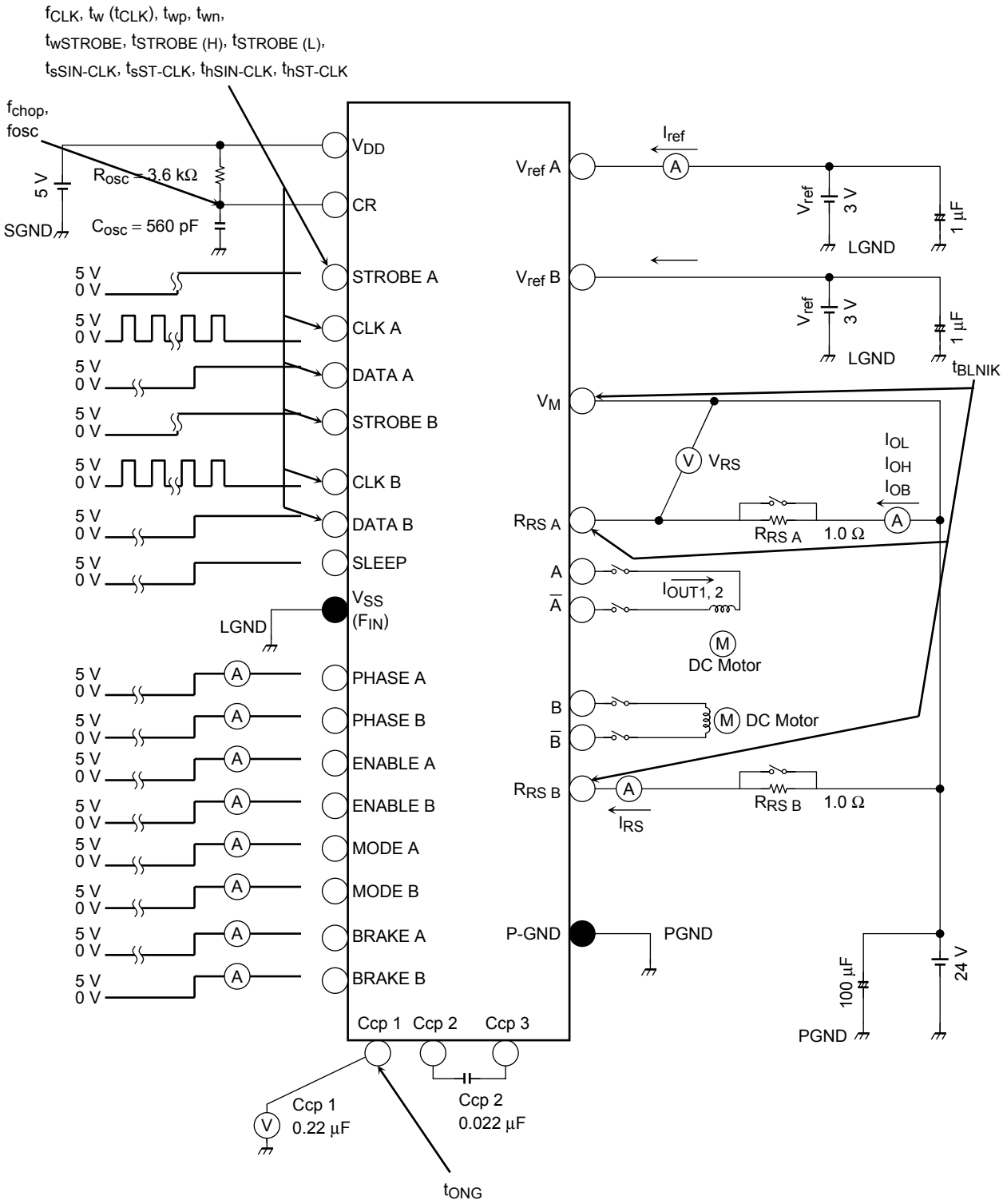
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock frequency	f_{CLK}	—		1.0	—	25.0	MHz
Minimum clock pulse width	t_w (t_{CLK})	AC		40.0	—	—	ns
	t_{wp}			20.0	—	—	
	t_{wn}			20.0	—	—	
Minimum STROBE pulse width	$t_{WSTROBE}$	AC		40.0	—	—	ns
	$t_{STROBE\ (H)}$			20.0	—	—	
	$t_{STROBE\ (L)}$			20.0	—	—	
Minimum SLEEP pulse width	$t_{WSTROBE}$	AC		t_{ONG}	—	—	ns
Phase difference between PHASE signal and fcr	tp	AC		—	—	$1/f_{CR}$	ns
Blanking time for preventing false detection	t_{BLNIK}		(Note 1)	—	300	—	ns
Data setup time	$t_{sSIN\text{-}CLK}$	AC		20.0	—	—	ns
	$t_{sST\text{-}CLK}$			20.0	—	—	
Data hold time	$t_{hSIN\text{-}CLK}$	AC		20.0	—	—	ns
	$t_{hST\text{-}CLK}$			20.0	—	—	
STROBE setup time (relative to CLK)	$t_{sSSB\text{-}CLK}$	AC		20.0	—	—	ns
STROBE hold time (relative to CLK)	$t_{hSB\text{-}CLK}$	AC		20.0	—	—	
Output transistor switching time	t_f	AC		—	40.0	100	ns
	t_f			—	40.0	100	
	t_{pLH}			—	100	200	
	t_{pHL}			—	580	1000	
	t_{pLZ}			—	100	200	
	t_{pHZ}			—	350	700	
	t_{pZL}			—	1000	2000	
	t_{pZH}			—	350	700	
CR reference signal oscillation frequency	f_{CR}		C_{osc} = 270 pF, R_{osc} = 3.9 kΩ	1.1	1.3	1.5	MHz
Chopping frequency	$f_{chop\ (min)}$ $f_{chop\ (typ.)}$ $f_{chop\ (max)}$			20.0	—	150.0	kHz
Oscillation frequency	f_{chop}		When f_{CR} = 480 kHz	—	30.0	—	kHz
Charge pump rise time	t_{ONG}	AC		—	2.0	4.0	ms

Note 1: The blanking time is internally fixed but it can be elongated by applying a serial blanking time signal.

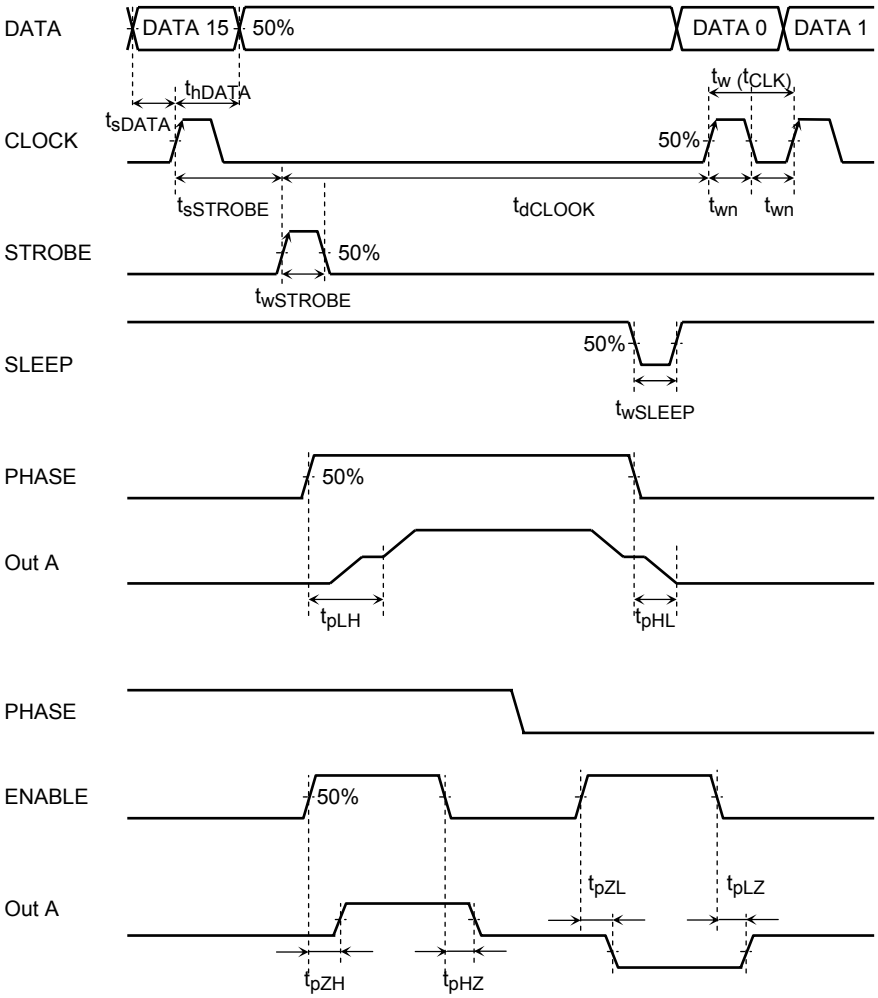
Test Circuit (DC)



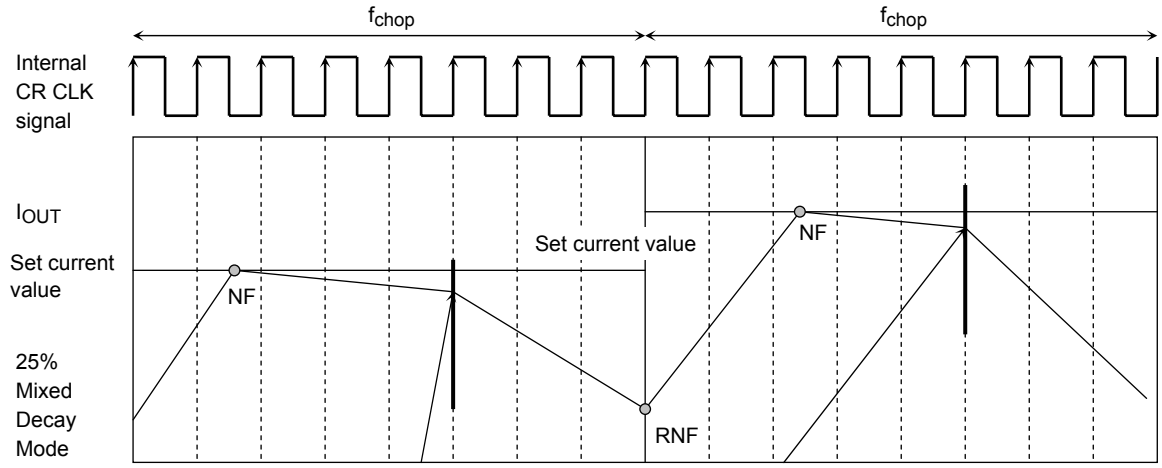
Test Circuit (AC)



AC Test Waveforms

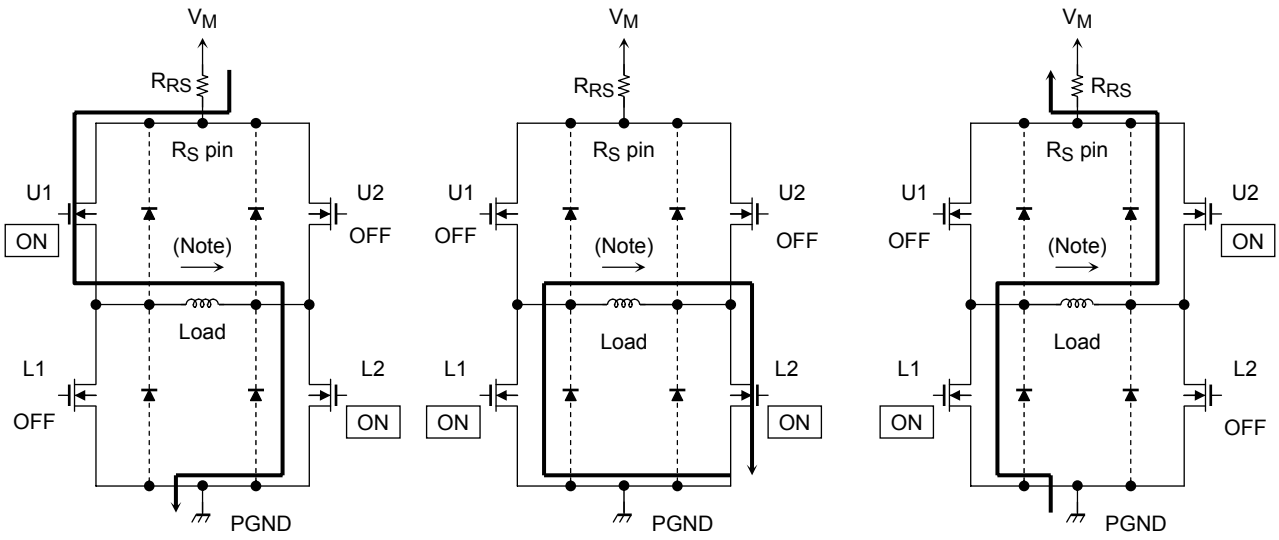


Waveform in Mixed Decay Mode (Current Waveform)



MDT (Mixed Decay Timming) point

Output Transistor Operating Mode



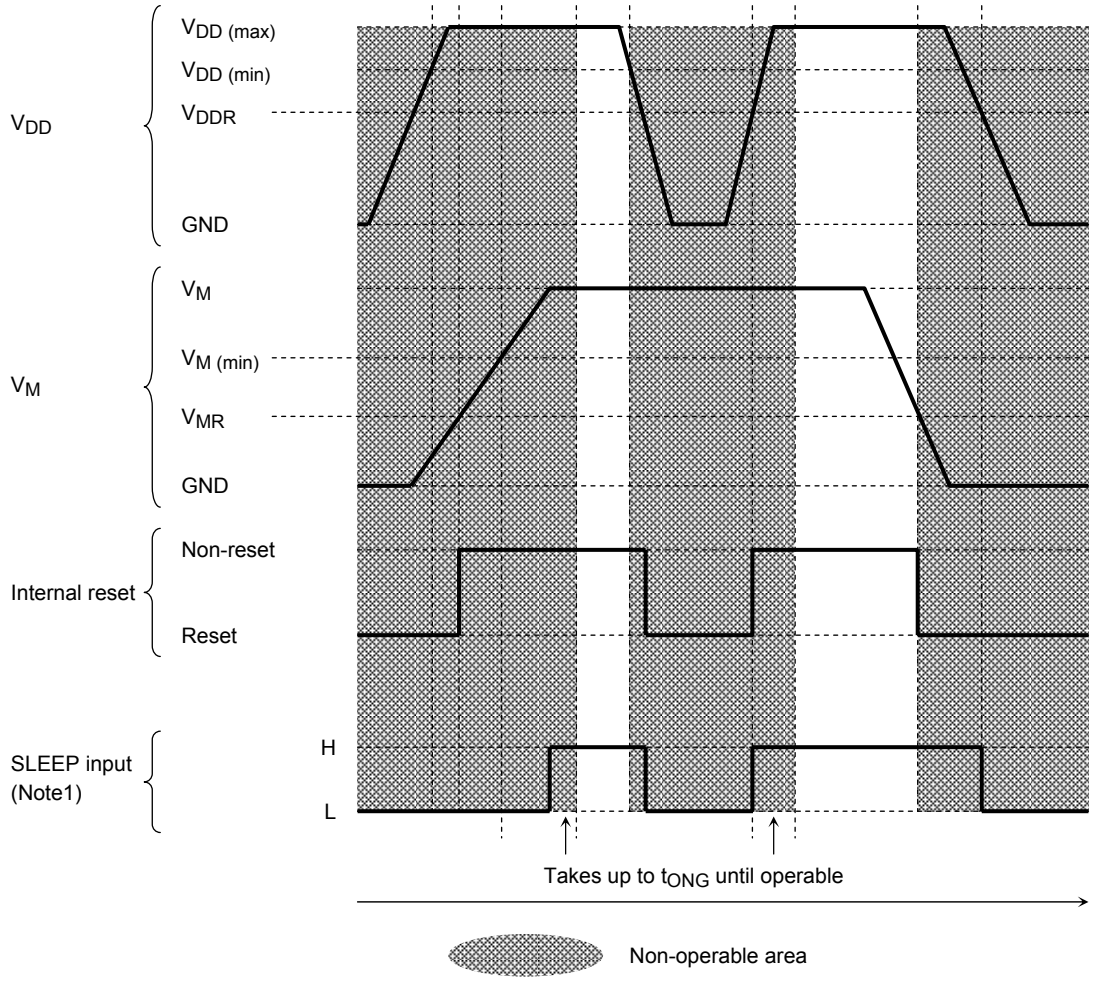
Output Transistor Operation Functions

CLK	U1	U2	L1	L2
Charge	ON	OFF	OFF	ON
Slow	OFF	OFF	ON	ON
Fast	OFF	ON	ON	OFF

Note: The above table is an example where current flows in the direction of the arrows in the above figures. When the current flows in the opposite direction of the arrows, see the table below.

CLK	U1	U2	L1	L2
Charge	OFF	ON	ON	OFF
Slow	OFF	OFF	ON	ON
Fast	ON	OFF	OFF	ON

Power Supply Sequence (Recommended)

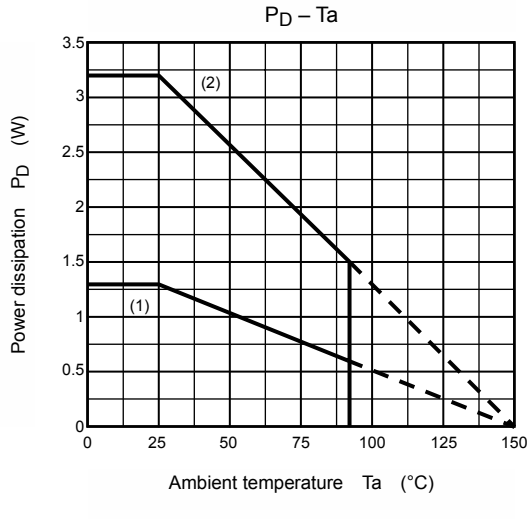


Note 1: If V_{DD} drops to the level of the V_{DDR} or below while the specified voltage is applied to the V_M pin, the IC is internally reset.
This is a protective measure against malfunction. Likewise, if V_M drops to the level of V_{MR} or below while regulation voltage is applied to V_{DD}, the IC is internally reset as a protective measure against malfunction.
To avoid malfunction, when turning on V_M or V_{DD}, applying a signal to the SLEEP pin at the above timing is recommended.
It takes time for the output control charge pump circuit to stabilize. Wait up to t_{ONG} time after power on before driving a motor.

Note 2: When the V_M value is between 3.3 to 5.5 V, the internal reset is released, thus output may be active. In such a case, the charge pump circuit cannot operate properly because of insufficient voltage. The IC should be held in SLEEP mode until V_M reaches 13 V or more.

Note 3: Since V_{DD} = 0 V and V_M = voltage within the rating are applied, output is turned off by internal reset.
At that time, a current of several mA flows due to a current path between V_M and V_{DD}.
When the output voltage is high, make sure that the specified voltage is applied to V_{DD}.

P_D – Ta (Package power dissipation)



Transient thermal resistance

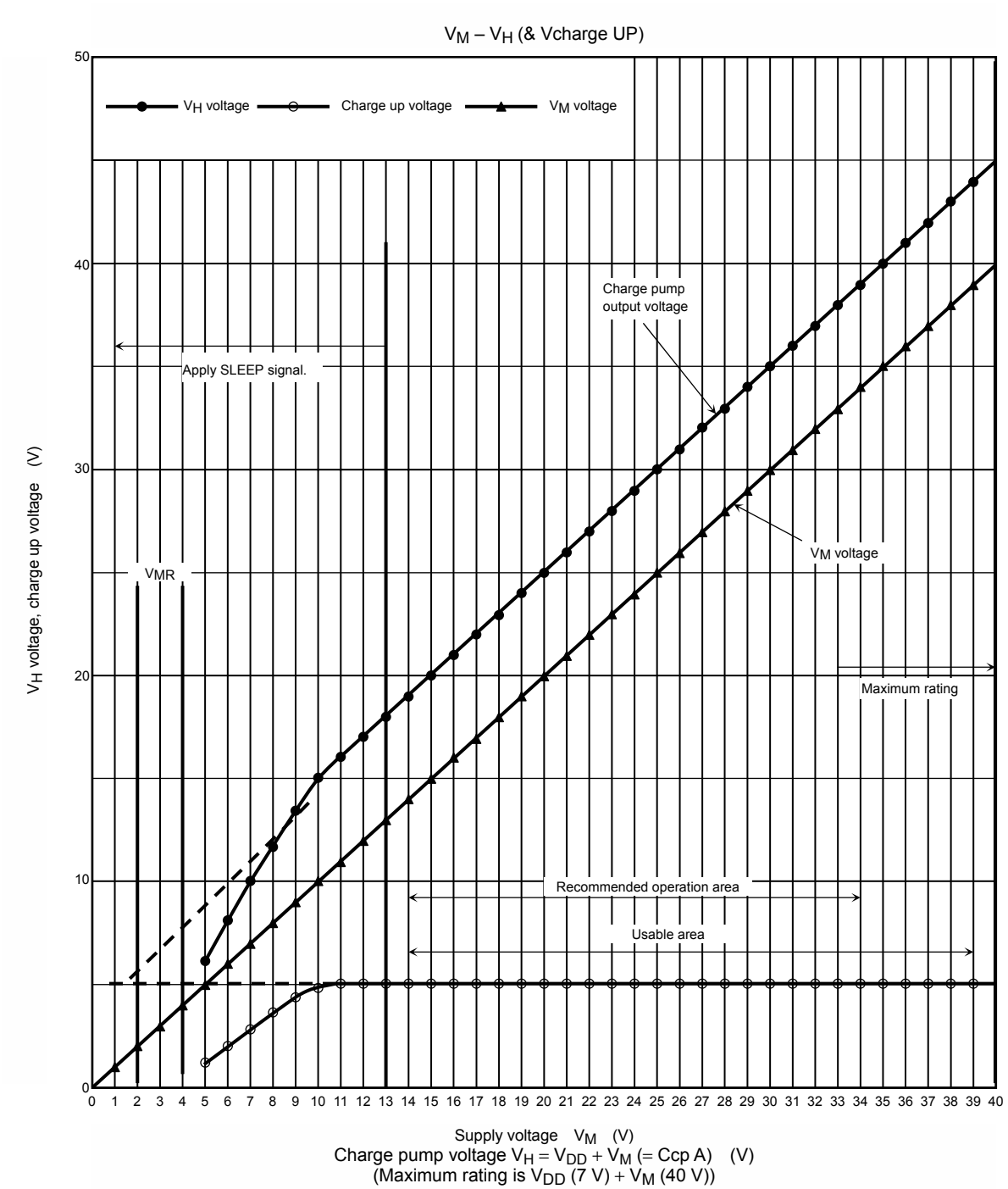
(1) HSOP36 $R_{th\ (j\text{-}a)}$ without a board (96°C/W)

(2) When mounted on a board (140 mm × 70 mm × 1.6 mm: 38°C/W: typ.)

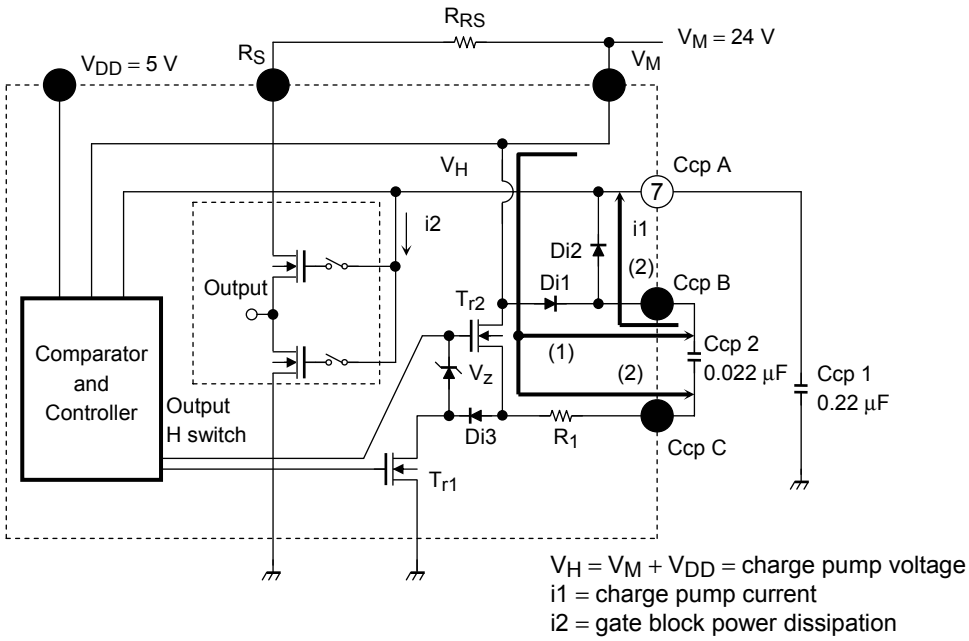
Note: $R_{th\ (j\text{-}a)}$: 8.5°C/W

Relationship between V_M and V_H (charge pump voltage)

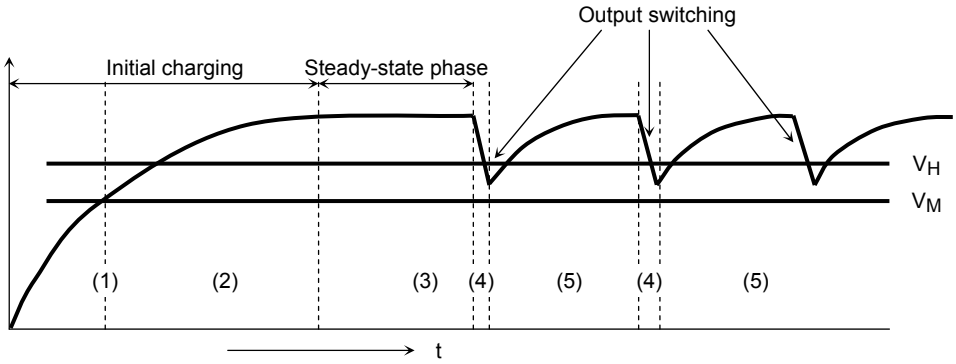
Note: V_{DD} = 5 V
Ccp 1 = 0.22 μF, Ccp 2 = 0.022 μF, f_{chop} = 150 kHz
(Care must be taken about the temperature charges of charge pump capacitor.)



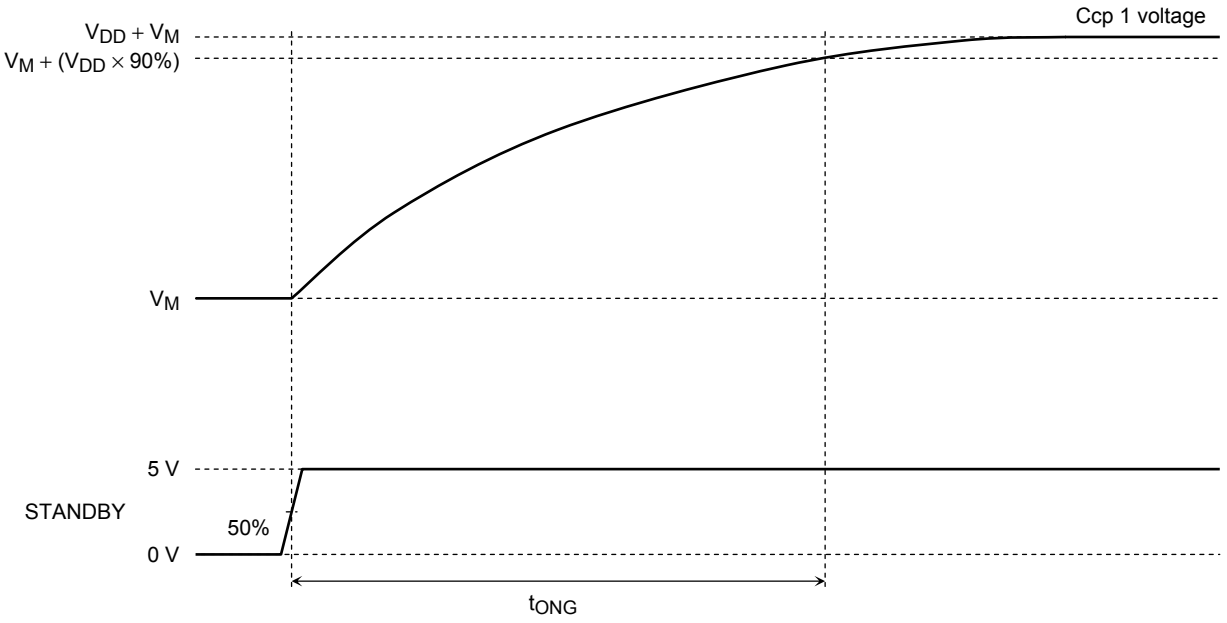
Operation of Charge Pump Circuit



- Initial charging
  - (1) When RESET is released, T_{r1} is turned on and T_{r2} turned off. Ccp 2 is charged from V_M via Di1.
  - (2) After T_{r1} is turned off and T_{r2} is turned on, and Ccp 1 is charged from Ccp 2 via Di2.
  - (3) When the voltage difference between V_M and V_H (Ccp A pin voltage = charge pump voltage) reaches V_{DD} or higher, operation halts (in the steady-state phase).
- Actual operation
  - (4) The charge of Ccp 1 charge is used at f_{chop} switching and the potential of V_H drops.
  - (5) The circuit is charged up by the operations of (1) and (2) above.



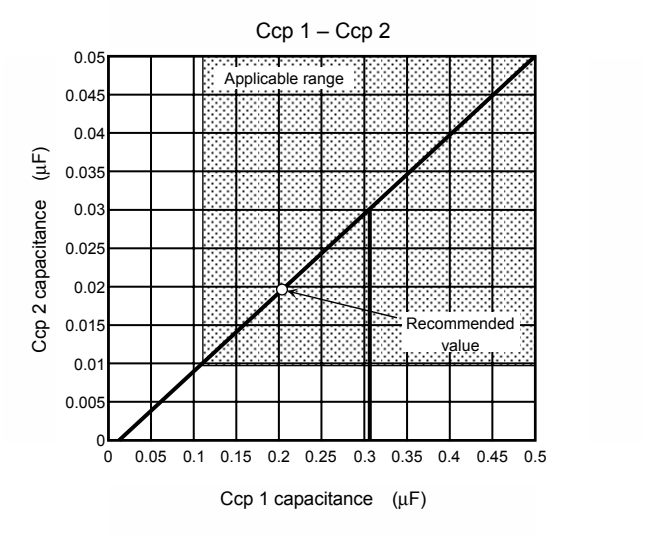
Charge Pump Rise Time



t_{ONG}: Time taken for capacitor Ccp 2 (charging capacitor) to fill up Ccp 1 (storing capacitor) to $V_M + V_{DD}$ after a reset is released.
The internal circuits cannot drive the gates correctly until the voltage of Ccp 1 reaches $V_M + V_{DD}$. Be sure to wait for t_{ONG} or longer before driving the motors.
Basically, the larger the Ccp 1 capacitance is, the smaller the voltage fluctuation is, though the initial charge up time is longer.
The smaller the Ccp 1 capacitance is, the shorter the initial charge-up time is, but the voltage fluctuation is larger.
Depending on the combination of capacitors (especially with small capacitance), voltage may not be sufficiently boosted. When the voltage does not increase sufficiently, R_{ON} of output DMOS becomes lower than the reference value, which raises the temperature.
Thus, use the capacitors under the capacitor combination conditions (Ccp 1 = 0.22 μF, Ccp 2 = 0.022 μF) recommended by Toshiba.

External Capacitor for Charge Pump

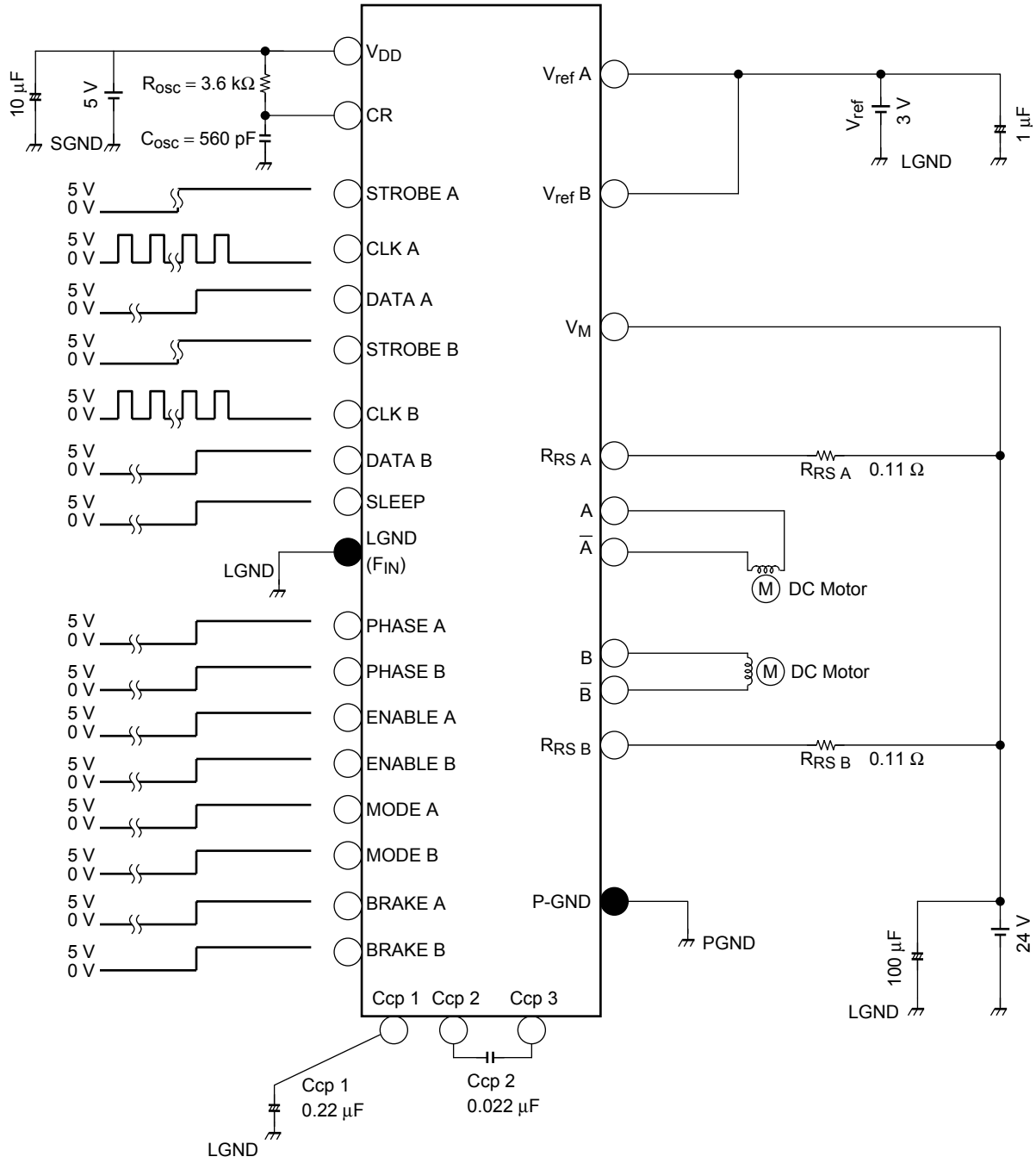
When driving a motor while V_{DD} = 5 V, f_{chop} = 150 kHz, L = 10 mH under the conditions of V_M = 27 V and 2.0 A, the logical values for Ccp 1 and Ccp 2 are as shown in the graph below:



Choose Ccp 1 and Ccp 2 to be combined from the above applicable range. We recommend Ccp 1:Ccp 2 at 10:1 or more. (If our recommended values (Ccp = 0.22 μF, Ccp 2 = 0.022 μF) are used, the drive conditions in the specification sheet are satisfied. (There is no capacitor temperature characteristic as a condition.)
When setting the constants, make sure that the charge pump voltage is not below the specified value and set the constants with a margin (the larger Ccp 1 and Ccp 2, the more the margin).
Some capacitors exhibit a large change in capacitance according to the temperature. Make sure the above capacitance is obtained under the IC ambient temperature.

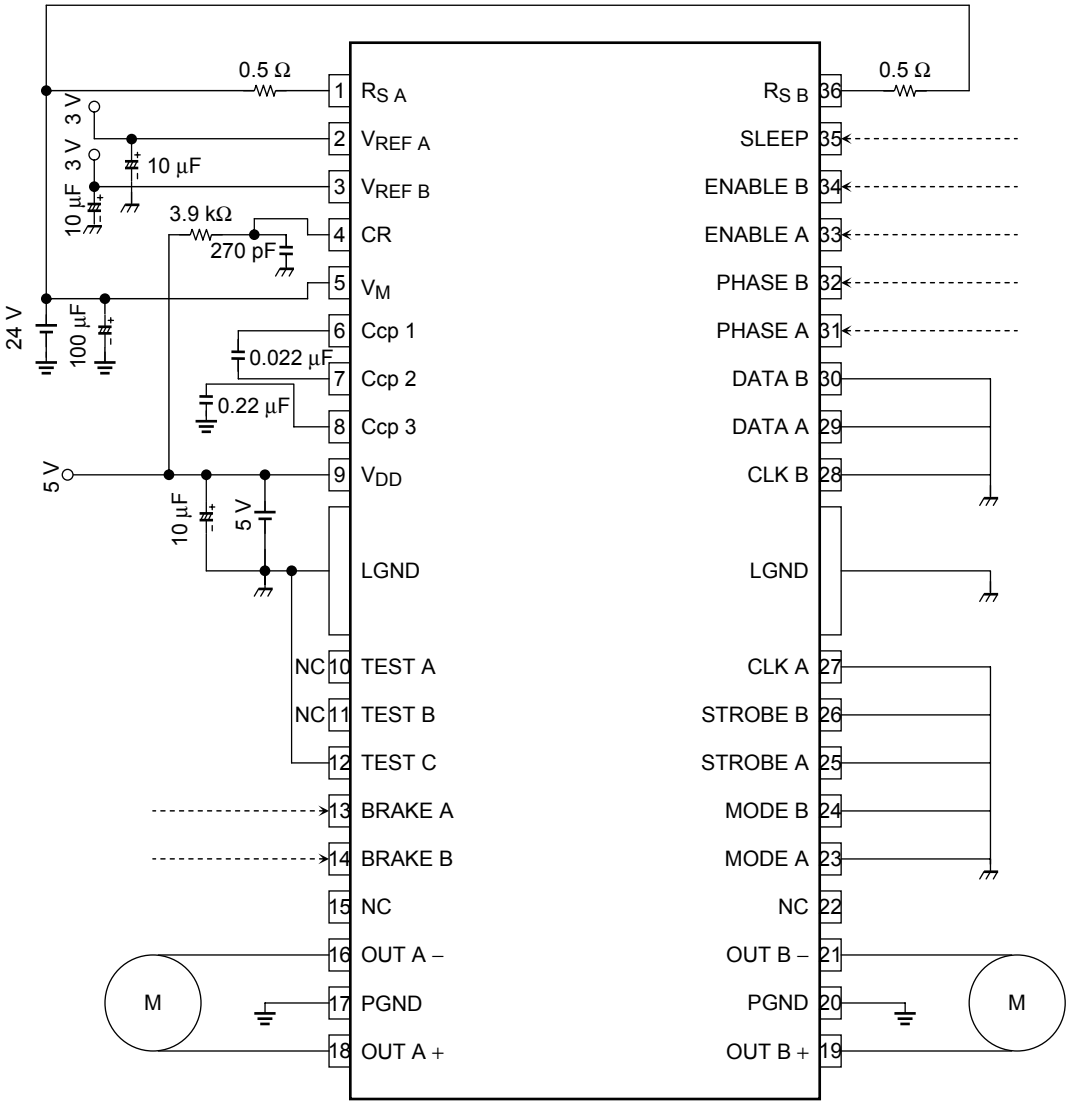
Recommended Application Circuit

The values of external constants are example recommended values. For values under different input conditions, see the above-mentioned recommended operating conditions.
(The following shows an example when fcho = 501 Hz (CR frequency = 800 kHz and constant-current limiter = 2.27 A) with serial signals placed in initial status.)



Note: It is recommended to add bypass capacitors as required.
Make sure that all gound pins are connected to the same ground rail.
STROBE, CLK, and DATA must be tied to LGND if serial input is not used for settings or motor control.
Because there may be short circuits between outputs, to supply, or to ground, be careful when designing output lines, V_{DD} (V_M) lines, and ground lines.

Connection Diagram (when external forced PWM mode is used)

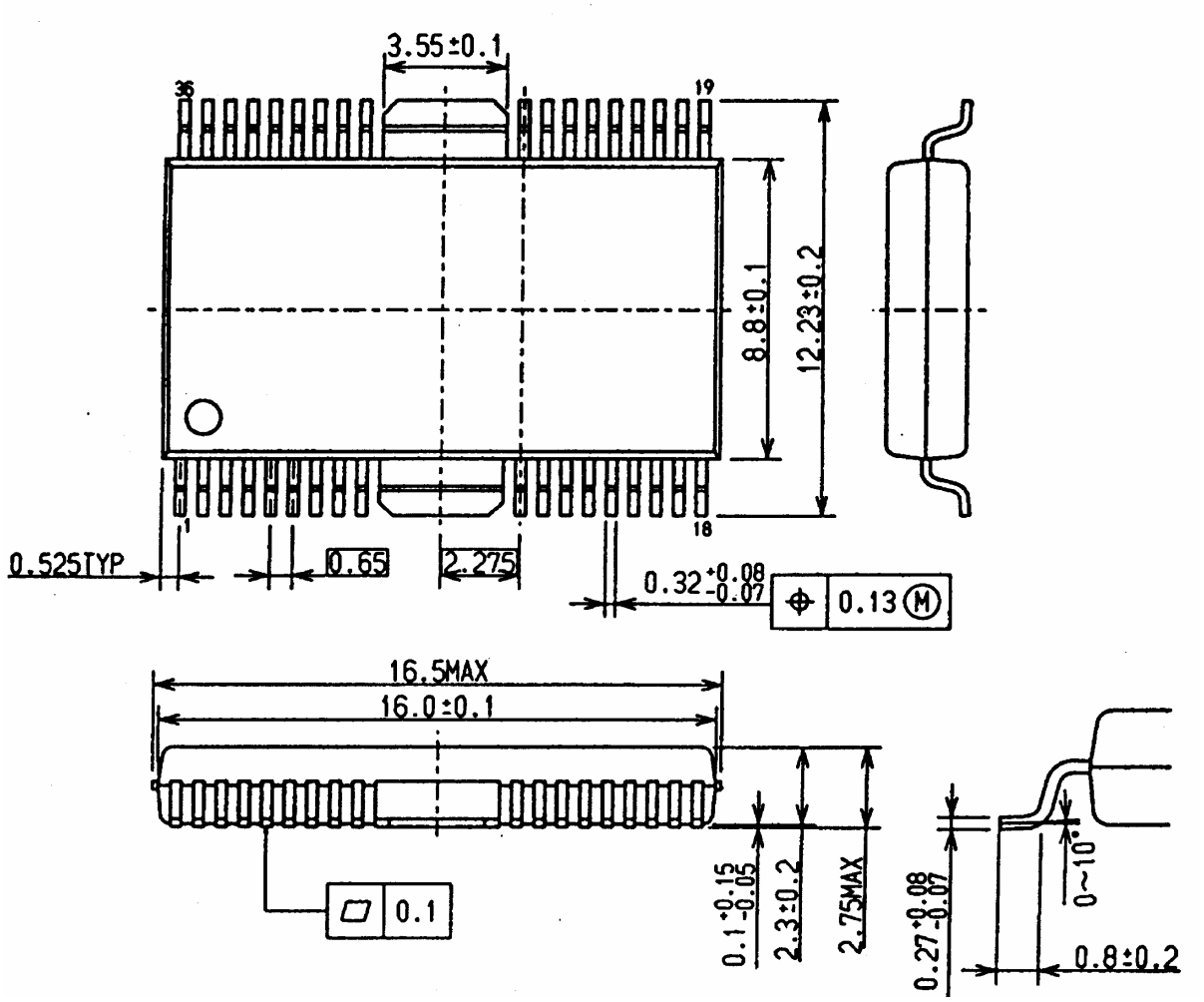


-----→ : Signal from central unit

Package Dimensions

HSOP36-P-450-0.65

Unit: mm



Weight: 0.79 g (typ.)

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