Preliminary Data Sheet
July 2000

microelectronics group

Lucent Technologies
Bell Labs Innovations

# T8535/T8536 Quad Programmable Codec

## Features

- 5 V operation
- Per-channel programmable gains, equalization, termination impedance, and hybrid balance
- Programmable μ-law, or A-law modes
  - — Up to 256 time slots per frame
  - — Supports PCM data rates of 512 kbits/s to 16.384 Mbits/s
  - — Double-clock mode timing compatible with ISDN standard interfaces
- Fully programmable time-slot assignment with bit offset
- Analog and digital loopback test modes
- Serial microprocessor interface
  - — Normal and byte-by-byte control modes
  - — Fast scan mode
- Six bidirectional control leads per channel, for SLIC and line card function control
- Differential analog output
  - — Mates directly to SLICs, eliminating external components
- Sigma-delta converters with dither noise reduction
- Quad design to minimize package count on dense line card applications
- Meets or exceeds ITU-T G.711—G.712 and relevant *Telcordia Technologies** requirements

## Description

The device consists of four independent channels of codec and digital signal processing functions on one chip. In addition to the classic A-to-D and D-to-A conversion, each channel provides termination impedance synthesis and a hybrid balance network.

The device is controlled by a serial microprocessor interface, and a series of bidirectional I/O leads are provided so that this control mechanism can be utilized to operate the battery feed device, ringing voltage switches, etc. Common data and clock paths can be shared over any number of devices. All the filter coefficients, signal processing, SLIC, and test features are accessible through this interface. This serial interface can be operated at speeds up to 4.096 Mbits/s.

The choice of a PCM bus is also programmable, with any channel capable of being assigned to any time slot. The PCM bus can be operated at speeds up to 16.384 Mbits/s, allowing for a maximum of 256 time slots. Separate transmit and receive interfaces are available for 4-wire bus designs, or they can be strapped together for a 2-wire PCM bus.

The device is available in four packages.

The T8536 64-pin TQFP features five data latches per channel and has two PCM ports.

The T8536 100-pin TQFP features six data latches per channel and has two PCM ports.

The T8536 68-pin PLCC features six data latches per channel and has one PCM port.

The T8535 44-pin PLCC has no data latches and one PCM port.

The T8535 and the T8533 Quad Programmable Line Card Signal Processor with Echo Cancellation are pin compatible, as are the T8536 68-pin PLCC device and the T8534 68-pin PLCC Quad Programmable Line Card Signal Processor with Echo Cancellation.

* *Telcordia Technologies* is a trademark of Bell Communications Research, Inc.

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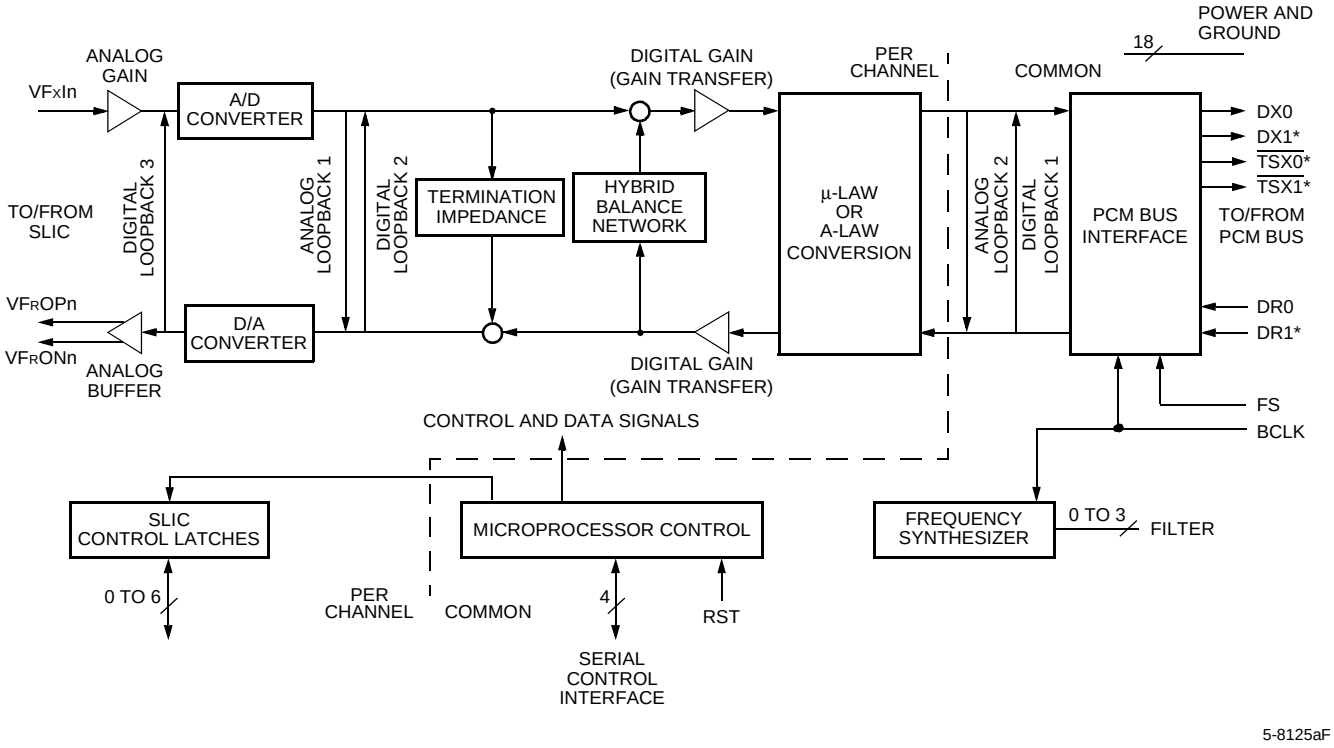
## General Description

Refer to Figure 1 for the following discussion.




* Second PCM port not available in all package types.

**Figure 1. Functional Block Diagram, Each Section**

This device performs virtually all the signal processing functions associated with a central office line termination. Functionality includes line termination impedance synthesis, fixed hybrid balance impedance synthesis, and level conversion both in the analog sense to accommodate various subscriber line interface circuits (SLICs) and in the digital sense for adjustment of the levels on the PCM bus. In general, the termination impedance synthesis generates the equivalent of a circuit with the parallel combination of a capacitor and a resistor in series with a resistor or the parallel combination of a resistor and the series combination of a resistor and capacitor. These general forms of impedance characteristic will satisfy most of the requirements specified throughout the world. Programmable selection of either μ-law or A-law encoding further aids worldwide deployment. All coefficients used in the filtering algorithms can be computed off-line in advance and downloaded to the device at the time of powerup. All signal processing is contained within the device, and there are only three interfaces of consequence to the system designer: the SLIC interface, the PCM interface, and the control interface.

The SLIC interface is designed to be flexible and convenient to use with a variety of SLIC circuits. With an appropriate choice of SLIC, no external components are required in the interface, with the exception of a dc blocking capacitor in the transmit direction. In some cases, dc blocking capacitors in the receive direction may be necessary as well, since the device operates from a single low-voltage supply.

## General Description (continued)

The PCM bus interface is flexible in that it allows, independently, the transmit and receive data for any channel to be placed in any time slot. The bus can be operated at a maximum 16.384 Mbits/s rate to accommodate a maximum 256 time slots. Separate pins are provided for each direction of transmission to allow 4-wire bus operation. The frame strobe signal is an 8 kHz signal that defines the beginning of the frame structure for all four channels. The interface will count 8 bits per time slot and insert or read the data for each channel as programmed. Lower speeds of the PCM bus are allowed. The PCM clock must be synchronous with the frame strobe signal.

The microprocessor control interface is a serial interface that uses the classical chip select type of operation. The interface controls the device by writing or reading various internal addresses. The command set consists of simple read and write operations, with the address determining the effect. All the memory locations, including the per-chip functions, are organized by channel.

There are several test modes included to facilitate confirmation of correct operation. In the signal path, two analog and three digital loopback tests are available, while in the microprocessor interface, there is a write/read test mode that tests the operation of the memory. Use of external test access switches allows a complete test of the signal path through the line card so that correct operation of various operational modes can be verified.

## Pin Information

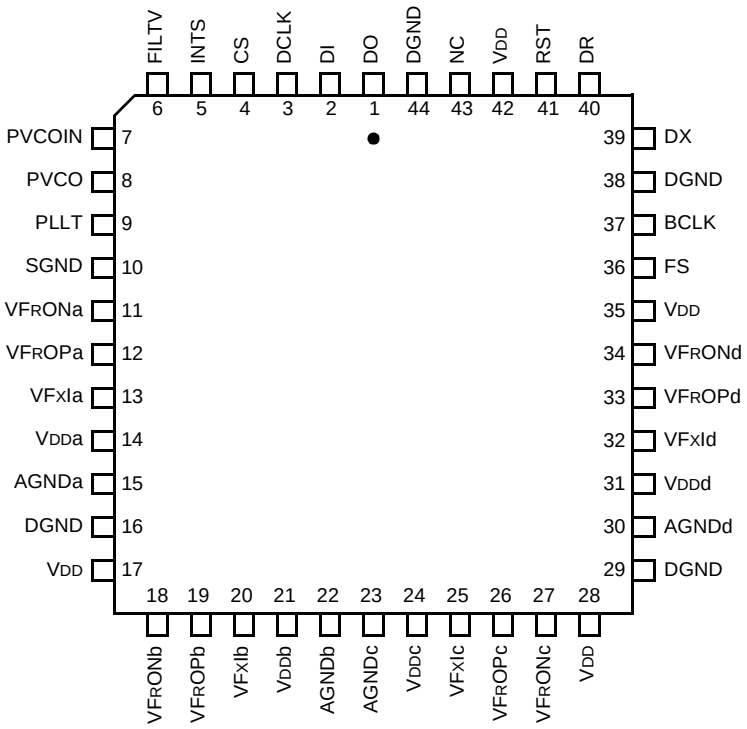



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**Figure 2. 44-Pin PLCC Pin Diagram**

**Table 1. Pin Assignments, 44-Pin PLCC, Per-Channel Functions**

| Ckt | | | | Name | Type | Name/Description |
|---|---|---|---|---|---|---|
| a | b | c | d | | | |
| 15 | 22 | 23 | 30 | AGND | GND | **Analog Ground.** A common AGND, DGND, SGND plane is highly recommended. |
| 14 | 21 | 24 | 31 | $V_{DD}$ | PWR | **Analog Power Supply.** |
| 13 | 20 | 25 | 32 | VFxI | I | **Voice Frequency Transmit Input.** |
| 12 | 19 | 26 | 33 | VFROP | O | **Voice Frequency Receive Output, Positive Polarity.** This pin can drive 2000 Ω (or greater) loads. |
| 11 | 18 | 27 | 34 | VFRON | O | **Voice Frequency Receive Output, Negative Polarity.** This pin can drive 2000 Ω (or greater) loads. |

## Pin Information (continued)

**Table 2. Pin Assignments, 44-Pin PLCC, Common Functions**

| Pin | Name | Type | Name/Description |
|---|---|---|---|
| 1 | DO | O | **Serial Data Output.** This is a 3-state output. |
| 2 | DI | I | **Serial Data Input.** |
| 3 | DCLK | I | **Serial Data Clock Input.** |
| 4 | CS | I | **Chip Select Input.** This lead determines the interval that the serial interface is active. |
| 5 | INTS | I | **Serial Interface Select.** Leaving this lead open places the serial interface in the normal mode; grounding it places the interface into the byte-by-byte mode. This lead has an internal pull-up. |
| 6 | FILTV | PWR | **Frequency Synthesizer Power (5 V).** This pin must be tied to $V_{DD}$. |
| 7 | PVCOIN | — | **Internal Test Point.** Do not connect to this lead. |
| 8 | PVCO | — | **Internal Test Point.** Do not connect to this lead. |
| 9 | PLLT | — | **Synthesizer Test Point.** Do not connect to this lead. |
| 10 | SGND | GND | **Synthesizer Ground.** Connect to digital ground. A common AGND, DGND, SGND plane is highly recommended. |
| 16, 29, 38, 44 | DGND | GND | **Digital Ground.** Logic ground and return for logic power supply. A common AGND, DGND, SGND plane is highly recommended. |
| 17, 28, 35, 42 | $V_{DD}$ | PWR | **Digital Power Supply (5 V).** |
| 36 | FS | I | **PCM Frame Strobe Input.** This 8 kHz clock must be derived from the same source as BCLK. |
| 37 | BCLK | I | **PCM Bit Clock Input.** This lead is used to develop internal clocks for certain clock rates. |
| 39 | DX | O | **PCM Transmit Data Output.** This is a 3-state output. |
| 40 | DR | I | **PCM Receive Data Input.** |
| 41 | RST | I | **Power-On Reset.** A low causes a reset of the entire chip. This pin may be connected to DGND with a 0.1 µF capacitor for a power-on reset function, or it may be driven by external logic. This lead has an internal pull-up. |
| 43 | NC | — | **No Connect.** This pin may be used as a tie point. |

## Pin Information (continued)

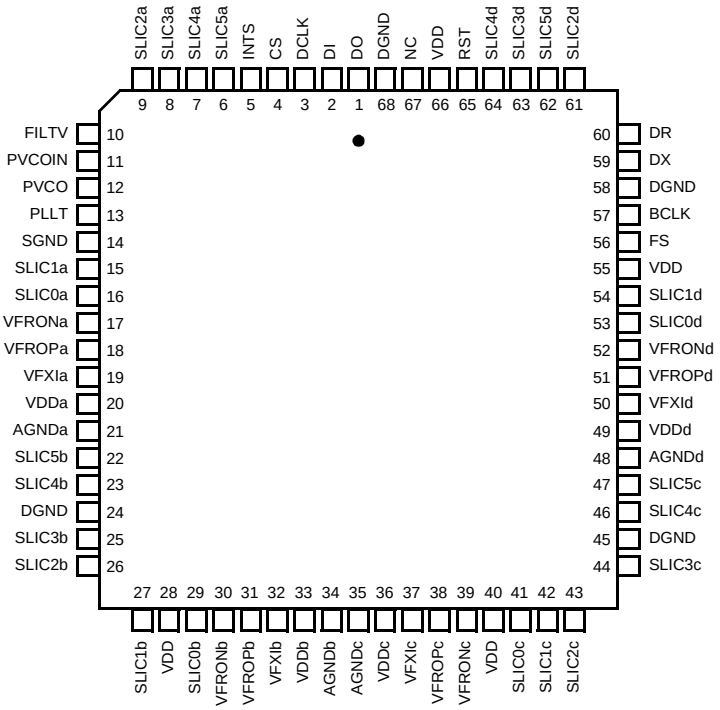


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**Figure 3. 68-Pin PLCC Pin Diagram**

**Table 3. Pin Assignments, 68-Pin PLCC, Per-Channel Functions**

| Ckt | | | | Name | Type | Name/Description |
|---|---|---|---|---|---|---|
| a | b | c | d | | | |
| 21 | 34 | 35 | 48 | AGND | GND | **Analog Ground.** A common AGND, DGND, SGND plane is highly recommended. |
| 20 | 33 | 36 | 49 | $V_{DD}$ | PWR | **Analog Power Supply.** |
| 19 | 32 | 37 | 50 | VFxI | I | **Voice Frequency Transmit Input.** |
| 18 | 31 | 38 | 51 | VFROP | O | **Voice Frequency Receive Output, Positive Polarity.** This pin can drive 2000 Ω (or greater) loads. |
| 17 | 30 | 39 | 52 | VFRON | O | **Voice Frequency Receive Output, Negative Polarity.** This pin can drive 2000 Ω (or greater) loads. |
| 16 | 29 | 41 | 53 | SLIC0 | I/O | **SLIC Control 0.** |
| 15 | 27 | 42 | 54 | SLIC1 | I/O | **SLIC Control 1.** |
| 9 | 26 | 43 | 61 | SLIC2 | I/O | **SLIC Control 2.** |
| 8 | 25 | 44 | 63 | SLIC3 | I/O | **SLIC Control 3.** |
| 7 | 23 | 46 | 64 | SLIC4 | I/O | **SLIC Control 4.** |
| 6 | 22 | 47 | 62 | SLIC5 | I/O | **SLIC Control 5.** |

## Pin Information (continued)

**Table 4. Pin Assignments, 68-Pin PLCC, Common Functions**

| Pin | Name | Type | Name/Description |
|---|---|---|---|
| 1 | DO | O | **Serial Data Output.** This is a 3-state output. |
| 2 | DI | I | **Serial Data Input.** |
| 3 | DCLK | I | **Serial Data Clock Input.** |
| 4 | CS | I | **Chip Select Input.** This lead determines the interval that the serial interface is active. |
| 5 | INTS | I | **Serial Interface Select.** Leaving this lead open places the serial interface in the normal mode; grounding it places the interface into the byte-by-byte mode. This lead has an internal pull-up. |
| 10 | FILTV | PWR | **Frequency Synthesizer Power (5 V).** This pin must be tied to $V_{DD}$. |
| 11 | PVCOIN | — | **Internal Test Point.** Do not connect to this lead. |
| 12 | PVCO | — | **Internal Test Point.** Do not connect to this lead. |
| 13 | PLLT | — | **Synthesizer Test Point.** Do not connect to this lead. |
| 14 | SGND | GND | **Synthesizer Ground.** Connect to digital ground. A common AGND, DGND, SGND plane is highly recommended. |
| 24, 45, 58, 68 | DGND | GND | **Digital Ground.** Logic ground and return for logic power supply. A common AGND, DGND, SGND plane is highly recommended. |
| 28, 40, 55, 66 | $V_{DD}$ | PWR | **Digital Power Supply (5 V).** |
| 56 | FS | I | **PCM Frame Strobe Input.** This 8 kHz clock must be derived from the same source as BCLK. |
| 57 | BCLK | I | **PCM Bit Clock Input.** This lead is used to develop internal clocks for certain clock rates. |
| 59 | DX | O | **PCM Transmit Data Output.** This is a 3-state output. |
| 60 | DR | I | **PCM Receive Data Input.** |
| 65 | RST | I | **Power-On Reset.** A low causes a reset of the entire chip. This pin may be connected to DGND with a 0.1 µF capacitor for a power-on reset function, or it may be driven by external logic. This lead has an internal pull-up. |
| 67 | NC | — | **No Connect.** Pin may be used as a tie point. |

## Pin Information (continued)

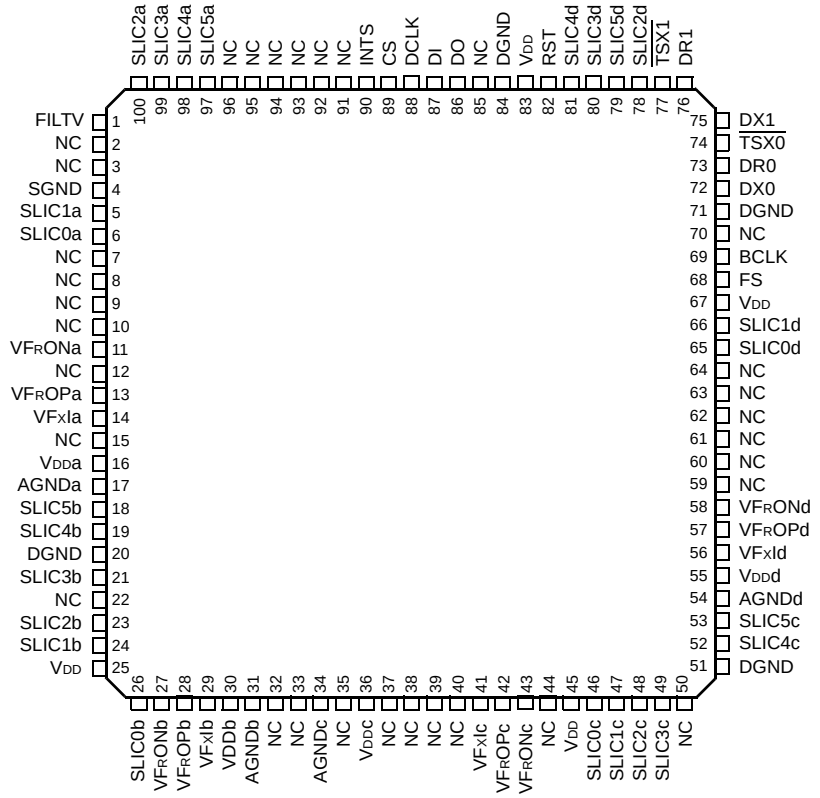


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**Figure 4. 100-Pin TQFP Pin Diagram**

**Table 5. Pin Assignments, 100-Pin TQFP, Per-Channel Functions**

| Ckt | | | | Name | Type | Name/Description |
|---|---|---|---|---|---|---|
| a | b | c | d | | | |
| 17 | 31 | 34 | 54 | AGND | GND | **Analog Ground.** A common AGND, DGND, SGND plane is highly recommended. |
| 16 | 30 | 36 | 55 | VDD | PWR | **Analog Power Supply.** |
| 14 | 29 | 41 | 56 | VFxI | I | **Voice Frequency Transmit Input.** |
| 13 | 28 | 42 | 57 | VFROP | O | **Voice Frequency Receive Output, Positive Polarity.** This pin can drive 2000 Ω (or greater) loads. |
| 11 | 27 | 43 | 58 | VFRON | O | **Voice Frequency Receive Output, Negative Polarity.** This pin can drive 2000 Ω (or greater) loads. |
| 6 | 26 | 46 | 65 | SLIC0 | I/O | **SLIC Control 0.** |
| 5 | 24 | 47 | 66 | SLIC1 | I/O | **SLIC Control 1.** |
| 100 | 23 | 48 | 78 | SLIC2 | I/O | **SLIC Control 2.** |
| 99 | 21 | 49 | 80 | SLIC3 | I/O | **SLIC Control 3.** |
| 98 | 19 | 52 | 81 | SLIC4 | I/O | **SLIC Control 4.** |
| 97 | 18 | 53 | 79 | SLIC5 | I/O | **SLIC Control 5.** |

## Pin Information (continued)

**Table 6. Pin Assignments, 100-Pin TQFP, Common Functions**

| Pin | Name | Type | Name/Description |
|---|---|---|---|
| 1 | FILTV | PWR | **Frequency Synthesizer Power (5 V).** This pin must be tied to $V_{DD}$. |
| 2, 3, 7—10, 12, 15, 22, 32, 33, 35, 37—40, 44, 50, 59—64, 70, 85, 91—96 | NC | — | **No Connect.** Pin may be used as a tie point. |
| 4 | SGND | GND | **Synthesizer Ground.** Connect to digital ground. A common AGND, DGND, SGND plane is highly recommended. |
| 20, 51, 71, 84 | DGND | GND | **Digital Ground.** Logic ground and return for logic power supply. A common AGND, DGND, SGND plane is highly recommended. |
| 25, 45, 67, 83 | $V_{DD}$ | PWR | **Digital Power Supply (5 V).** |
| 68 | FS | I | **PCM Frame Strobe Input.** This 8 kHz clock must be derived from the same source as BCLK. |
| 69 | BCLK | I | **PCM Bit Clock Input.** This lead is used to develop internal clocks for certain clock rates. |
| 72 | DX0 | O | **PCM Transmit Data Output 0.** This is a 3-state output. |
| 73 | DR0 | I | **PCM Receive Data Input 0.** |
| 74 | $\overline{TSX0}$ | O | **Backplane Line Driver Enable 0 (Active-Low).** Normally, these open-drain outputs are floating in a high-impedance state. When a time slot is active on DX0, this output pulls low to enable a backplane line driver. |
| 75 | DX1 | O | **PCM Transmit Data Output 1.** This is a 3-state output. |
| 76 | DR1 | I | **PCM Receive Data Input 1.** |
| 77 | $\overline{TSX1}$ | O | **Backplane Line Driver Enable 1 (Active-Low).** Normally, these open-drain outputs are floating in a high-impedance state. When a time slot is active on DX1, this output pulls low to enable a backplane line driver. |
| 82 | RST | I | **Power-On Reset.** A low causes a reset of the entire chip. This pin may be connected to DGND with a 0.1 μF capacitor for a power-on reset function, or it may be driven by external logic. This lead has an internal pull-up. |
| 86 | DO | O | **Serial Data Output.** This is a 3-state output. |
| 87 | DI | I | **Serial Data Input.** |
| 88 | DCLK | I | **Serial Data Clock Input.** |
| 89 | CS | I | **Chip Select Input.** This lead determines the interval that the serial interface is active. |
| 90 | INTS | I | **Serial Interface Select.** Leaving this lead open places the serial interface in the normal mode; grounding it places the interface into the byte-by-byte mode. This lead has an internal pull-up. |

## Pin Information (continued)

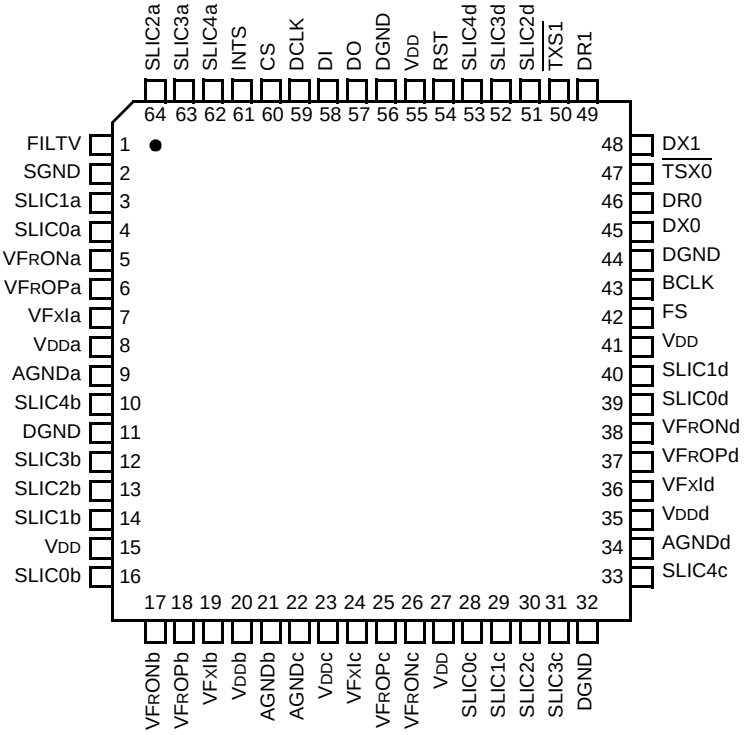


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**Figure 5. 64-Pin TQFP Pin Diagram**

**Table 7. Pin Assignments 64-Pin TQFP, Per-Channel Functions**

| Ckt | | | | Name | Type | Name/Description |
|---|---|---|---|---|---|---|
| a | b | c | d | | | |
| 9 | 21 | 22 | 34 | AGND | GND | **Analog Ground.** A common AGND, DGND, SGND plane is highly recommended. |
| 8 | 20 | 23 | 35 | $V_{DD}$ | PWR | **Analog Power Supply.** |
| 7 | 19 | 24 | 36 | VFxI | I | **Voice Frequency Transmit Input.** |
| 6 | 18 | 25 | 37 | VFROP | O | **Voice Frequency Receive Output, Positive Polarity.** This pin can drive 2000 Ω (or greater) loads. |
| 5 | 17 | 26 | 38 | VFRON | O | **Voice Frequency Receive Output, Negative Polarity.** This pin can drive 2000 Ω (or greater) loads. |
| 4 | 16 | 28 | 39 | SLIC0 | I/O | **SLIC Control 0.** |
| 3 | 14 | 29 | 40 | SLIC1 | I/O | **SLIC Control 1.** |
| 64 | 13 | 30 | 51 | SLIC2 | I/O | **SLIC Control 2.** |
| 63 | 12 | 31 | 52 | SLIC3 | I/O | **SLIC Control 3.** |
| 62 | 10 | 33 | 53 | SLIC4 | I/O | **SLIC Control 4.** |

## Pin Information (continued)

**Table 8. Pin Assignments 64-Pin TQFP, Common Functions**

| Pin | Name | Type | Name/Description |
|---|---|---|---|
| 1 | FILTV | PWR | **Frequency Synthesizer Power (5 V).** This pin must be tied to $V_{DD}$. |
| 2 | SGND | GND | **Synthesizer Ground.** Connect to digital ground. A common AGND, DGND, SGND plane is highly recommended. |
| 11, 32, 44, 56 | DGND | GND | **Digital Ground.** Logic ground and return for logic power supply. A common AGND, DGND, SGND plane is highly recommended. |
| 15, 27, 41, 55 | $V_{DD}$ | PWR | **Digital Power Supply (5 V).** |
| 42 | FS | I | **PCM Frame Strobe Input.** This 8 kHz clock must be derived from the same source as BCLK. |
| 43 | BCLK | I | **PCM Bit Clock Input.** This lead is used to develop internal clocks for certain clock rates. |
| 45 | DX0 | O | **PCM Transmit Data Output 0.** This is a 3-state output. |
| 46 | DR0 | I | **PCM Receive Data Input 0.** |
| 47 | $\overline{TSX0}$ | O | **Backplane Line Driver Enable 0 (Active-Low).** Normally, these open-drain outputs are floating in a high-impedance state. When a time slot is active on DX0, this output pulls low to enable a backplane line driver. |
| 48 | DX1 | O | **PCM Transmit Data Output 1.** This a 3-state output. |
| 49 | DR1 | I | **PCM Receive Data Input 1.** |
| 50 | $\overline{TSX1}$ | O | **Backplane Line Driver Enable 1 (Active-Low).** Normally, these open-drain outputs are floating in a high-impedance state. When a time slot is active on DX1, this output pulls low to enable a backplane line driver. |
| 54 | RST | I | **Power-On Reset.** A low causes a reset of the entire chip. This pin may be connected to DGND with a 0.1 μF capacitor for a power-on reset function, or it may be driven by external logic. This lead has an internal pull-up. |
| 57 | DO | O | **Serial Data Output.** This is a 3-state output. |
| 58 | DI | I | **Serial Data Input.** |
| 59 | DCLK | I | **Serial Data Clock Input.** |
| 60 | CS | I | **Chip Select Input.** This lead determines the interval that the serial interface is active. |
| 61 | INTS | I | **Serial Interface Select.** Leaving this lead open places the serial interface in the normal mode; grounding it places the interface into the byte-by-byte mode. This lead has an internal pull-up. |

# Functional Description

## Clocking Considerations

The PCM bus uses BCLK as the bit clock and the one-going edge of FS to determine the location of the beginning of a frame. These two clocks must be derived from the same source. Internally, the device develops all the internal clocks with a phase-locked loop that uses BCLK as the timing source. BCLK and FS must be continuously present and without gaps in order for the device to operate correctly.

DCLK is used to clock the internal serial interface and may be asynchronous to the other clocks. There is no need to derive this clock from the same source as the other clocks. The serial bus may be operated at any speed up to 4.096 Mbits/s. DCLK can be gapped, however additional clock cycles are required in and around the command frame to process data, and during and after a hardware or a software reset to ensure complete clearing of internal logic. There is no limit on the number of devices on the same serial bus.

## The Control Interface

The device is controlled via a series of memory locations accessed by a serial data connection to the external master controller. This interface operates using the chip select lead to enable transmission of information. All chip functions are enabled or disabled by setting or clearing bits in the control memory. Filter coefficients and gain adjustments are also stored in this memory.

The codec has both a serial input lead and a serial output lead. These may be used individually for a 4-wire serial interface, or tied together for a 2-wire interface. The line driver circuitry is capable of driving relatively high currents so that in the event that the line is long enough to show significant transmission line effects, it can be terminated in the characteristic impedance at each end with resistors to $V_{CC}$ and ground.

All data transfers on the serial bus are byte oriented with the least significant bit (shown in this data sheet as bit 0) transmitted first, followed by the more significant bits. For data fields, the least significant byte of the first data byte is transmitted first, followed by the more significant bytes, each byte transmitted LSB first. This format is compatible with the serial port on most microcontrollers.

### Modes

There are two different modes of operation for the serial interface, the normal mode and the byte-by-byte mode. These two modes differ in the manner in which CS is used to control the transfer. Note that the CS lead is used to control the transfer of serial data from master controller to slave codec and in the reverse direction.

In normal mode, (INTS pin open) the CS lead must go low for the duration of the transfer. The only error check performed by the codec is to verify that CS is low for an integral number of bytes. Detection of an active (active-low) chip select for other than an integral multiple of 8 bits results in the operation being terminated. The next active excursion of chip select will be interpreted as a new command; hence, the serial I/O interface can always be initialized by asserting CS for a number of clock periods that is not an integral multiple of 8. CS is captured using DCLK, so DCLK must be transitioned to perform this initialization. Undefined command codes are reserved for future use and may cause unwanted operation of the device.

The byte-by-byte mode (INTS pin tied to ground) uses CS to control each byte of the transfer. In this mode, CS goes low for exactly 8 bits at a time, corresponding to a 1-byte transfer either to or from the codec chip. Repeated transitions of CS are used to control subsequent bytes of data to/from the codec. For a write command in this mode, CS must go low for each byte of the transfer until the transfer is complete. For a read command, CS will go low for each of the 3 bytes of the read command transferred to the device, then low again for each byte to be read. Notice that the total number of bytes transferred (and excursions on CS) is N + 3, where N is the number of bytes to be read in the command. This mode of operation is useful in cases where the master is a microprocessor with a built-in UART that transfers 1 byte at a time. Error detection is limited to detection of an active CS for other than an integral multiple of 8 bits. Recovery is the same as normal mode. Note that the clock phase is shifted in this mode.

Flow control can be accomplished by suspending the transitions on DCLK by holding either state. During the data transfer, CS must remain low while clock transitions are suspended with DCLK in either state.

## Functional Description (continued)

### The Control Interface (continued)

#### Protocol

The format of the command protocol is shown in Figures 6 and 7.

The control interface operates with one external master controller and multiple slave codec devices. Each transfer is initiated by the master, and the slave responds for either read operations or the fast scan mode. The slave does not check the bus for activity prior to transmitting; it only checks for an active CS. The master should allow for a wait between the end of a read command until CS becomes active for the read data. The master must refrain from sending additional commands to the slave chip until the response is received. On a 4-wire bus, commands to other devices may be initiated before the response is received, but care in generating the CS function is needed to ensure that the multiple responses do not interfere. It should be noted that multiple memory locations can be accessed in the same command by setting the data field length field to the desired number of bytes to be transferred. If flow control is desired, it must be performed by using separate commands, each transferring smaller blocks of information, or by controlling the serial clock (gapping the serial clock), or with CS in the case of byte-by-byte mode.

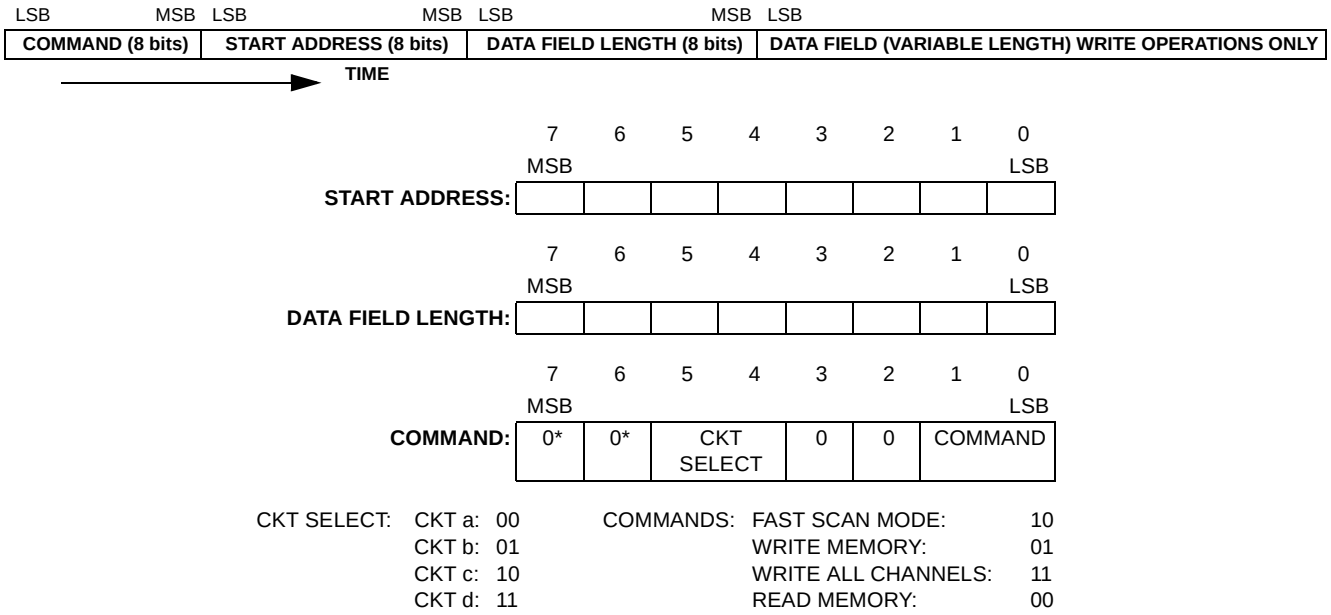
There is no response from the slave to the master for a write operation. The response to a read operation simply includes the data to be read in the data field. This data is sent least significant bit first, with the bytes sent in ascending sequence. Commands from the master controller include data for write operations, but not for read operations. Since the coefficients and gains are stored in volatile memory, all the coefficients and gains must be loaded after powerup. There is, however, no need to reload them when switching from active to standby modes, or vice versa. Great care should be exercised in loading memory when the codec channel is not in standby mode. Sudden changes in the termination or balance impedances can result in undesirable system operation.

All data is transmitted in a byte-oriented fashion with the least significant bit of each byte transferred first. Multibyte fields are transferred least significant byte first in both directions. The data field will contain the first addressed data location first, with subsequent data locations transmitted in ascending order.

## Functional Description (continued)

### The Control Interface (continued)

**Protocol** (continued)




* Location of memory bank selection. All user controls are in memory bank 0; other memory banks contain internal state information for the device.

Note: Data field length is in bytes for all operations. All data is transmitted in bytes with the LSB for each byte transmitted first. For 16-bit memory operations, the least significant byte of the first memory location is transmitted first, followed by the most significant byte; each byte is transmitted LSB first. Additional memory locations are loaded in ascending sequence.

**Figure 6. Command Frame Format, Master to Slave, Read or Write Commands**


Note: All data is transmitted in bytes with the LSB for each byte transmitted first. For memory operations, the least significant byte of the first memory location is transmitted first, followed by the most significant byte, each byte transmitted LSB first. Additional memory locations are loaded in ascending sequence.

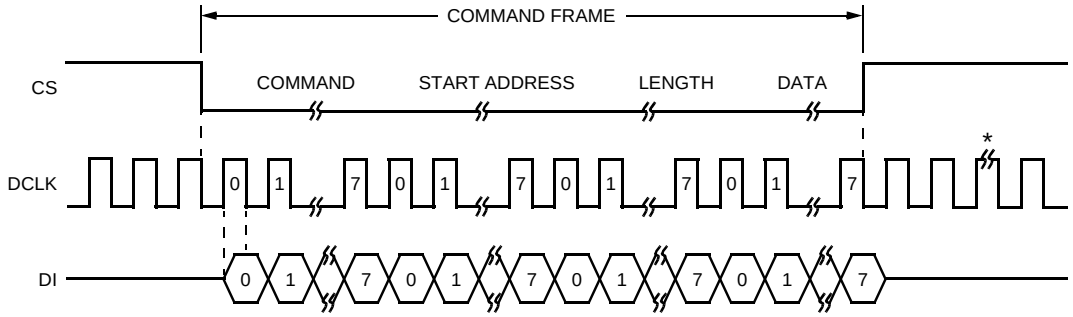
**Figure 7. Command Frame Format, Slave to Master, Read Commands**

## Functional Description (continued)

### The Control Interface (continued)

#### Write Command

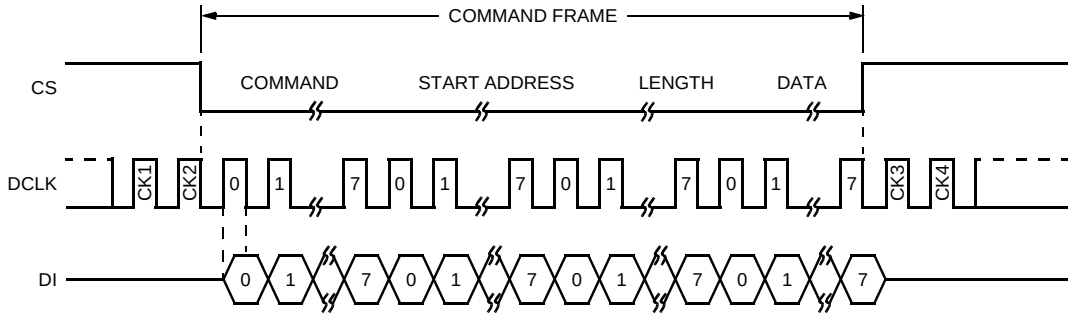
A write command is used to write to the memory addresses. Figures 8—11 illustrate normal or byte-by-byte operation with continuous or gapped DCLKs. For gapped DCLK operation, transitions, not frequency, are critical (as long as transitions occur no faster than 122 ns apart).




* Two or more full DCLK cycles are required before the start of a new command frame.

Note: Data field length of 1 shown.

**Figure 8. Write Operation, Normal Mode (Continuous DCLK)**




Notes:

Data field length of 1 shown.

CK1 through CK4 are additional DCLK pulses required to properly process the data.

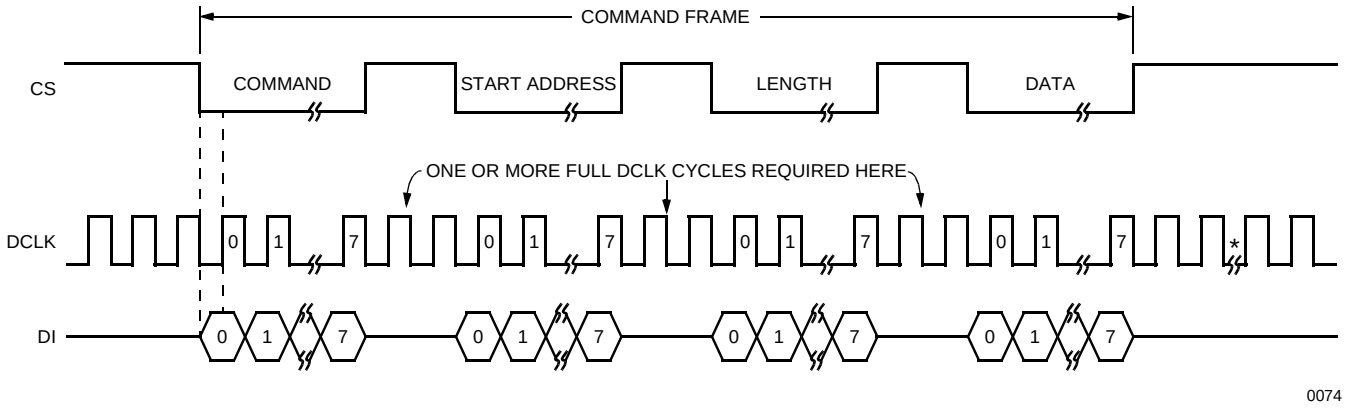
CK3 and CK4 are not necessary if another command frame follows this sequence.

**Figure 9. Write Operation, Normal Mode (Gapped DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

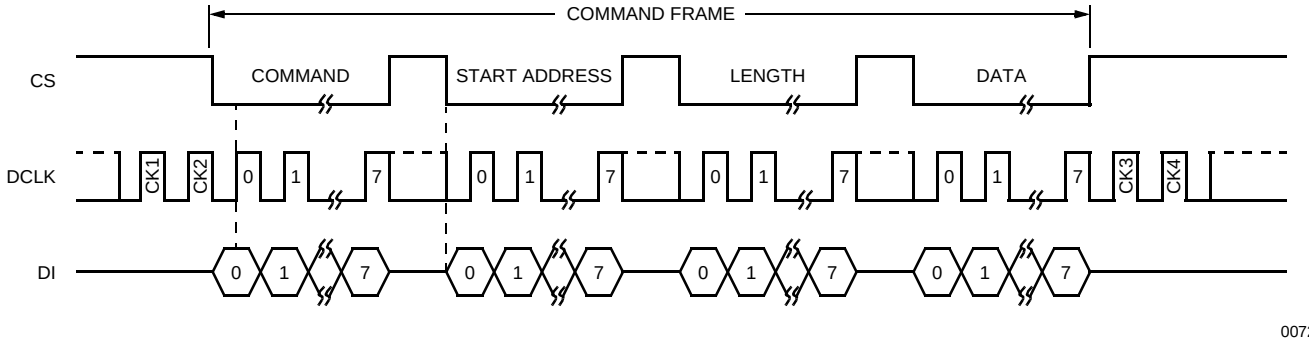
**Write Command** (continued)




* Two or more full DCLK cycles are required before the start of a new command frame.

Note: Data field length of 1 shown.

**Figure 10. Write Operation, Byte-by-Byte Mode (Continuous DCLK)**




Notes:

Data field length of 1 shown.

CK1 through CK4 are additional DCLK pulses required to properly process the data.

CK3 and CK4 are not necessary if another command frame follows this sequence.

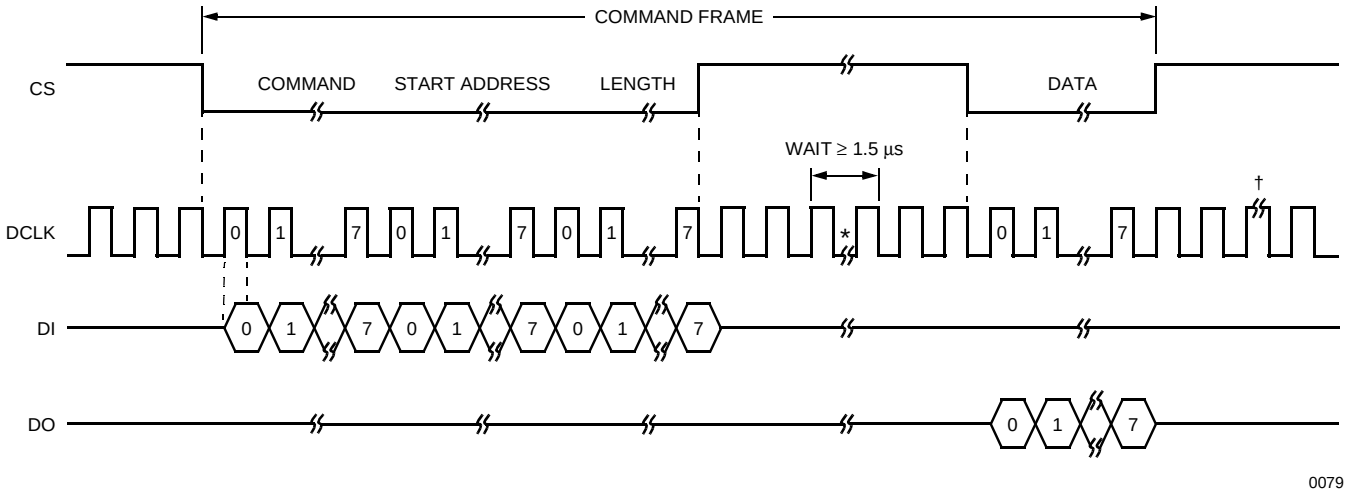
**Figure 11. Write Operation, Byte-by-Byte Mode (Gapped DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

#### Read Command

The normal flow of information to the master controller is always in response to a read command. All control memory locations are accessed in 8-bit bytes. All read commands from the master controller require a response from the addressed codec. It is the responsibility of the master controller to ensure that only one device is transmitting on the serial interface line at any one time. The master controller also must ensure that the CS lead goes high after transferring the 3-byte sequence used to initiate the read, and then it goes low again for the response. In this case, it should be noted that the device expects the second time CS goes low that data is to be sent to the master; thus, it does not interpret the DI lead as containing a valid instruction during that CS excursion and a write during this time is not recommended. Note also that the CS lead must allow the number of bytes sent in a read command to be transferred before a subsequent command can be received by the codec. Figures 12—15 illustrate normal or byte-by-byte operation with continuous or gapped DCLKs. Like a write command, transitions, not frequency, are critical with regard to gapped DCLK operation.




* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait ≥ 1.5 µs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between LENGTH and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

† Two or more DCLK cycles are required before the start of a new command frame.

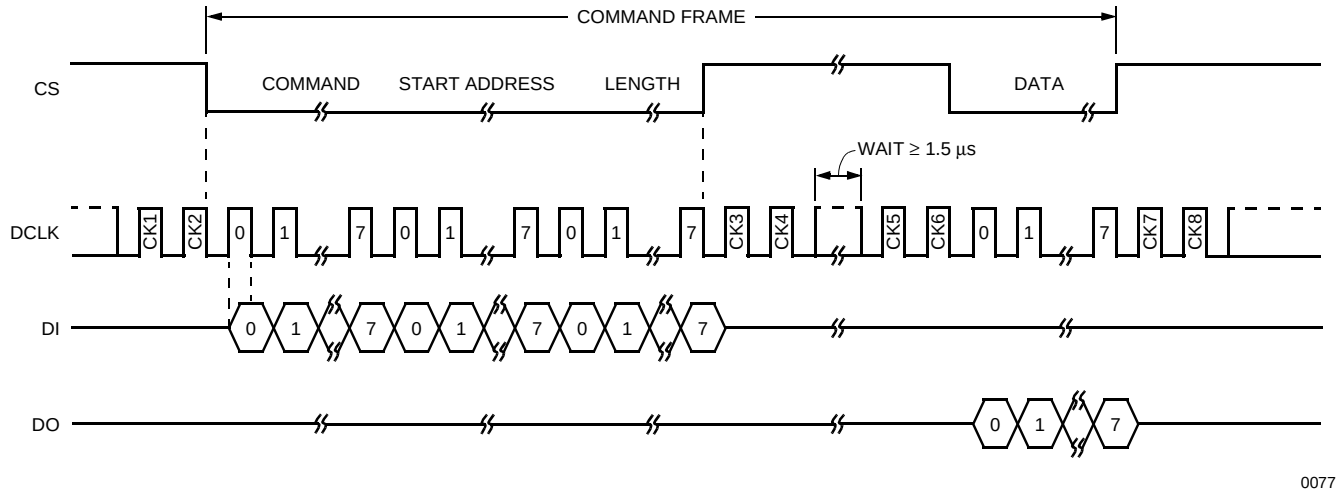
Note: Data field length of 1 shown.

**Figure 12. Read Operation, Normal Mode (Continuous DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

#### Read Command (continued)




Notes:

Data field length of 1 shown.

CK1 through CK8 are additional DCLK pulses required to properly process the data.

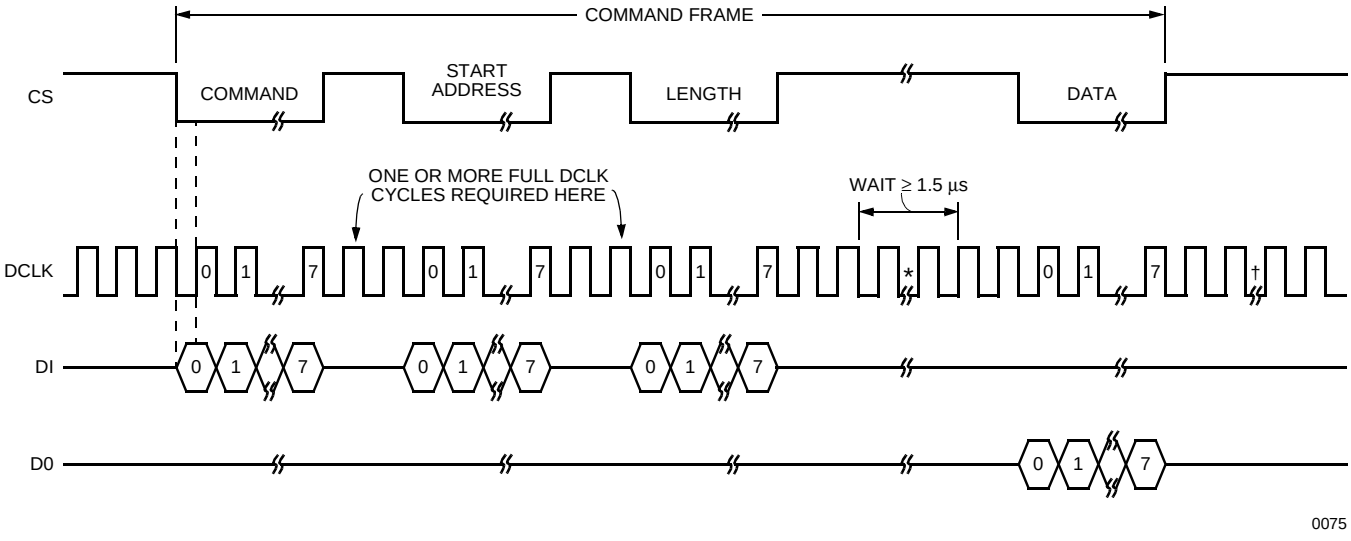
CK7 and CK8 are not necessary if another command frame follows this sequence.

**Figure 13. Read Operation, Normal Mode (Gapped Clock)**

## Functional Description (continued)

### The Control Interface (continued)

**Read Command** (continued)




* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait ≥ 1.5 µs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between LENGTH and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

† Two or more DCLK cycles are required before the start of a new command frame.

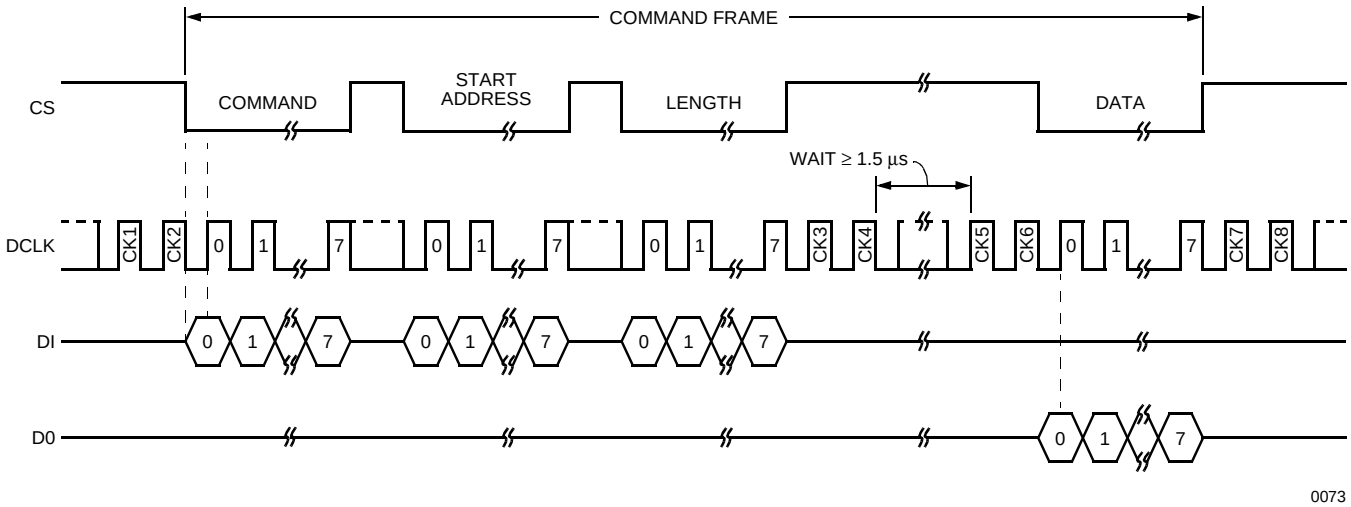
Note: Data field length of 1 shown.

**Figure 14. Read Operation, Byte-by-Byte Mode (Continuous DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

**Read Command** (continued)




Notes:

Data field length of 1 shown.

CK1 through CK8 are additional DCLK pulses required to properly process the data.

CK7 and CK8 are not necessary if another command frame follows this sequence.

**Figure 15. Read Operation, Byte-by-Byte Mode (Gapped DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

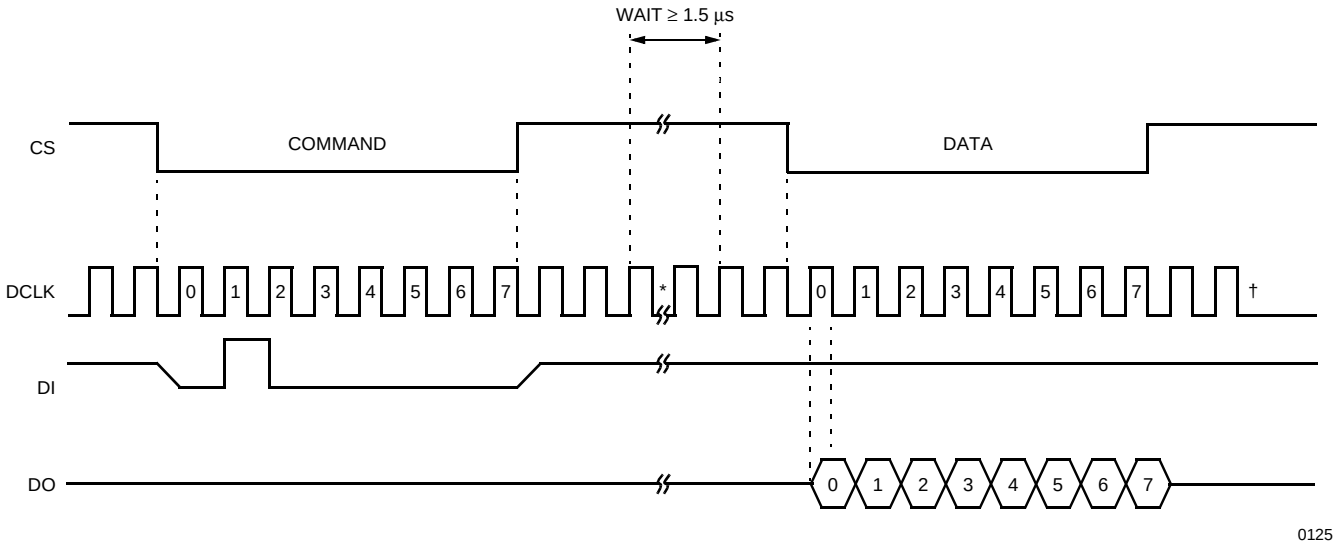
#### Fast Scan Mode

The fast scan mode allows a single byte command to read two SLIC control leads for all four channels with a 1-byte reply. This mode significantly speeds up the normal scanning for off-hook, ring trip, and ring ground detection. This special command sequence allows the controlling microprocessor to fast scan 2 bits in the SLIC control byte of each of the four channels. The command code is $(00000010)_2$; there are no start address or length fields. The command returns only a single byte of data, formatted as shown in Table 9.

**Table 9. Bit Assignments for Fast Scan Mode**

| Bit | Reported Status |
|---|---|
| 0 (LSB) | Channel 0, bit 0 (ckt a, address 160, bit 0) |
| 1 | Channel 0, bit 1 (ckt a, address 160, bit 1) |
| 2 | Channel 1, bit 0 (ckt b, address 160, bit 0) |
| 3 | Channel 1, bit 1 (ckt b, address 160, bit 1) |
| 4 | Channel 2, bit 0 (ckt c, address 160, bit 0) |
| 5 | Channel 2, bit 1 (ckt c, address 160, bit 1) |
| 6 | Channel 3, bit 0 (ckt d, address 160, bit 0) |
| 7 (MSB) | Channel 3, bit 1 (ckt d, address 160, bit 1) |

The circuit select in the command structure (Figure 6) is not used for this special single-byte command. The rules for toggling chip select apply as for the read command. Figures 16—19 illustrate normal or byte-by-byte operation with continuous or gapped DCLKs.




* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait ≥ 1.5 µs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between COMMAND and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

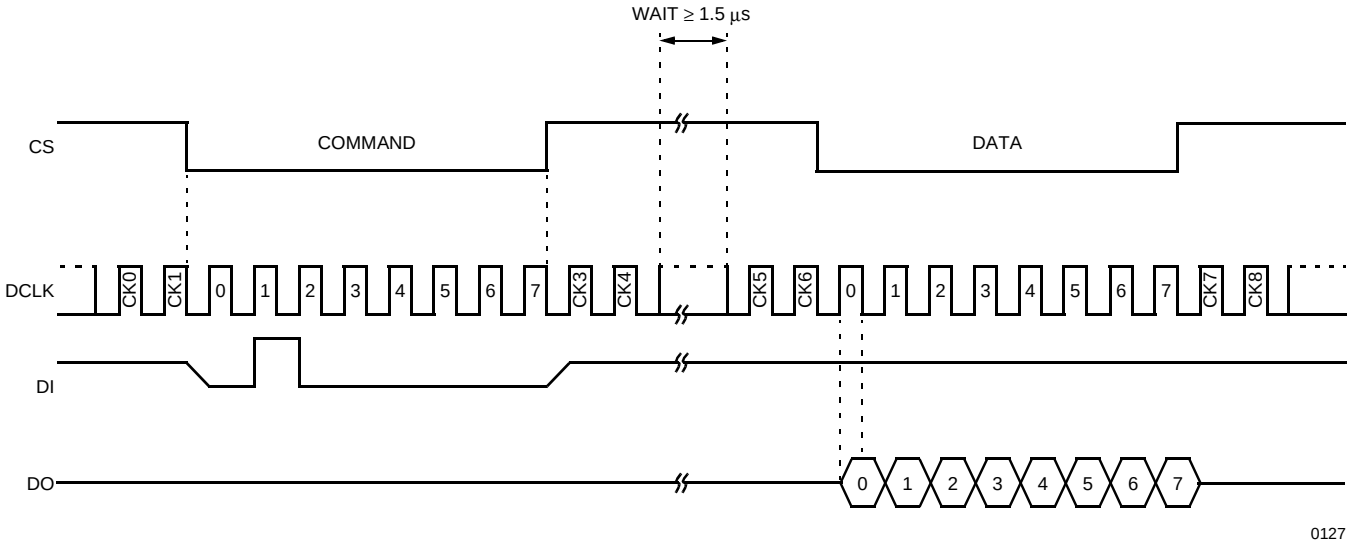
† Two or more DCLK cycles are required before the start of a new command frame.

**Figure 16. Fast Scan, Normal Mode (Continuous DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

#### Fast Scan Mode (continued)



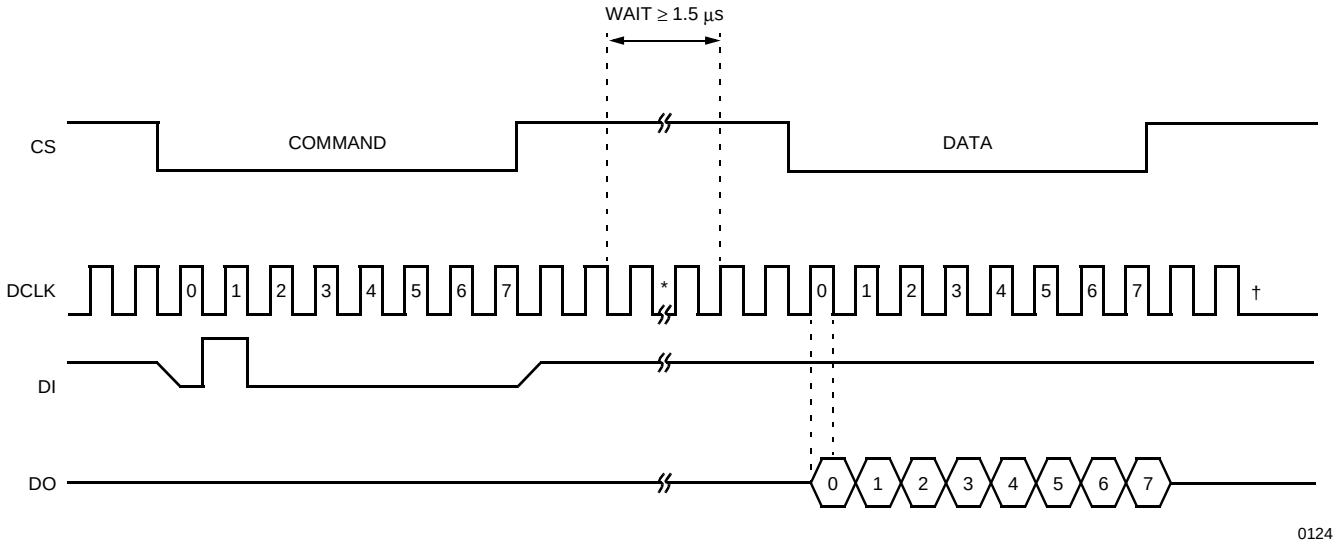

Note: CK1 through CK8 are additional DCLK pulses required to properly process the data.

**Figure 17. Fast Scan, Normal Mode (Gapped DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

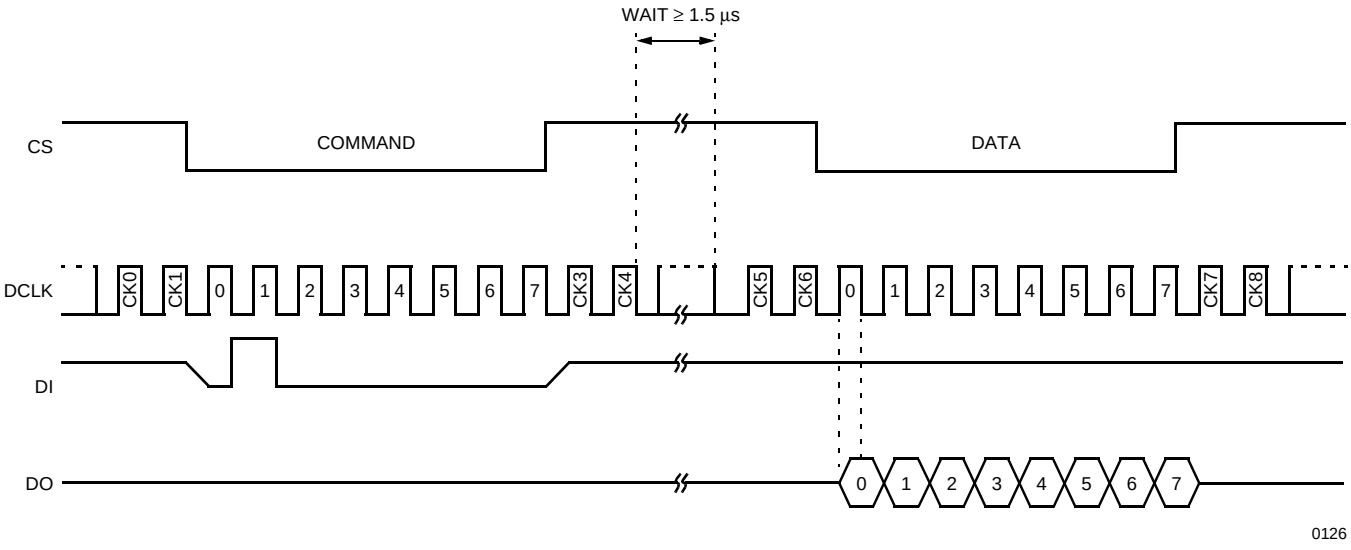
#### Fast Scan Mode (continued)




* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait ≥ 1.5 µs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between COMMAND and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

† Two or more DCLK cycles are required before the start of a new command frame.

**Figure 18. Fast Scan, Byte-by-Byte Mode (Continuous DCLK)**




Note: CK1 through CK8 are additional DCLK pulses required to properly process the data.

**Figure 19. Fast Scan, Byte-by-Byte Mode (Gapped DCLK)**

## Functional Description (continued)

### The Control Interface (continued)

#### Write All Channels

The write all channels command causes all four channels to be loaded with the same coefficients with a single data transfer from the master controller. This allows for a faster initialization of the device after a powerup. This command should be used with caution since it affects all four channels. The normal memory write and read commands affect only one channel.

### Reset Functionality

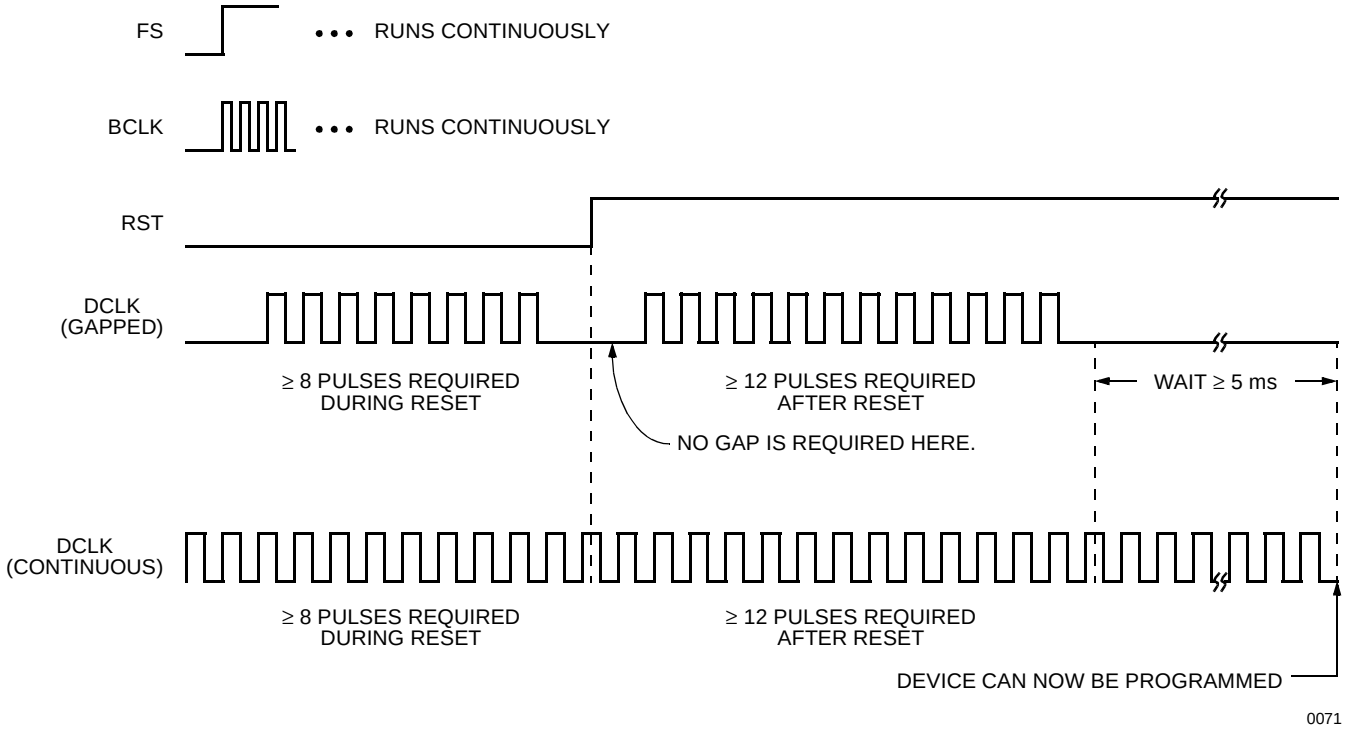



**Figure 20. Hardware Reset Procedure**

The reset function allows the internal logic of the device to be set to a known initial condition, either externally by activating the reset lead, or on a per-channel basis through the microprocessor interface by setting and then clearing bits, if required, in address RESCTRL (address 128). These two reset functions have different effects, and each of the software reset functions is a subset of the hardware reset functionality. The primary difference is in the treatment of the internal memory. The hardware reset is assumed to be a result of a catastrophic hardware event, such as a loss of power or an initial powerup. Accordingly, the assumption is made that the internal memory does not contain valid data, and default values for all memory locations are loaded. A software reset, however, can only be initiated if the device is operational (at least the microprocessor interface), so the contents of the memory may indeed be valid; thus, the resets may be more specific. Additionally, software resets only affect the selected channel.

## Functional Description (continued)

### Reset Functionality (continued)

A 0.1 µF capacitor between the RST lead and ground will effectively hold the lead low long enough to reset the device on powerup, allowing for a cost-effective power-on reset function. Notice that the memory must be reloaded through the serial interface after a hardware reset function. For proper operation, it is necessary for FS and BCLK to be present and stable during a reset. DCLK transitions (frequency is not critical as long as the maximum rate is not exceeded) are also required in order for all internal logic to be properly cleared as is a wait period for the internal PLL to stabilize. See the timing diagram shown in Figure 20 for the proper hardware or power-on reset procedure.

For a software reset, the control memory should not be accessed for a minimum of 256 µs following the reset.

#### Memory Control Mapping

Several memory locations are used to control the device. The Software Interface tables (Table 20, Memory Mapping and Table 21, Control Bit Definition) show the memory assignments that are useful in call processing and system testing. It should be noted that other memory locations are used by the device to hold intermediate results and other device state information. Writing to these other locations can cause serious disruptions in the operation of the device and should be avoided.

### Standby Mode

The device enters a low-power standby mode with powerup or software reset, or by programming the CHACTIVE register 129, bit 0. In standby mode, the control interface is active, capable of writing or reading registers. SLIC read and write data latches are also active. Analog signals at $VF_XI$ and PCM signals at $D_R$ are ignored in this mode. BCLK must be present for proper standby mode operation.

### Test Capabilities

The device has several built-in test capabilities that can be used to verify correct operation of the signal processing of the line card. These test functions are accessed in several different control addresses. Five loopback modes are employed: the first for the digital signal from the PCM bus to be looped back to the PCM bus. This loopback facility can be used to verify correct operation of the PCM bus interface logic, as well as operation of the PCM bus. The second digital loopback function allows complete testing of the digital processing capability of the codec by looping the data back at the analog/digital conversion interface. The third loopback function can be used to check the operation of all the signal processing performed in the device, including the conversions to/from analog. These digital loopback functions can be used with tone generation and reception via the PCM bus.

The first analog loopback facility is at the digital side of the delta-sigma converters and loops analog transmit data back to the analog receive path. The second analog loopback is at the PCM bus interface and loops the transmit data from the line back to the receive path.

By assigning the transmit and receive time slots identically, a loopback arrangement at the PCM bus can be effectively programmed for signals generated on the line side of the codec. This mode is useful for testing from the line side through the entire device.

### SLIC Control Capabilities

Memory locations 158, 159, and 160 are used to control six bidirectional latches that are intended to allow the serial interface to control other line card devices, such as ringing/test switches, telecom electromechanical relays, and SLIC devices. When the TTL latches are configured as outputs, external devices should be set up to sink current from the latch. Location 158 sets the operational mode of these latches as either inputs or outputs. Location 159 specifies what is to be written on the latch leads driven by the device. Location 160 reports the actual state of these leads. It should be noted that a channel control reset forces all of these external leads, except those corresponding to bits 2 and 3, to the high-impedance state, so any inputs connected to bits 0, 1, 4, and 5 should have appropriate pull-up or pull-down resistors (off-chip, if required) to force the external device into a known state at powerup or in the event of a reset. Bits 2 and 3 will reset to outputs with a value of zero.

## Functional Description (continued)

### SLIC Control Capabilities (continued)

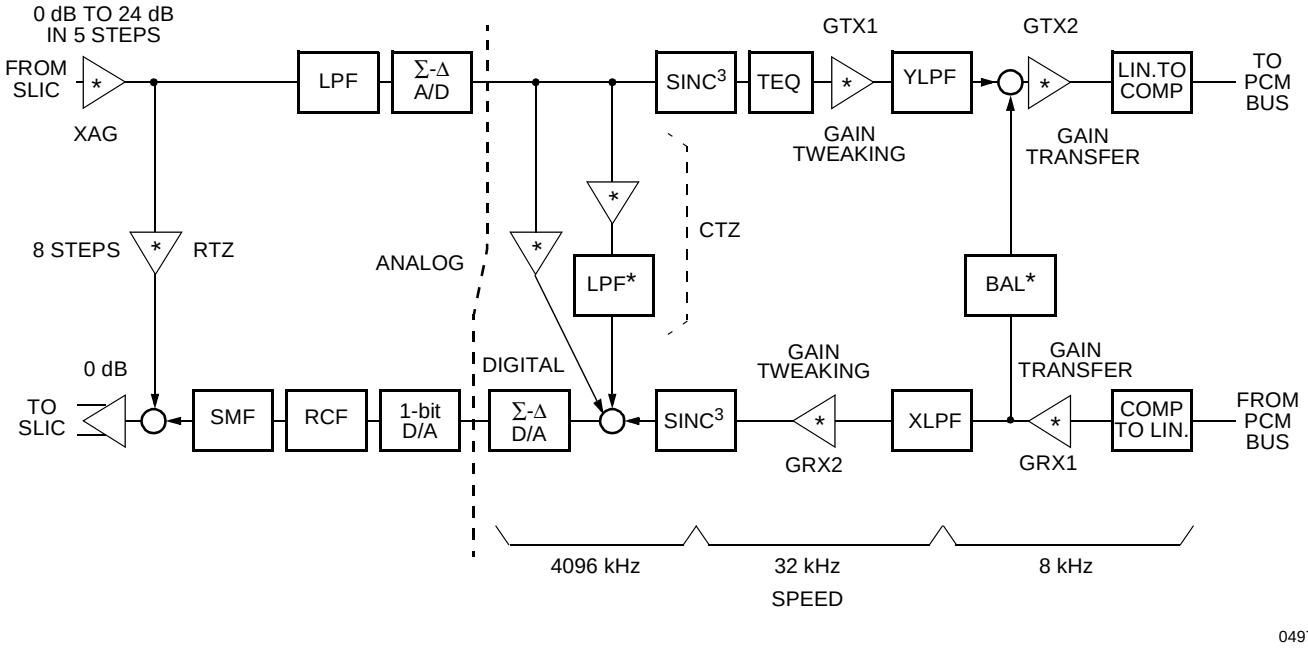
The fast scan mode allows for a minimal data transfer on the serial bus to monitor bits 0 and 1 of the SLIC data memory location (159). If these 2 bits are wired as inputs to the off-hook and/or ring ground detection circuits, a convenient method of rapidly scanning for these two functions is obtained. Bits 2 and 3 default to outputs; thus, they are convenient to provide control of the SLIC state. In any event, all six leads are programmable for maximum flexibility.

### Suggested Initialization Procedures

It is suggested that upon powerup, a hardware reset be used to set the device into a known state. The serial interface should then be used to load the memory addresses that differ from the default values (the write all channels command is convenient for this function). If other devices are controlled by the SLIC data memory location, then it also should be loaded with a known configuration. After the completion of this sequence, the device is ready to be activated. Depending on the application, the next step may either be normal operation or a set of test sequences. After the initialization of the memory, the device and associated line card devices can be controlled by using memory locations 130, 131, 145, 155, 156, 157, 158, 159, and 129; that is, by supplying the PCM bus time-slot addresses, switching the SLIC into the proper mode, and activating the codec. Within memory location 129, the codec would normally be placed into active mode, with both directions of the PCM bus enabled at the start of a call. At the completion of a call, the codec should be placed into standby mode and the PCM bus disabled. Great caution should be used when changing the memory while the codec is in active mode, since termination impedances, balance impedances, and gains may change. These changes are likely to yield undesirable system effects. It is safe to refresh coefficients that are known to be unchanging in the application. It is always possible to read the memory to verify its contents without deleterious effects on codec operation. Normal operation would load the memory and perform all gain adjustments while the codec is in standby mode. Under no circumstances should memory above address 162 be written, since this section of memory is used for state data and intermediate results. Also, all reserved addresses should not be written. Changing this information may have deleterious effects on system operation.

### Signal Processing

Figure 21 details the signal processing functional blocks of one channel of the codec.




* Programmable blocks.

**Figure 21. Internal Signal Processing**

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational section of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Storage Temperature Range | $T_{stg}$ | –55 | 150 | °C |
| Power Supply Voltage (all leads designated power) | $V_{DDX}$ | — | 6.5 | V |
| Negative Voltage on Any Lead with Respect to Ground | $V_{SS}$ | –0.25 | — | V |
| Thermal Resistance, Junction to Ambient: | | | | |
| 68-Pin PLCC[1] | $R_{\Theta JA}$ | — | 43 | °C/W |
| 44-Pin PLCC[1] | $R_{\Theta JA}$ | — | 49 | °C/W |
| 64-Pin TQFP[2] | $R_{\Theta JA}$ | — | 40 | °C/W |
| 100-Pin TQFP[2] | $R_{\Theta JA}$ | — | 30 | °C/W |
| Package Power Dissipation | $P_D$ | — | 1 | W |
| SLIC Control Interface Latches, Current per Device | $I_L$ | — | 160 | mA |

1. Sparse copper, one layer test board.
2. Four layer, JEDEC test board.

## Operating Ranges

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | –40 | 85 | °C |
| Operating Junction Temperature | $T_J$ | –40 | 125 | °C |
| Power Supply Voltage (all leads designated power) | $V_{DDX}$ | 4.75 | 5.25 | V |

## Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. A standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely accepted and can be used for comparison.

| HBM ESD Threshold Voltage | |
|---|---|
| **Device** | **Voltage** |
| T8535/T8536 | > 2000 |

## Electrical Characteristics

For all specifications: $T_A$ = –40 °C to +85 °C, $V_{DD}$ = 5 V ± 5%, unless otherwise noted. Typical values are for $T_A$ = 25 °C and $V_{DD}$ = 5 V. Input signal frequency is 1004 Hz, BCLK = 16.384 MHz, and DCLK = 4.096 MHz, unless otherwise noted.

### dc Characteristics

**Table 10. dc Characteristics**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Low | $V_{IL}$ | All inputs | — | — | 0.8 | V |
| Input Voltage High | $V_{IH}$ | All inputs | 2.0 | — | — | V |
| Input Current | $I_{IL}$ | Digital, without pull-up, inputs, GND < $V_{IN}$ < $V_{DD}$ | –10 | — | 10 | µA |
| | | With internal pull-up, $V_{IN}$ = GND (INTS and RST leads) | –240 | — | 10 | µA |
| | | With internal pull-up, $V_{IN}$ = $V_{DD}$ (INTS and RST leads) | –10 | — | 10 | µA |
| Output Voltage Low: | | | | | | |
| All Outputs | $V_{OL}$ | $I_L$ = 3.2 mA | — | — | 0.4 | V |
| SLIC Controls, Configured as Outputs | $V_{OL}$ | $I_L$ = 24 mA | — | — | 1.0 | V |
| Output Voltage High | $V_{OH}$ | $I_L$ = –320 µA | 3.5 | — | — | V |
| Output Current in High-impedance State | $I_{OZ}$ | — | –30 | — | 30 | µA |
| Line Driver (DX and DO leads) Output Voltage High | $V_{OH}$ | $I_L$ = –10 mA | $V_{DD}$ – 0.5 | — | — | V |
| Line Driver (DX and DO leads) Output Voltage Low | $V_{OL}$ | $I_L$ = 10 mA | — | — | 1.0 | V |

## Electrical Characteristics (continued)

### Analog Interface

The following specifications pertain to the analog SLIC interface for each channel.

**Table 11. Analog Interface**

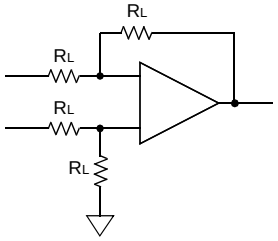
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Resistance | $R_{VFXI}$ | $0.25 < V_{IN} < (V_{DDX} - 0.25)$ V | 100 | — | 300 | kΩ |
| dc Input Voltage | $V_{IX}$ | Relative to ground. Signal should be capacitively coupled to VFxI. | 1.8 | 2.0 | 2.2 | V |
| Load Resistance at VFROP and VFRON (differential) | $R_L$ |  5-8881F | 7.5 | — | — | kΩ |
| Output Resistance | $R_O$ | Digital input code corresponding to idle PCM code (μ-law). | — | 2 | 10 | Ω |
| Output Offset Voltage Between VFROP and VFRON | $V_{OS}$ | Digital input code corresponding to idle PCM code (μ-law). | –100 | 0 | 100 | mV |
| Output Offset Voltage Between VFROP and VFRON, Standby Mode | $V_{OSS}$ | $R_L$ = 100 kΩ | –20 | 0 | 20 | mV |
| Common-mode Output Voltage, Active Mode | $V_{OCM}$ | Digital input code corresponding to alternating ± zero μ-law PCM code. | 1.8 | 2.0 | 2.2 | V |
| Common-mode Output Voltage, Standby Mode | $V_{OCMS}$ | — | 1.7 | 2.0 | 2.3 | V |

**Table 12. Power Dissipation**

Power measurements are made at BCLK = 2.048 MHz, DCLK = 2.048 MHz, no inputs from serial interface, interface latches set as outputs, outputs unloaded.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| All Channels in Standby, Dissipation for One Channel | $I_{DDS}$ | — | — | 21 | 28 | mW |
| One Channel Active, Dissipation for Active Channel | $I_{DD1}$ | — | — | 200 | — | mW |
| Four Channels Active, Dissipation for One Channel | $I_{DD1}$ | — | — | 85 | 125 | mW |

## Electrical Characteristics (continued)

### Gain and Dynamic Range

**Table 13. Gain and Dynamic Range**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Absolute Levels | GAL | Maximum 0 dBm0 levels (1004 Hz): VFXI (encoder milliwatt), all programmable transmit gains set to 0 dB. | — | 2.80 | — | Vp-p |
| | | RCV (decoder milliwatt), termination impedance off, all programmable receive gains set to 0 dB. | — | 5.29 | — | Vp-p |
| Absolute Levels | GAL | Minimum 0 dBm0 levels (1004 Hz): VFXI (encoder milliwatt), XAG = 24 dB, GTX1 = 6 dB, GTX2 = 0 dB. | — | 87.5 | — | mVp-p |
| | | RCV (decoder milliwatt), termination impedance off, GRX1 = 0 dB, GRX2 = –6 dB | — | 2.63 | — | Vp-p |
| Absolute Maximum Voltage Swings | GAL | VFXI | — | — | 3.2 | Vp-p |
| | | VFROP to VFRON (differential) | — | — | 5.28 | Vp-p |
| Transmit Gain Absolute Accuracy | GXA | Transmit gain programmed for maximum 0 dBm0 test level, measured deviation of digital code from ideal 0 dBm0 level at DX digital outputs, with transmit gain set to 0 dB: | | | | |
| | | 20 °C to 70 °C | — | ±0.15 | — | dB |
| | | 0 °C to 85 °C | –0.25 | — | 0.25 | dB |
| | | –40 °C to +85 °C | –0.35 | — | 0.35 | dB |
| Transmit Gain Variation with Programmed Gain | GXAG | Measured transmit gain over the range from maximum to minimum, calculated deviation from the programmed gain relative to GXA at 0 dB, $V_{DD}$ = 5 V. | –0.1 | — | 0.1 | dB |
| Transmit Gain Variation with Frequency, 600 Ω Resistive Source Impedance and Synthesized Termination Impedance | GXAF | Relative to 1004 Hz, minimum gain < GX < maximum gain, VFXI = 0 dBm0 signal, path gain set to 0 dB: | | | | |
| | | f = 16.67 Hz | — | –50 | –30 | dB |
| | | f = 40 Hz | — | –40 | –26 | dB |
| | | f = 50 Hz | — | –40 | –30 | dB |
| | | f = 60 Hz | — | –55 | –30 | dB |
| | | f = 200 Hz | –1.8 | –0.5 | 0 | dB |
| | | f = 300 Hz to 3000 Hz | –0.125 | ±0.04 | 0.135 | dB |
| | | f = 3140 Hz | –0.57 | 0.01 | 0.125 | dB |
| | | f = 3380 Hz | –0.735 | –0.03 | 0.015 | dB |
| | | f = 3860 Hz | — | –9.0 | –8.98 | dB |
| | | f = 4600 Hz and above | — | — | –32 | dB |

## Electrical Characteristics (continued)

### Gain and Dynamic Range (continued)

**Table 13. Gain and Dynamic Range** (continued)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit Gain Variation with Signal Level | GXAL | Sinusoidal test method*, reference level = 0 dBm0: | | | | |
| | | $VF_XI$ = –40 dBm0 to +3 dBm0 | –0.25 | — | 0.25 | dB |
| | | $VF_XI$ = –50 dBm0 to –40 dBm0 | –0.50 | — | 0.50 | dB |
| | | $VF_XI$ = –55 dBm0 to –50 dBm0 | –1.40 | — | 1.40 | dB |
| Receive Gain Absolute Accuracy | GRA | Receive gain programmed to –6 dB, apply 0 dBm0 signal to IPCM, measure $V_{RCV}$, $R_L$ = 100 kΩ differential: | | | | |
| | | 20 °C to 70 °C | — | ±0.15 | — | dB |
| | | 0 °C to 85 °C | –0.25 | — | 0.25 | dB |
| | | –40 °C to +85 °C | –0.30 | — | 0.30 | dB |
| Relative Gain, $VF_ROP$ to $VF_RON$ | — | Digital input 0 dBm0 signal, f = 300 Hz to 3400 Hz. | –0.01 | — | 0.01 | dB |
| Relative Phase, $VF_ROP$ to $VF_RON$ | — | Digital input 0 dBm0 signal, f = 300 Hz to 3400 Hz. | –0.25 | — | 0.25 | Degrees |
| Receive Gain Variation with Programmed Gain | GRAG | Measure receive gain over the range from maximum to minimum setting, calculated deviation from the programmed gain relative to GRA at 0 dB, $V_{DD}$ = 5 V. | –0.1 | — | –0.1 | dB |
| Receive Gain Variation with Frequency, 600 Ω Resistive Termination | GRAF | Relative to 1004 Hz, digital input = 0 dBm0 code, minimum gain < GR < maximum gain, 0 dB path gain: | | | | |
| | | f = below 3000 Hz | –0.125 | ±0.04 | 0.125 | dB |
| | | f = 3140 Hz | –0.57 | ±0.04 | 0.125 | dB |
| | | f = 3380 Hz | –0.735 | –0.550 | 0.015 | dB |
| | | f = 3860 Hz | — | –10.7 | –8.98 | dB |
| | | f = 4600 Hz and above | — | — | –28 | dB |
| Receive Gain Variation with Signal Level | GRAL | Sinusoidal test method*, reference level = 0 dBm0: | | | | |
| | | IPCM digital level = –40 dBm0 to +3 dBm0 | –0.25 | — | 0.25 | dB |
| | | IPCM digital level = –50 dBm0 to –40 dBm0 | –0.50 | — | 0.50 | dB |
| | | IPCM digital level = –55 dBm0 to –50 dBm0 | –1.40 | — | 1.40 | dB |

* Applied to all four channels.

## Electrical Characteristics (continued)

### Noise Characteristics

**Table 14. Per-Channel Noise Characteristics**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit Noise, C-Message Weighted | $N_{XC}$ | 0 dB transmit gain* | — | 10 | 18 | dBrnC0 |
| Transmit Noise, P-Message Weighted | $N_{XP}$ | 0 dB transmit gain* | — | — | –68 | dBm0p |
| Receive Noise, C-Message Weighted | $N_{RC}$ | 0 dB receive gain, digital pattern corresponding to idle PCM code, μ-law*. | — | 10 | 13 | dBrnC0 |
| Receive Noise, P-Message Weighted | $N_{RP}$ | 0 dB receive gain, digital pattern corresponding to idle PCM code, A-law*. | — | — | –75 | dBm0p |
| Noise, Single Frequency | $N_{RS}$ | f = 0 kHz to 100 kHz, loop around measurement, $V_{VFXI}$ = 0 Vrms. | — | — | –53 | dBm0 |
| Power Supply Rejection, Transmit | $PSR_X$ | $V_{DD}$ = 5.0 $V_{DC}$ + 100 mVrms:<br>f = 0 kHz to 4 kHz<br>f = 4 kHz to 50 kHz<br>C-message weighted | <br>36<br>30 | <br>—<br>— | <br>—<br>— | <br>dBC<br>dBC |
| Power Supply Rejection, Receive | $PSR_R$ | Measured on $VF_ROP$,<br>$V_{DD}$ = 5.0 $V_{DC}$ + 100 mVrms:<br>f = 0 kHz to 4 kHz<br>f = 4 kHz to 25 kHz<br>f = 25 kHz to 50 kHz | <br><br>36<br>40<br>36 | <br><br>—<br>—<br>— | <br><br>—<br>—<br>— | <br><br>dBC<br>dBC<br>dBC |
| Spurious Out-of-Band Signals at the Channel Outputs | SOS | 0 dBm0, 300 Hz to 3400 Hz signal applied to $V_{VFXI}$, transmit gain set to 0 dB:<br>4600 Hz to 7600 Hz<br>7600 Hz to 8400 Hz<br>8.4 kHz to 50 kHz | <br>—<br>—<br>— | <br>—<br>—<br>— | <br>–30<br>–40<br>–30 | <br>dB<br>dB<br>dB |

* RTZ and CTZ paths open. All channels active.

## Electrical Characteristics (continued)

### Distortion and Group Delay

**Table 15. Distortion and Group Delay**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal to Total Distortion, Transmit or Receive | $STD_X$<br>$STD_R$ | Sinusoidal test method level:<br>μ-law –30 dBm0 to +3 dBm0<br>A-law –30 dBm0 to +3 dBm0<br>μ-law –40 dBm0 to –30 dBm0<br>A-law –40 dBm0 to –30 dBm0<br>μ-law –45 dBm0 to –40 dBm0<br>A-law –45 dBm0 to –40 dBm0 | <br>36<br>35<br>31<br>30<br>27<br>25 | <br>—<br>—<br>—<br>—<br>—<br>— | <br>—<br>—<br>—<br>—<br>—<br>— | <br>dB<br>dB<br>dB<br>dB<br>dB<br>dB |
| Single Frequency Distortion, Transmit | $SFD_X$ | 0 dBm0 single frequency input, 200 Hz ≤ $f_{IN}$ ≤ 3400 Hz; measured at any other single frequency. | — | — | –46 | dB |
| Single Frequency Distortion, Receive | $SFD_R$ | 0 dBm0 single frequency input, 200 Hz ≤ $f_{IN}$ ≤ 3400 Hz; measured at any other single frequency. | — | — | –46 | dB |
| Intermodulation Distortion | IMD | Transmit or receive, two frequencies in the range of 300 Hz to 3400 Hz. | — | –55 | –49 | dB |
| TX Group Delay, Absolute* | $D_{XA}$ | f = 1600 Hz, 600 Ω resistive termination. | — | — | 475 | μs |
| RX Group Delay, Absolute* | $D_{RX}$ | f = 1600 Hz, 600 Ω resistive termination. | — | — | 235 | μs |

* Absolute group delay is a function of time-slot assignment and the maximum in this table refers to the optimal (minimum group delay) time-slot assignment.

## Electrical Characteristics (continued)

### Crosstalk

**Table 16. Crosstalk**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit to Transmit Crosstalk, 0 dBm0 Level | $CT_{X-X}$ | f = 300 Hz to 3400 Hz, any channel to any channel | — | –95 | –80 | dB |
| Transmit to Receive Crosstalk, 0 dBm0 Level | $CT_{X-R}$ | f = 300 Hz to 3400 Hz, any channel to any other channel<br>In-channel | —<br>— | –100<br>–100 | –80<br>–80 | dB<br>dB |
| Receive to Transmit Crosstalk, 0 dBm0 Level | $CT_{R-X}$ | f = 300 Hz to 3400 Hz, any channel to any other channel<br>In-channel | —<br>— | –100<br>–85 | –80<br>–65 | dB<br>dB |
| Receive to Receive Crosstalk, 0 dBm0 Level | $CT_{R-R}$ | f = 300 Hz to 3400 Hz, any channel to any channel | — | –100 | –80 | dB |

# Timing Characteristics

## Control Interface Timing

### Serial Control Port Timing

**Table 17. Serial Control Port Timing** (see Figure 22 and Figure 23)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{DCLK}$ | Serial Bus Clock Frequency | — | — | — | 4096 | kHz |
| — | Serial Bus Clock Duty Cycle | — | 40 | 50 | 60 | % |
| $t_{CSSETUP}$ | Chip Select Setup Time, Normal Mode | $D_{CLK}$ = 4.096 MHz | 7 | — | — | ns |
| $t_{CSHOLD}$ | Chip Select Hold Time, Normal Mode | $D_{CLK}$ = 4.096 MHz | 4 | — | $t_{DCLK} - t_{CSSETUP}$ | ns |
| $t_{SXDLY}$ | Serial Bus Output Data Delay, Normal Mode | $D_{CLK}$ = 4.096 MHz | — | — | 9 | ns |
| $t_{SDHOLD}$ | Serial Bus Input Data Hold Time, Normal Mode | $D_{CLK}$ = 4.096 MHz | 4 | — | — | ns |
| $t_{SDSETUP}$ | Serial Bus Input Data Setup Time, Normal Mode | $D_{CLK}$ = 4.096 MHz | 7 | — | — | ns |
| $t_{RISE}$ | Clock Edge Rise Time | $D_{CLK}$ = 4.096 MHz | — | — | 12 | ns |
| $t_{FALL}$ | Clock Edge Fall Time | $D_{CLK}$ = 4.096 MHz | — | — | 12 | ns |
| $t_{RISE}$, $t_{FALL}$ | Line Driver Rise/Fall Time (DO output) | $I_L$ = 15 mA, $C_{LOAD}$ = 100 pF | — | — | 30 | ns |
| $t_{CSBHOLD}$ | Chip Select Hold Time, Byte-by-Byte Mode | $D_{CLK}$ = 4.096 MHz | 4 | — | — | ns |
| $t_{SXBDLY}$ | Serial Bus Output Data Delay, Byte-by-Byte Mode | $D_{CLK}$ = 4.096 MHz* | — | — | 9 | ns |
| $t_{CSBSETUP}$ | Chip Select Setup Time, Byte-by-Byte Mode | $D_{CLK}$ = 4.096 MHz | 7 | — | — | ns |
| $t_{SDBHOLD}$ | Serial Bus Data Hold Time, Byte-by-Byte Mode | $D_{CLK}$ = 4.096 MHz | 4 | — | — | ns |
| $t_{SDBSETUP}$ | Serial Bus Data Setup Time, Byte-by-Byte Mode | $D_{CLK}$ = 4.096 MHz | 7 | — | — | ns |
| $t_{CSBHOLD}$ | Chip Select Hold Time, Byte-by-Byte Mode | $D_{CLK}$ = 4.096 MHz | 4 | — | $t_{DCLK} - t_{CSBSETUP}$ | ns |

* The $t_{SXBDLY}$ delay is from either DCLK or CS, whichever transition is later, for the first bit of the byte.

## Timing Characteristics (continued)

### Control Interface Timing (continued)

#### Normal Mode

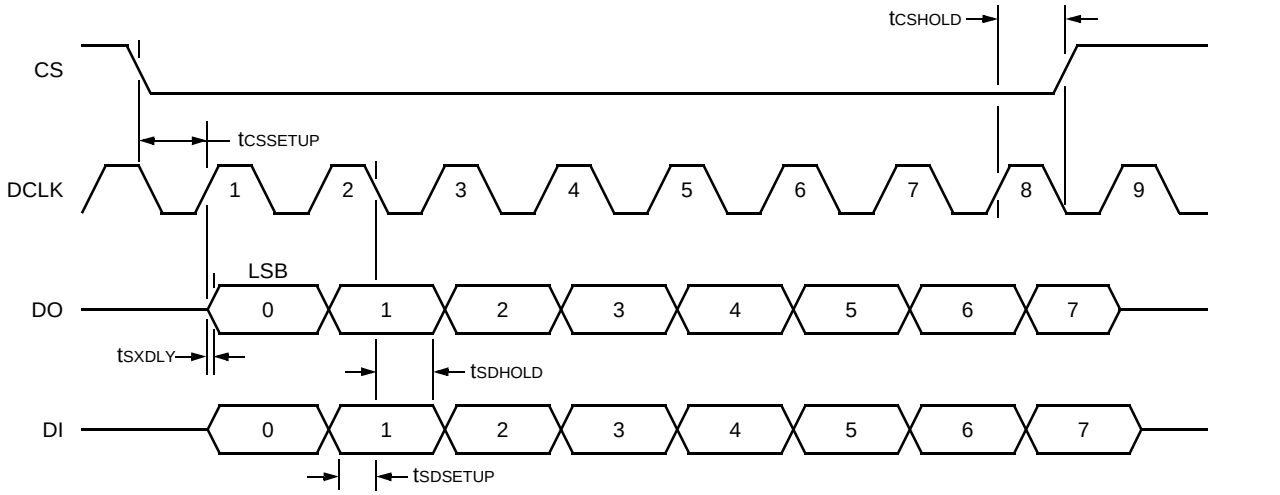



**Figure 22. Serial Interface Timing, Normal Mode (One Byte Transfer Shown)**

#### Byte-by-Byte Mode

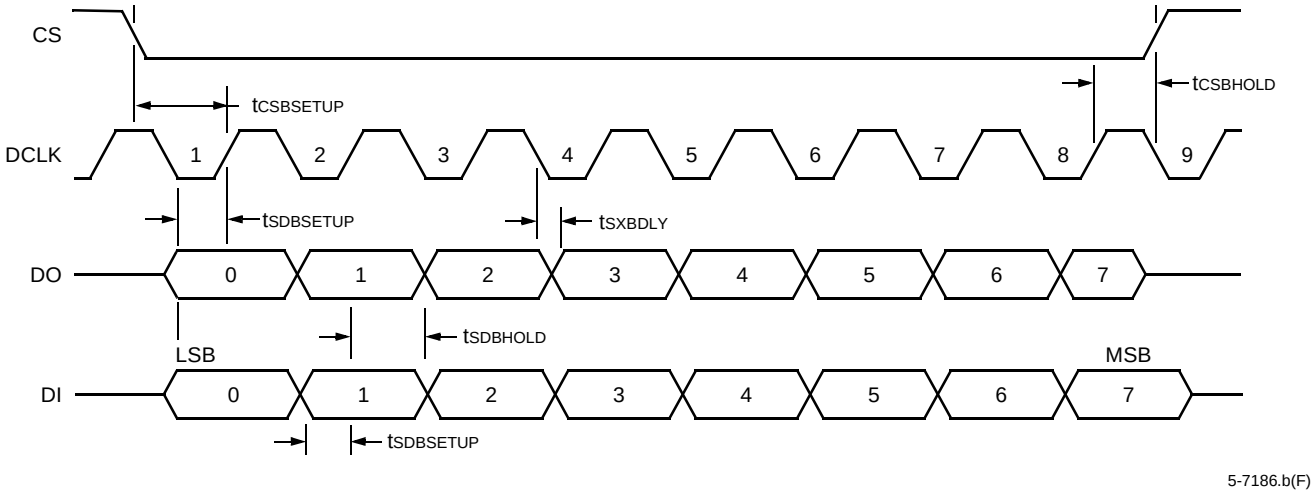



**Figure 23. Byte-by-Byte Mode Timing**

## Timing Characteristics (continued)

### PCM Interface Timing

#### Single-Clocking Mode

Frame sync (FS) signifies the start of frame on the PCM bus for all four channels. FS occurs every 125 µs at an 8 kHz rate. FS must be synchronous with the PCM bus clock (BCLK) and must be high for a minimum of one BCLK period. The PCM interface operates using fixed data rate timing, data timing for both transmit and receive are controlled by BCLK. BCLK can be any value from 512 kHz (eight time slots) to 16.384 MHz (256 time slots) as defined by Table 18.

The PCM bus transfers the most significant bit of the time slot first, consistent with normal telephony practice. Figure 24 shows DX beginning on the rising edge of BCLK and FS and DR being latched on the falling edge of BCLK. Figure 25 shows DX beginning and FS being latched on the rising edge of BCLK and DR being latched on the falling edge of BCLK.

Figure 24 portrays a bit offset of zero, and Figure 25 portrays a transmit bit offset of one and a receive bit offset of two. Bit offset skews the PCM transmit and/or receive data independently from the FS reference. Up to 7 BCLK cycles of bit offset can be employed on a per-channel basis. This flexibility can accommodate special timing requirements. If using the same offset for all channels, simply use the write all channels command.

$\overline{\text{TSX0}}$ or $\overline{\text{TSX1}}$ is active (low) when DX data is transmitting.

**Table 18. PCM Interface Timing: Single-Clocking Mode** (see Figures 24 and 25)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{BCLK}$ | Allowable BCLK Frequencies | — | — | 512 | — | kHz |
| | | — | — | 1024 | — | kHz |
| | | — | — | 1536 | — | kHz |
| | | — | — | 2048 | — | kHz |
| | | — | — | 3072 | — | kHz |
| | | — | — | 4096 | — | kHz |
| | | — | — | 8192 | — | kHz |
| | | — | — | 16384 | — | kHz |
| — | Jitter of BCLK | — | — | — | 100 ns in 100 ms = 1 ppm | — |
| — | BCLK Duty Cycle | — | 40 | 50 | 60 | % |
| $t_{FSSETUP}$ | Frame Strobe Setup Time | $B_{CLK}$ = 16.384 MHz | 7 | — | — | ns |
| $t_{FSHOLD}$ | Frame Strobe Hold Time | $B_{CLK}$ = 16.384 MHz | 4 | — | — | ns |
| $t_{FSWIDTH}$ | Frame Strobe Width | FS synchronous with BCLK | $t_{BCLK}$ | — | 125 µs – $t_{BCLK}$ | — |
| $t_{XDLY}$ | PCM Bus Output Data Delay | $B_{CLK}$ = 16.384 MHz | — | — | 9 | ns |
| $t_{IDHOLD}$ | PCM Bus Input Data Hold Time | $B_{CLK}$ = 16.384 MHz | 4 | — | — | ns |
| $t_{IDSETUP}$ | PCM Bus Input Data Setup Time | $B_{CLK}$ = 16.384 MHz | 7 | — | — | ns |
| $t_{RISE}$ | Clock Edge Rise Time | $B_{CLK}$ = 16.384 MHz | — | — | 8 | ns |
| $t_{FALL}$ | Clock Edge Fall Time | $B_{CLK}$ = 16.384 MHz | — | — | 8 | ns |
| $t_{RISE}$, $t_{FALL}$ | DX Output Rise/Fall Time | $I_L$ = 15 mA, $C_{LOAD}$ = 100 pF | — | — | 30 | ns |
| $t_{DXHIGHZ}$ | DX Output Data Float on TS Exit | $C_{LOAD}$ = 0 | — | — | 5 | ns |
| $t_{TSXDELAY}$ | Line Driver Enable Delay | — | — | — | 5 | ns |
| $t_{TSXHIGHZ}$ | Line Driver Enable Float on TS Exit | — | — | — | 5 | ns |

## Timing Characteristics (continued)

### PCM Interface Timing (continued)

#### Single-Clocking Mode (continued)

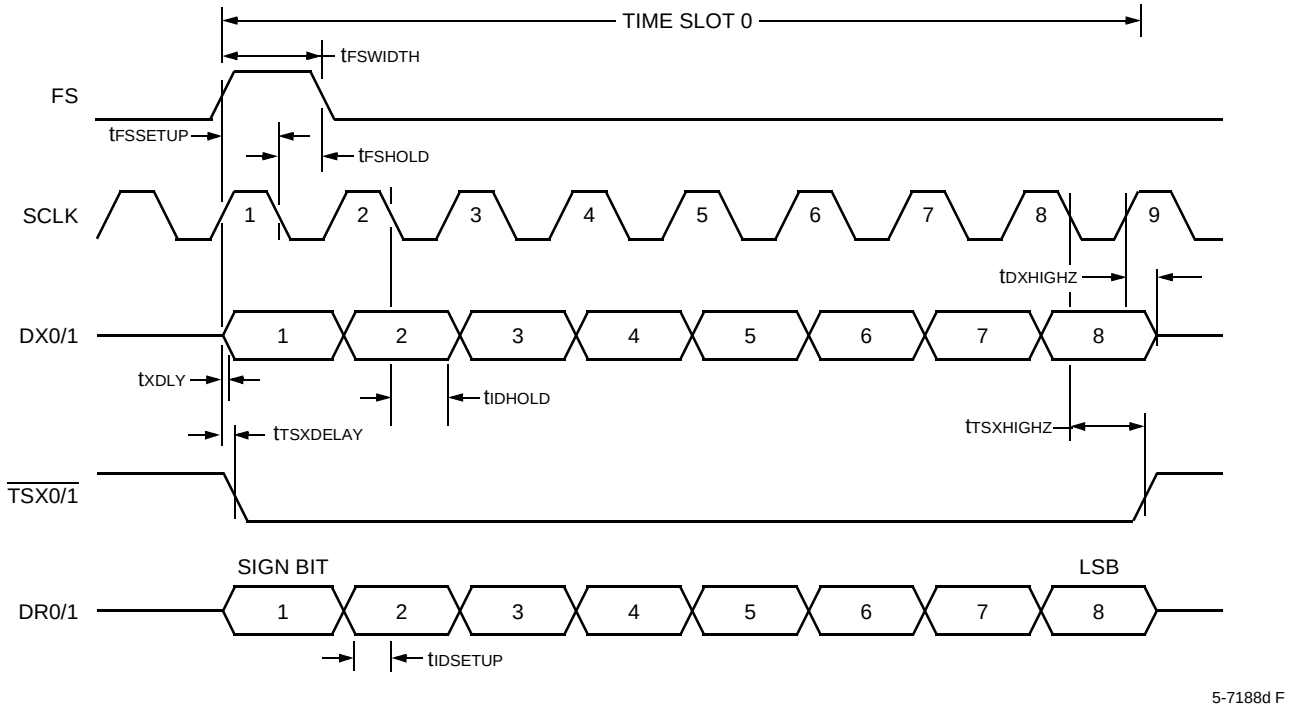



**Figure 24. Single-Clocking Mode (TXBITOFF = 0, RXBITOFF = 0, PCMCTRL2 = 0x00)**

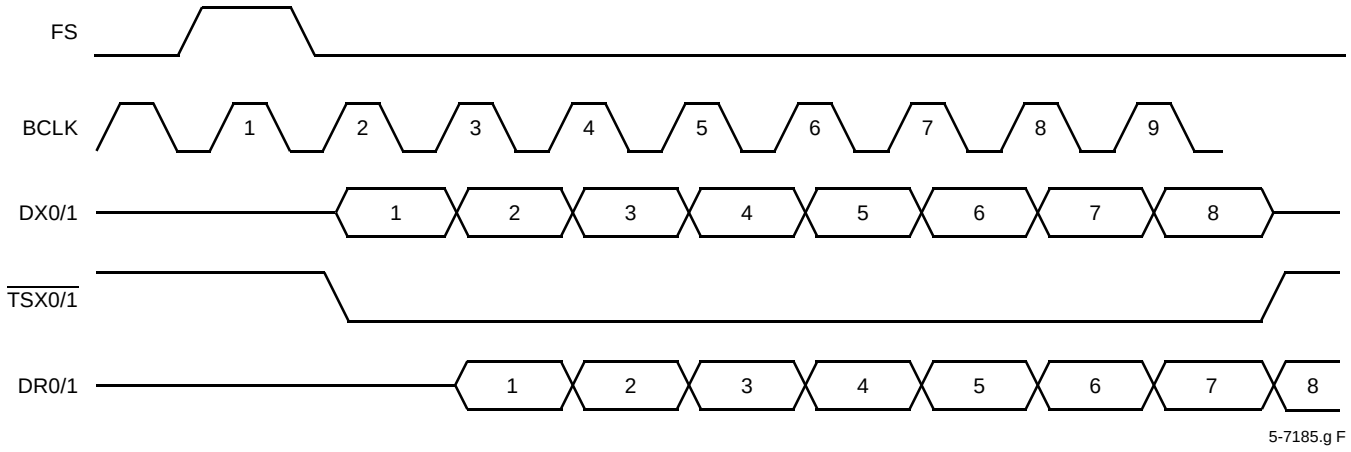



**Figure 25. Single-Clocking Mode (TXBITOFF = 1, RXBITOFF = 2, PCMCTRL2 = 0x01)**

## Timing Characteristics (continued)

### PCM Interface Timing (continued)

#### Double-Clocking Mode

As with the single-clocking mode, FS signifies the start of frame on the PCM bus for all four channels and occurs every 125 µs at an 8 kHz rate. FS must be synchronous with BCLK and must be high for a minimum of one BCLK period. And the PCM interface operates using fixed data rate timing; data timing for both transmit and receive are controlled by BCLK. In double-clocking mode, however, BCLK runs at twice the PCM data rate. BCLK can be any value from 512 kHz (data rate of 256 kbits/s, 4 time slots) to 16.384 MHz (data rate of 8192 kbits/s, 128 time slots) as defined by Table 19.

The PCM bus transfers the most significant bit of the time slot first. In Figure 26, the MSB of receive data is latched on the falling BCLK edge following the first falling BCLK edge that latches FS. Transmit data starts on the first rising edge of BCLK prior to the falling BCLK edge that latches FS.

Figure 26 portrays a bit offset of zero. Like single-clocking mode, bit offset skews the PCM transmit and/or receive data independently from the FS reference. Up to 7 BCLK cycles of bit offset can be employed on a per-channel basis. This flexibility can accommodate special timing requirements. If using the same offset for all channels, simply use the write all channels command.

$\overline{\text{TSX0}}$ or $\overline{\text{TSX1}}$ (not shown in Figure 26) is active (low) when DX data is transmitting.

**Table 19. PCM Interface Timing: Double-Clocking Mode** (see Figure 26)

| Symbol | Parameter | Signal | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| fBCLK | Allowable BCLK Frequencies | — | — | 512 | — | kHz |
| | | — | — | 1024 | — | kHz |
| | | — | — | 1536 | — | kHz |
| | | — | — | 2048 | — | kHz |
| | | — | — | 3072 | — | kHz |
| | | — | — | 4096 | — | kHz |
| | | — | — | 8192 | — | kHz |
| | | — | — | 16384 | — | kHz |
| tBCL | Clock Period | BCLK | 61 | — | 1953 | ns |
| tR, tF | Clock Rise/Fall | BCLK | — | — | 8 | ns |
| tWL, tWH | Pulse Width | BCLK | tBCL x 0.4 | — | tBCL x 0.6 | ns |
| tR, tF | Frame Rise/Fall | FS | — | — | 15 | ns |
| tWFH | Frame Width High | FS | tBCL | — | — | ns |
| tWFL | Frame Width Low | FS | tBCL | — | — | ns |
| tSF | Frame Setup | FS | 7 | — | tBCL – 50 | ns |
| tHF | Frame Hold | FS | 4 | — | — | ns |
| tDDC | Data Delay Clock | DX | — | — | 9 | ns |
| tDDF | Data Delay Frame | DX | — | — | 9 | ns |
| tSD | Data Setup | DR | 7 | — | — | ns |
| tHD | Data Hold | DR | 4 | — | — | ns |

Note: DX load = 150 pF.

## Timing Characteristics (continued)

### PCM Interface Timing (continued)

**Double-Clocking Mode** (continued)

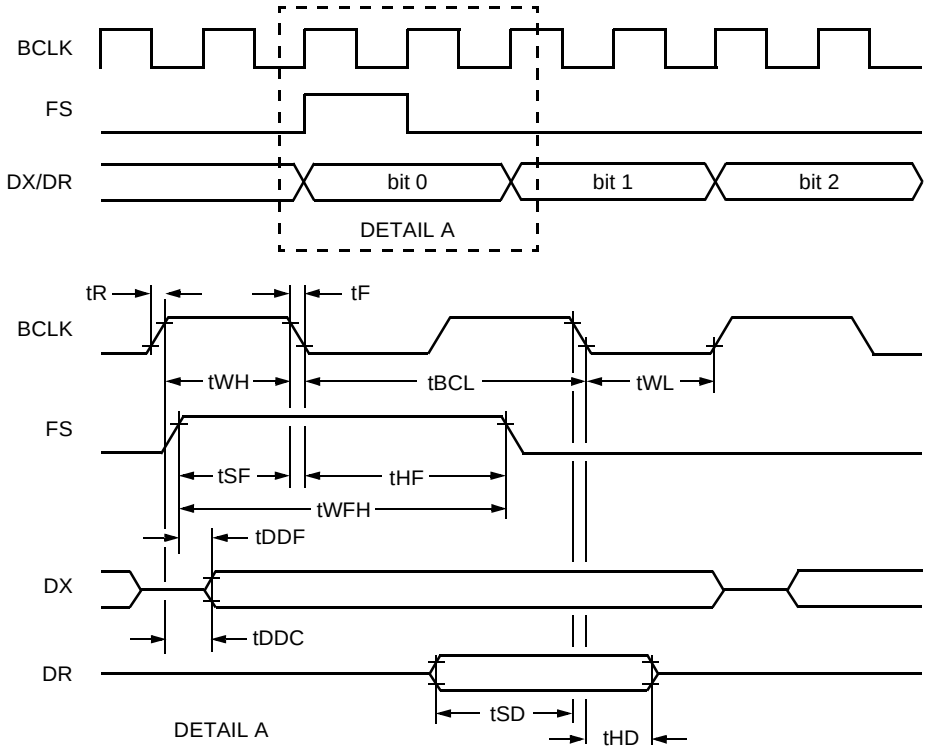



**Figure 26. Double-Clocking Mode (Bit Offset = 0, PCMCTRL2 = 0x00)**

## Software Interface

**Table 20. Memory Mapping**

With the exceptions noted, all of these memory locations may be read to determine the state of the controls contained therein. In the following table, bit 0 is the LSB (transmitted first on the serial interface) and bit 7 is the most significant bit of the byte. Unused bits in an address or multibyte address should be loaded as zero. All of the memory locations can be programmed on a per-channel basis.

Note that the entire coefficient set for a channel (or all four channels) may be loaded with one command.

| Control Name | Address (Decimal) | # of Bits Used | Default Value | Description |
|---|---|---|---|---|
| HBALTAPS | 0—27<br>64—91 | 448 | — | Balance impedance tap coefficients. |
| Reserved | 28—63<br>92—127 | — | — | These addresses have no function. |
| RESCTRL | 128 | 2 | 0x00 | Reset address. Writing a one in the used positions causes a reset as defined by the bit definition. This reset remains in force until the bit is written as a zero. |
| CHACTIVE | 129 | 1 | 0x00 | Standby/Active control. |
| RXBITOFF | 130 | 4 | 0x00 | Bit offset for receive direction. |
| RXOFF | 131 | 8 | 16 * channel # | Time-slot assignment for receive direction. |
| GRX1 | 132 | 11 | 0x0400 | Gain transfer for receive direction. |
| GRX2 | 134—135 | 11 | 0x01ac | Gain tweaking. Control of gain sensitive to impedance and SLIC parameter choices, receive direction. |
| Reserved | 136—139 | — | — | This address has no function. |
| CTZCTRL | 140—143 | 31 | 07ed0000 | CTZ bleed coefficients. |
| Reserved | 144 | — | — | This address has no function. |
| PCMCTRL2 | 145 | 6 | 0x00 | PCM transmission and sampling edge control. |
| SDCTRL | 146 | 7 | 0x19 | RTZ, transmit analog gain (XAG), and digital loopback 3 controls. |
| SDTSI | 147 | 7 | 17 * channel # | Internal time-slot interchanger and loopback controls. Default sets external pins to state referenced in this data sheet. |
| GTX2 | 148—149 | 12 | 0x0400 | Gain tweaking. Control of gain sensitive to impedance and SLIC parameter choices, transmit direction. |
| ZEQTX | 150—152 | 21 | 0x000000 | Transmit line equalization. |
| GTX1 | 153—154 | 12 | 0x051a | Gain transfer for transmit direction. |
| TXBITOFF | 155 | 4 or 5 | 0x00 | Bit offset for transmit direction. |
| TXOFF | 156 | 8 | 16 * channel # | Time-slot assignment for transmit direction. |
| PCMCTRL1 | 157 | 7 | 0x00 | PCM, companding, and loopback controls. |
| SLICTS | 158 | 6 | 0x0c | SLIC 3-state control. Latch I/O. |
| SLICWR | 159 | 6 | 0x00 | Data to be written to the SLIC latches if the corresponding bit is set in the SLICTS control word. |
| SLICRD | 160 | 6 | — | Current actual state of the SLIC leads. This will be the same as SLICWR for those leads configured as outputs. All other positions will reflect the actual state of the external lead. A write operation to this word will be ignored, and within one PCM frame (125 μs), the data will be overwritten. |
| Reserved | 161 | — | — | This address has no function. |
| VERIFY | 162 | 8 | 0x00 | Test address for serial interface verification. |

## Software Interface (continued)

**Table 21. Control Bit Definition**

The following table shows the control bit assignments in the memory control addresses. In all control bit cases, the bit being set places the function into the active mode as defined in the function column.

| Control Name (Address) | Bit Assignment(s) | Function |
|---|---|---|
| HBALTAPS (0—27, 64—91) | 448 | Balance impedance coefficients. Default value is 0x00 for all bytes except for addresses 3 and 5, which are 0x80, and address 69, which is 0x88. |
| RESCTRL (128) | 2—7 | Not used, load as zeros. |
| | 1 | A one resets all other internal states. |
| | 0 | A one resets all control addresses to default values. Note that setting this bit will result in it and all others of this word becoming cleared on the next PCM frame as a normal part of the reset functionality. Alternatively, hardware reset can be used to reset all control and state functions. It is necessary to wait at least 256 µs after asserting this bit before initiating any other serial I/O transactions. |
| CHACTIVE (129) | 1—7 | Load as zeros. |
| | 0 | Active/Standby mode. A zero causes the channel to enter standby (low-power) mode and disables the PCM interface for this channel. A one activates the channel and the corresponding PCM bus interface. Default is zero. |
| RXBITOFF (130) | 5—7 | Receive direction bit offset for the FS signal. Defaults to zero. These 3 bits can be thought of as the least significant bits (RXOFF contains the more significant bits) of a bit counter that determines the location of the first bit of the PCM data from FS. |
| | 0—4 | Load as zeros. |
| RXOFF (131) | 0—7 | Receive time-slot assignment. Defaults to (16 * channel number). Each time slot represents 8 bits. |
| GRX1 (132—133) | 0—10 | Gain adjustment for gain transfer stage in receive direction. Defaults to 0x0400 (0 dB). This is an 11-bit multiply operation with a maximum gain of two (6 dB). 0 dB is the maximum recommended setting. |
| GRX2 (134—135) | 0—10 | Gain adjustment for tweak gain stage in receive direction. Defaults to 0x01ac (−7.58 dB). This is an 11-bit multiply operation with a maximum gain of two (6 dB). 0 dB is the maximum recommended setting. |
| CTZCTRL (140—143) | 0—30 | Coefficients for the CTZ termination bleed. Defaults to 0x07ed0000. |
| PCMCTRL2 (145) | 6—7 | Load as zeros. |
| | 5 | A one selects DX PCM port 1. A zero selects DX PCM port 0. Defaults to zero. PCM port 1 is not available in all package types. |
| | 4 | A one selects DR PCM port 1. A zero selects DR PCM port 0. Defaults to zero. PCM port 1 is not available in all package types. |
| | 3 | A one selects double-clocking mode. Defaults to zero (single-clocking mode). A write to any channel affects all four channels. |
| | 2 | A one starts transmit data on a falling BCLK edge. A zero starts transmit data on a rising BCLK edge. Defaults to zero. A write to any channel affects all four channels. |
| | 1 | A one latches receive data on a rising BCLK edge. A zero latches receive data on a falling BCLK edge. Defaults to zero. A write to any channel affects all four channels. |
| | 0 | A one latches FS on a rising BCLK edge. A zero latches FS on a falling BCLK edge. Defaults to zero. A write to any channel affects all four channels. |

## Software Interface (continued)

**Table 21. Control Bit Definition** (continued)

| Control Name (Address) | Bit Assignment(s) | Function |
|---|---|---|
| SDCTRL (146) | 7 | Load as zero. |
| | 6 | Enable **digital loopback 3**. Defaults to zero (loopback disabled). |
| | 3—5 | RTZ gain. Defaults to 3 (equal level point value of 3 * 0.075 = 0.225). Turn off by writing to zero. |
| | 0—2 | Transmit analog gain (XAG). Defaults to 1 (6 dB) gain. |

| Bit Number | | | Function (dB) |
|---|---|---|---|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | 0.0 |
| 0 | 0 | 1 | 6.02 |
| 0 | 1 | 0 | 12.04 |
| 0 | 1 | 1 | 18.06 |
| 1 | 0 | 0 | 24.08 |

| | | |
|---|---|---|
| SDTSI (147) | 7 | Load as zero. |
| | 6 | Digital loopback, receive to transmit at the sigma-delta converters (**digital loopback 2**). Defaults to zero (no loopback). |
| | 4—5 | Digital channel feeding this analog receive channel. Defaults to channel number. |
| | 3 | Send idle-channel code (alternating bits) to this analog receive path. Defaults to zero (off). |
| | 2 | Loopback from transmit to receive at the sigma-delta converters (**analog loopback 1**). Defaults to zero (no loopback). |
| | 0—1 | Analog channel feeding this digital channel in the transmit direction. Defaults to channel number. |
| GTX2 (148—149) | 0—11 | Gain control for gain transfer stage in transmit direction. Defaults to 0x0400 (0 dB). This is a 12-bit multiply operation with a maximum gain of four (12 dB). |
| ZEQTX (150—152) | 0—20 | Coefficients for the transmit equalization stage. Varies frequency response and accommodates current sensing SLICs. Defaults to 0x000000. |
| GTX1 (153—154) | 0—11 | Gain control for tweak gain stage in transmit direction. Defaults to 0x051a (2.11 dB). This is a 12-bit multiply operation with a maximum gain of four (12 dB). |
| TXBITOFF (155) | 5—7 | Transmit direction bit offset for the FS signal. Defaults to zero. These 3 bits can be thought of as the least significant bits (TXOFF contains the more significant bits) of a bit counter that determines the location of the first bit of the PCM data from FS. |
| | 0—4 | Load as zeros. |
| TXOFF (156) | 0—7 | Transmit time-slot assignment. Defaults to (16 * channel number). Each time slot represents 8 bits. |

## Software Interface (continued)

**Table 21. Control Bit Definition** (continued)

| Control Name (Address) | Bit Assignment(s) | Function |
|---|---|---|
| PCMCTRL1 (157) | 7 | 3-state transmit PCM interface. Defaults to zero. A one forces the PCM interface into a high-impedance state during its assigned time-slot on the PCM bus. Placing the channel in standby mode also forces a high-impedance condition on the transmit interface. |
| | 6 | Transmit zeros instead of data. Defaults to zero (off). |
| | 5 | Load as zero. |
| | 4 | Place idle-channel code on receive path. Defaults to zero (off). |
| | 3 | Loopback receive to transmit at PCM conversion interface (**digital loopback 1**). Resets to zero. |
| | 2 | Loopback transmit to receive at PCM conversion interface (**analog loopback 2**). Resets to zero. |
| | 1 | Reserved. Must be programmed to zero. Defaults to zero. |
| | 0 | μ-law or A-law. A one sets A-law mode, and a zero sets μ-law mode. Defaults to zero (μ-law). |
| SLICTS (158) | 6—7 | Load as zeros. |
| | 0—5 | Controls the drivers for the corresponding SLIC latches. A one enables the lead as an output. Defaults to 0x0C (bits 2 and 3 set, the rest cleared). |
| SLICWR (159) | 6—7 | Load as zeros. |
| | 0—5 | SLIC data latches. If the corresponding bit in the SLICTS address is set for an output, the device will drive the corresponding bit according to the contents of this address. Default is zero. |
| SLICRD (160) | 6—7 | Not used, ignore on read. |
| | 0—5 | Reports the actual state of the SLIC leads. Anything written to this address is ignored, and within one PCM frame (125 μs), the data will be overwritten. |
| VERIFY (162) | 0—7 | Test location for serial interface. This location has no internal use, but merely latches write data for the purpose of testing the serial interface. |

## Applications

The following reference circuit shows a complete schematic for interfacing to the Lucent L9215G SLIC. All ac parameters are programmed by the T8536. Note that this implementation differentiates itself in that no external components are required in the ac interface to provide a dc termination impedance or for stability. For illustration purposes, 0.5 Vrms PPM injection was assumed in this example and no meter pulse rejection is used. Also, this example illustrates the device using programmable overhead and current limit.

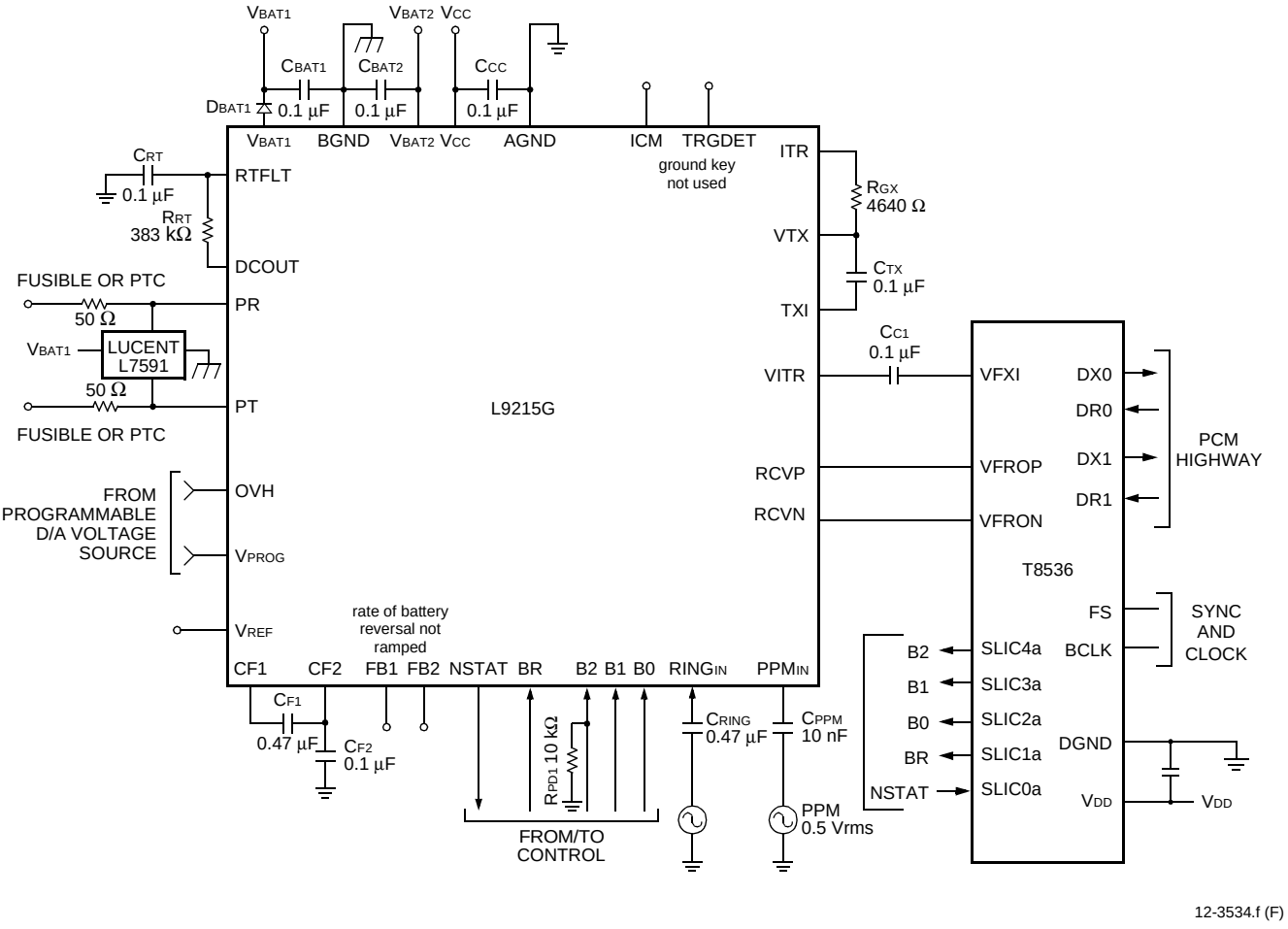


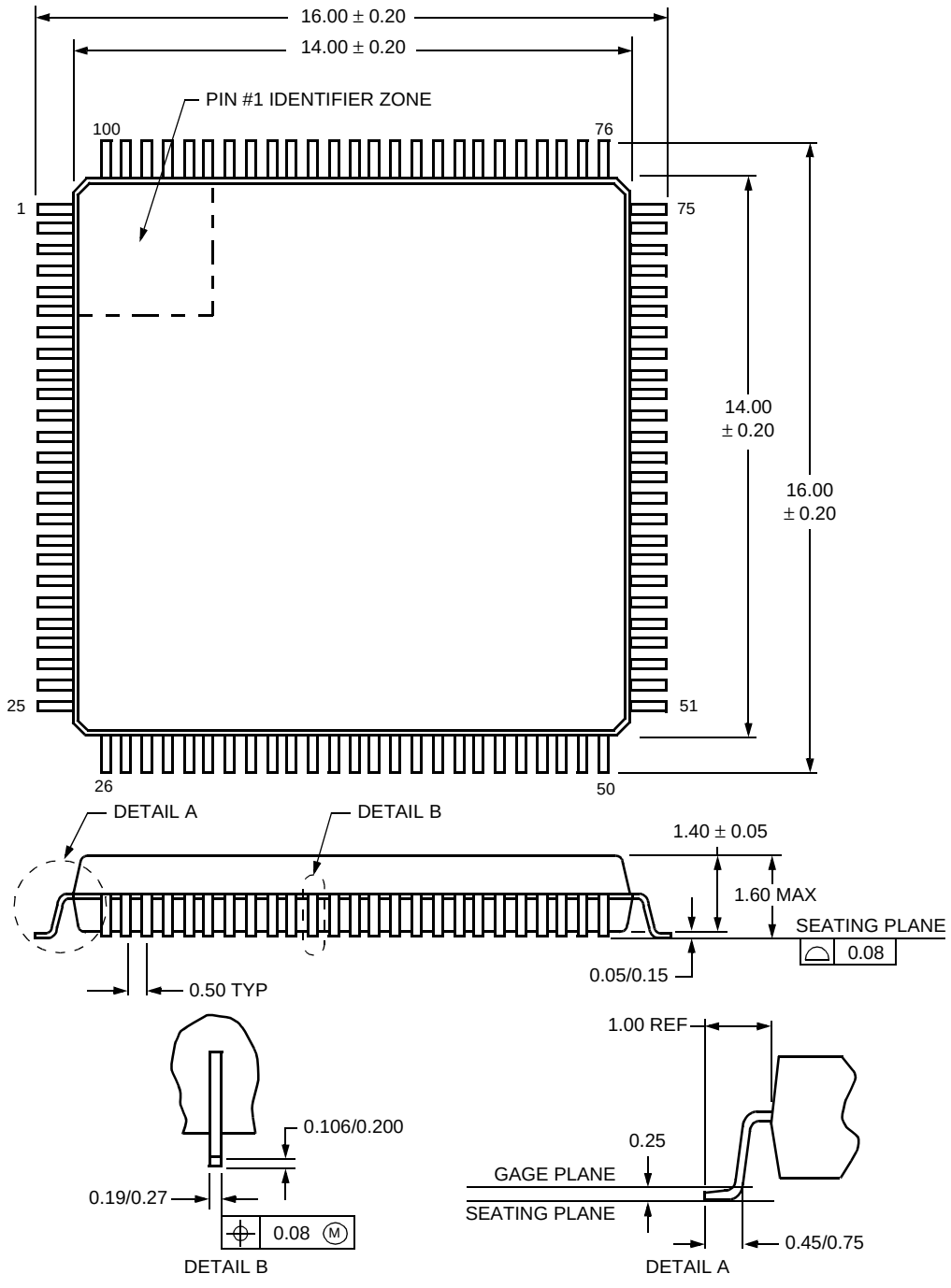

**Figure 27. POTS Interface**

## Outline Diagrams

### 100-Pin TQFP

Dimensions shown are in millimeters.

**Note:** The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.



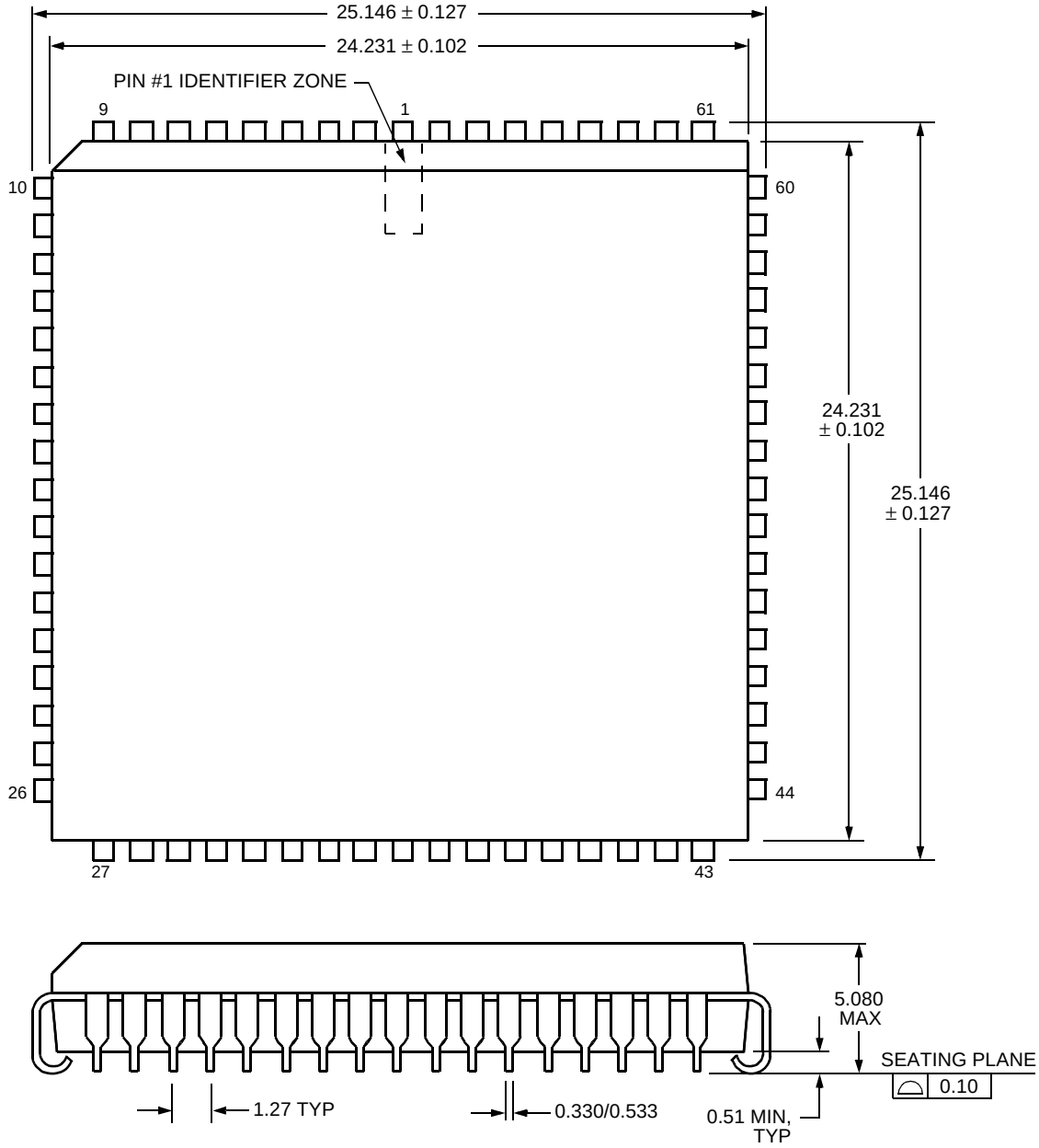

5-2146F

## Outline Diagrams (continued)

### 68-Pin PLCC

Dimensions shown are in millimeters.

**Note:** The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.



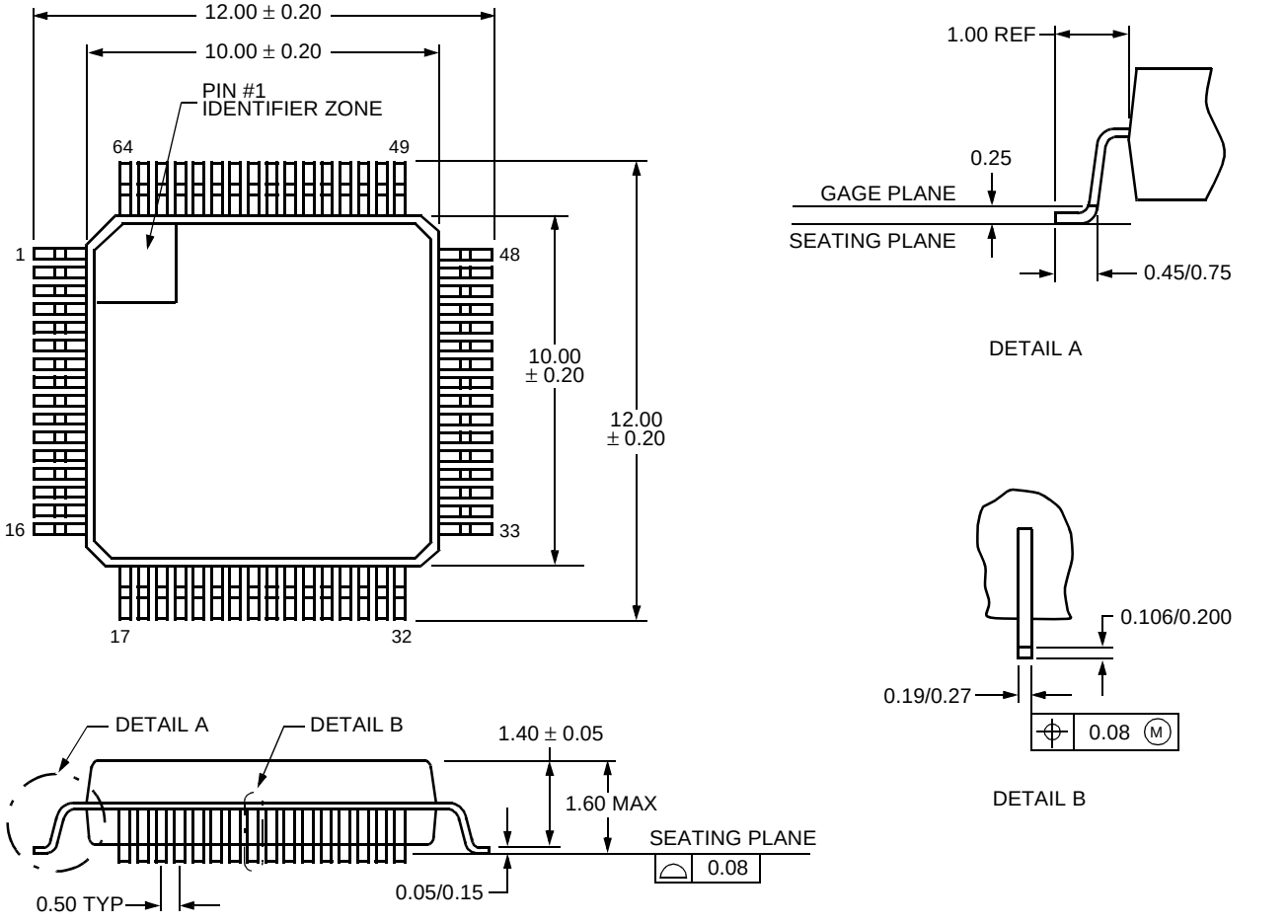

5-2139

## Outline Diagrams (continued)

### 64-Pin TQFP

Dimensions shown are in millimeters.

**Note:** The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.



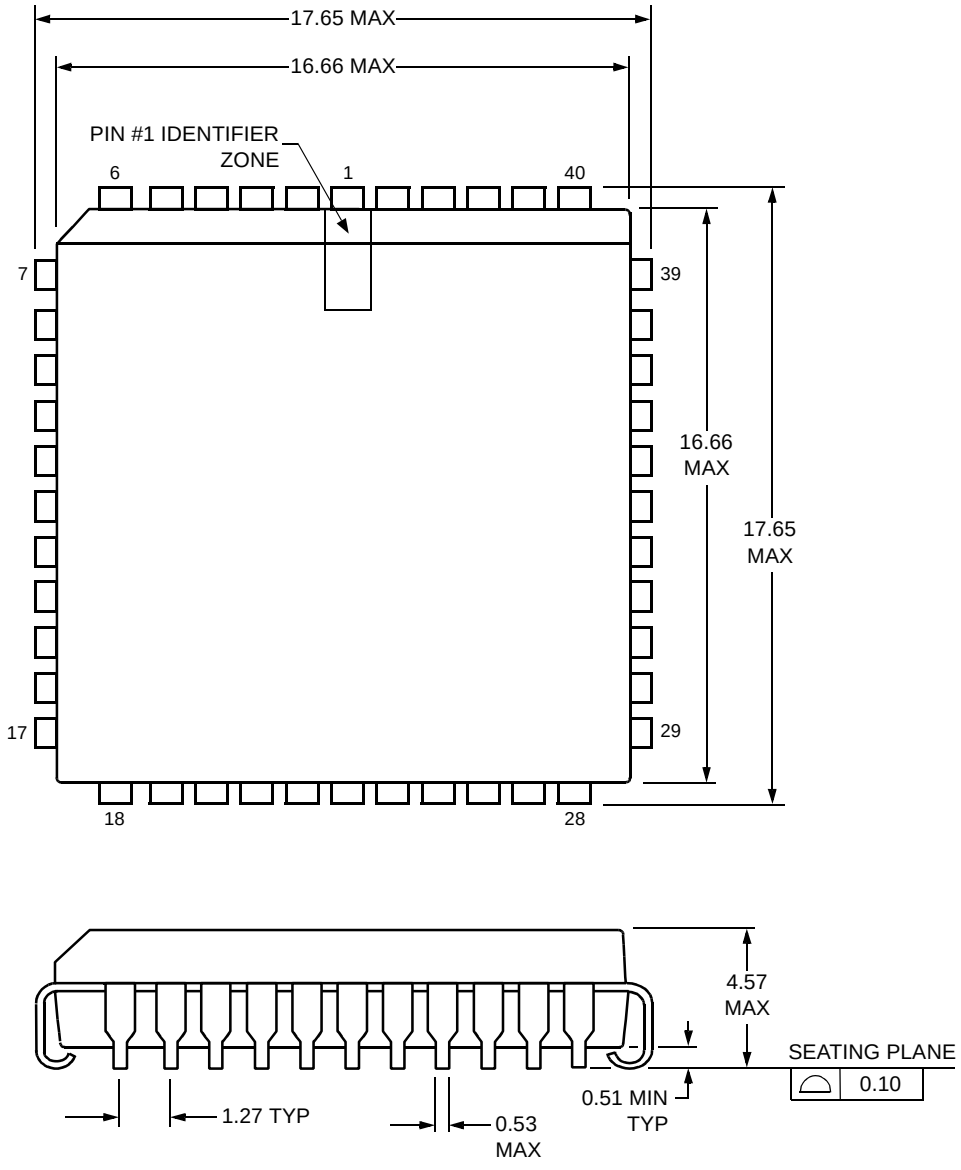

5-3080

## Outline Diagrams (continued)

### 44-Pin PLCC

Dimensions are in millimeters.

**Note:** The dimensions in this outline diagram are intended for informational purposes only. For detailed footprint drawings to assist your design efforts, please contact your Lucent Technologies Sales Representative.




5-2506(F)

## Ordering Information

| Device Code | Package | Temperature | Comcode |
|---|---|---|---|
| T-8535 - - - ML-D | 44-Pin PLCC<br>Dry-bagged | –40 °C to +85 °C | 108420472 |
| T-8536 - - - ML-D | 68-Pin PLCC<br>Dry-bagged | –40 °C to +85 °C | 108420506 |
| T-8536 - - - ML-DT | 68-Pin PLCC<br>Tape & Reel<br>Dry-bagged | –40 °C to +85 °C | 108420514 |
| T-8536 - - 1TL-DB | 100-Pin TQFP<br>Dry Pack Tray | –40 °C to +85 °C | 108558511 |
| T-8536 - - 1TL-DT | 100-Pin TQFP<br>Tape & Reel<br>Dry-bagged | –40 °C to +85 °C | 108760091 |
| T-8536 - - - TL-DB | 64-Pin TQFP<br>Dry Pack Tray | –40 °C to +85 °C | 108420498 |

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