TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6LE2

Gate Driver for TFT LCD Panels

The T6LE2 is a 300 / 263 / 256-channel output gate driver for TFT LCD panels.

Unit: mm

T6LE2	User Area Pitch	
	IN	OUT

Please contact Toshiba or a distributor for the latest COF specification and product line-up.

COF (Chip On Film)

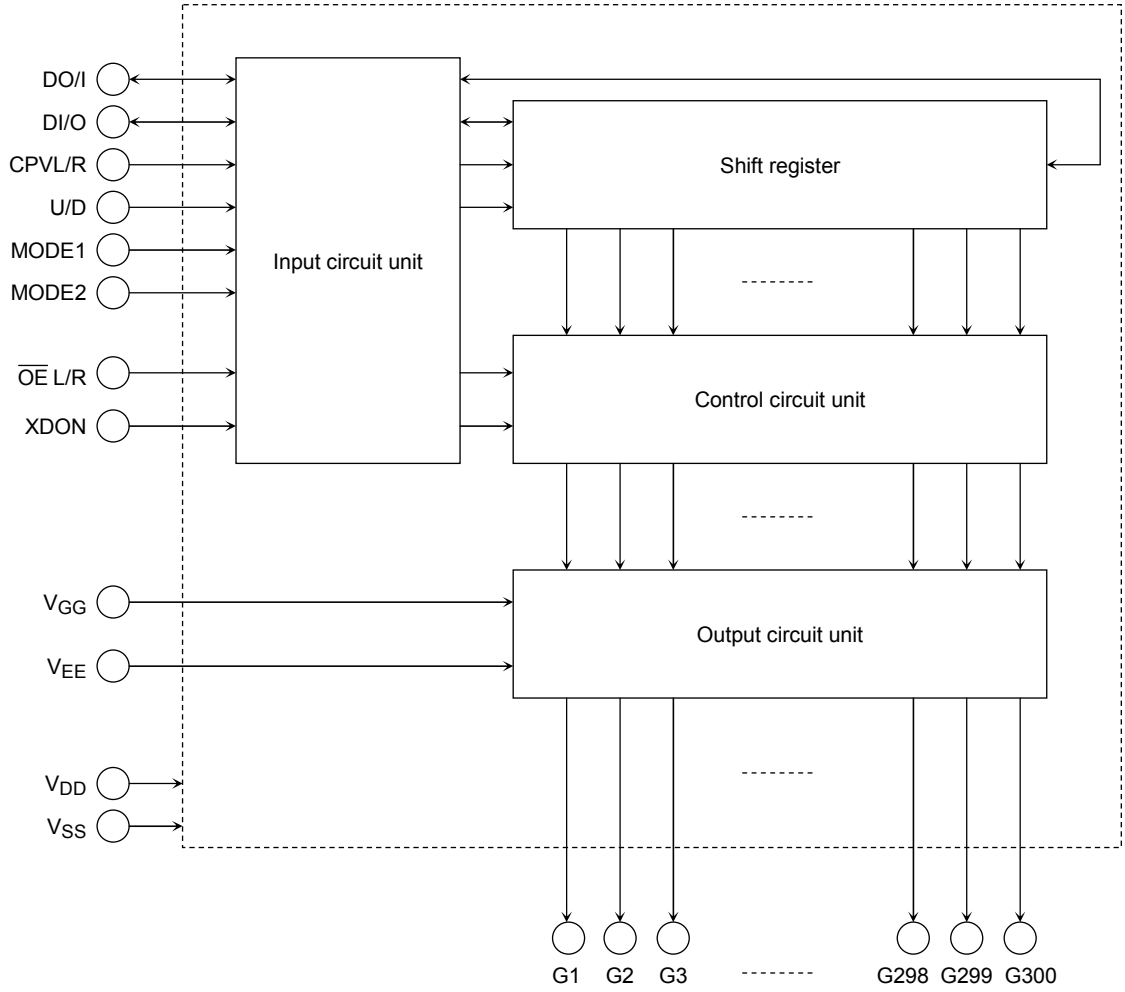
Features

- LCD drive output pins : Switchable 300 / 263 / 256 pins
- LCD drive voltage : max 43.5 V
- Data transfer method : Bidirectional shift register
- Operating temperature : −20 to 75°C
- Package : COF

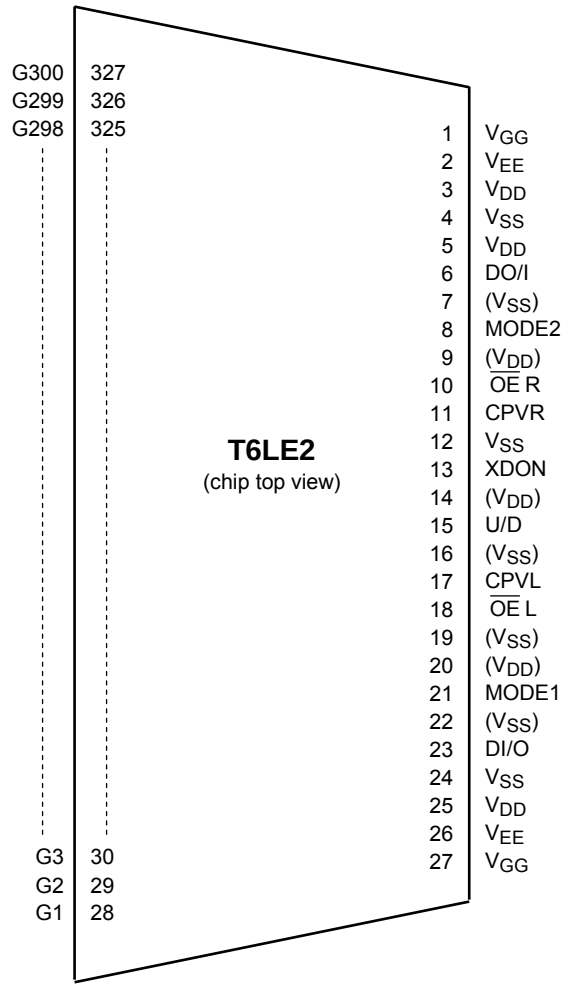
Application

Module for PC monitors, LCDs for TV and Module for amusement

Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest COF specification.

Pin Function

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>
Vertical shift clock, output enable input / output select pin
These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below.
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
• When set for input
This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPVL/R.
• When set for output
When two or more T6LE2 are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPVL/R.
</td></tr>
<tr><td>U/DL
U/DR</td><td>I/O</td><td>
Transfer direction select / vertical shift clock, output enable input / output select pin
This pin specifies the direction in which data is transferred through the shift registers.
The shift register data is shifted synchronously with the rising edge of CPV as follows:
When U/D is high, data is shifted in the direction
U/D = “H”: G1 → G2 → G3 → G4 → ··· → G300
When U / D is low, the direction is reversed to give
U/D = “L”: G300 → G299 → G298 → G297 → ··· → G1
This pin is used to perform input / output settings for CPVL, CPVR, $\overline{OE}$ L, $\overline{OE}$ R.
<table>
<tr><th>U/D</th><th>Input</th><th>Output</th></tr>
<tr><td rowspan="2">L</td><td>CPVR</td><td>CPVL</td></tr>
<tr><td>$\overline{OE}$ R</td><td>$\overline{OE}$ L</td></tr>
<tr><td rowspan="2">H</td><td>CPVL</td><td>CPVR</td></tr>
<tr><td>$\overline{OE}$ L</td><td>$\overline{OE}$ R</td></tr>
</table>
The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD}) or low (V_{SS}).
</td></tr>
<tr><td>CPVL
CPVR</td><td>I/O</td><td>
Vertical shift clock
• When set for input:
This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPVL/R.
• When set for output:
The signal input to CPVL/R is output to CPVR/L asynchronous to other signals.
These pins are switched between input and output by setting the U/D pin as below.
<table>
<tr><th>U/D</th><th>CPVL</th><th>CPVR</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
</td></tr>
<tr><td>$\overline{OE}$ L
$\overline{OE}$ R</td><td>I/O</td><td>
Output enable pin
When set for input:
These signals control the data appearing at the LCD panel drive pins (G1 through G300).
$\overline{OE}$ L/R doesn’t synchronize with the CPVL/R.
When $\overline{OE}$ L/R is low : outputs shift data and data contents.
When $\overline{OE}$ L/R is high : controls the LCD panel drive output to V_{EE} level.
When set for output:
The signal input to $\overline{OE}$ L/R is output to $\overline{OE}$ R/L.
These pins are switched between input and output by setting the U/D pin as below.
<table>
<tr><th>U/D</th><th>$\overline{OE}$ L</th><th>$\overline{OE}$ R</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>MODE1
MODE2</td><td>I</td><td>Output channels select pins
This signal selects 300 / 263 / 256-pin mode for the LCD panel driver.
<table>
<tr><th>MODE1</th><th>MODE2</th><th>LCD drive output pins</th><th>Non-output pins</th></tr>
<tr><td>H</td><td>H</td><td>300-out</td><td>—</td></tr>
<tr><td>H</td><td>L</td><td>263-out</td><td>G133 to G169 (V_{EE} level)</td></tr>
<tr><td>L</td><td>H</td><td>256-out</td><td>G129 to G172 (V_{EE} level)</td></tr>
<tr><td>L</td><td>L</td><td></td><td>—</td></tr>
</table></td></tr>
<tr><td>XDON</td><td>I</td><td>Display-ON input pin
When XDON = low, the V_{GG} voltage is output all output pins irrespective of the shift data and the content of input data. After, the contents of the shift registers becomes unfixed the data.
XON operates asynchronously with CPV. This pin is pulled-up to the V_{DD}.
Since all LCD drive outputs output (G1 to G300) the V_{GG} level, much current may generate them momentarily.
When 263 / 256-pin mode, unapplied LCD panel drive pins fixed V_{EE}.
The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD}) or low (V_{SS}).</td></tr>
<tr><td>G1 to G300</td><td>O</td><td>LCD panel drive pins
These pins output the shift register data or the voltage of V_{GG} or V_{EE} depending on the control signals $\overline{OE}$ and XDON.</td></tr>
<tr><td>V_{GG}</td><td>—</td><td>Power supply for LCD drive</td></tr>
<tr><td>V_{EE}</td><td>—</td><td>Power supply for LCD drive</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for the internal logic
The (V_{DD}) is the MODE1, MODE2 and U/D pin for connection.</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Power supply for the internal logic
The (V_{SS}) is the MODE1, MODE2 and U/D pin for connection.</td></tr>
</table>

Device Operation

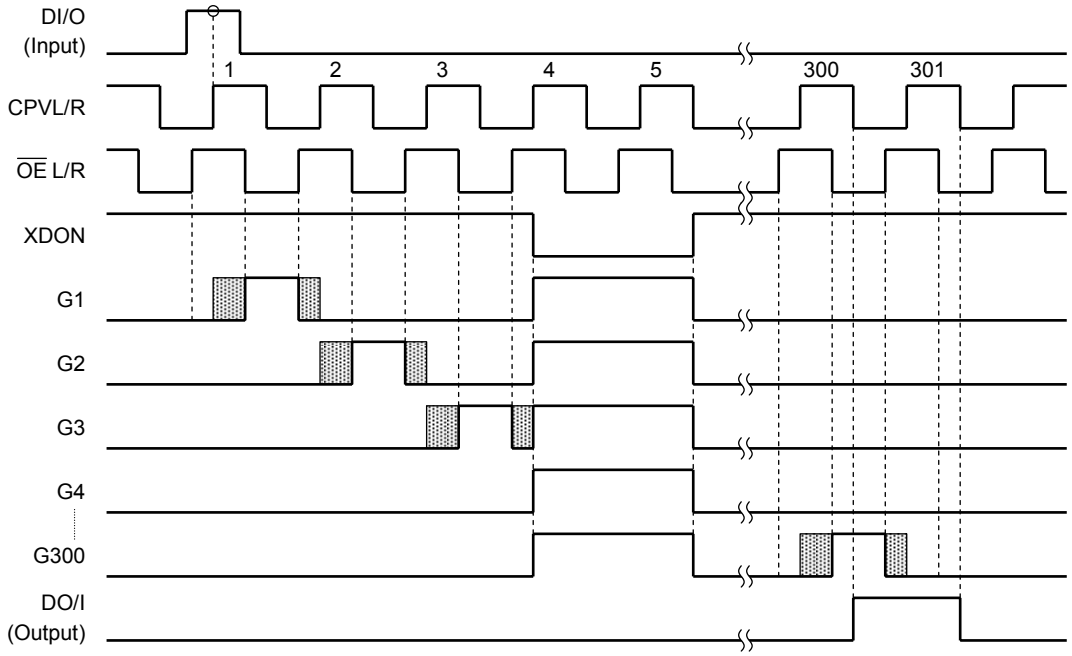
- **Shift data transfer method**

MODE1	MODE2	Output Mode	U/D Pin	Shift Data		Data Transfer Method
				Input	Output	
H	H	300-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ··· → G300
			L	DO/I	DI/O	G300 → G299 → G298 → ··· → G1
H	L	263-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ··· → G132 → G170 → ··· → G300
			L	DO/I	DI/O	G300 → G299 → G298 → ··· → G170 → G132 →··· → G1
L	H	256-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ··· → G128 → G173 → ··· → G300
			L	DO/I	DI/O	G300 → G299 → G298 → ··· → G173 → G128 →··· → G1
L	L	Don't use				

The input data (DI/O or DO/I) is latched into the internal register synchronously with the rising edge of the shift clock CPV. At the same time that the data is shifted to the next register at the next rise of CPV, new vertical shift data is latched into.

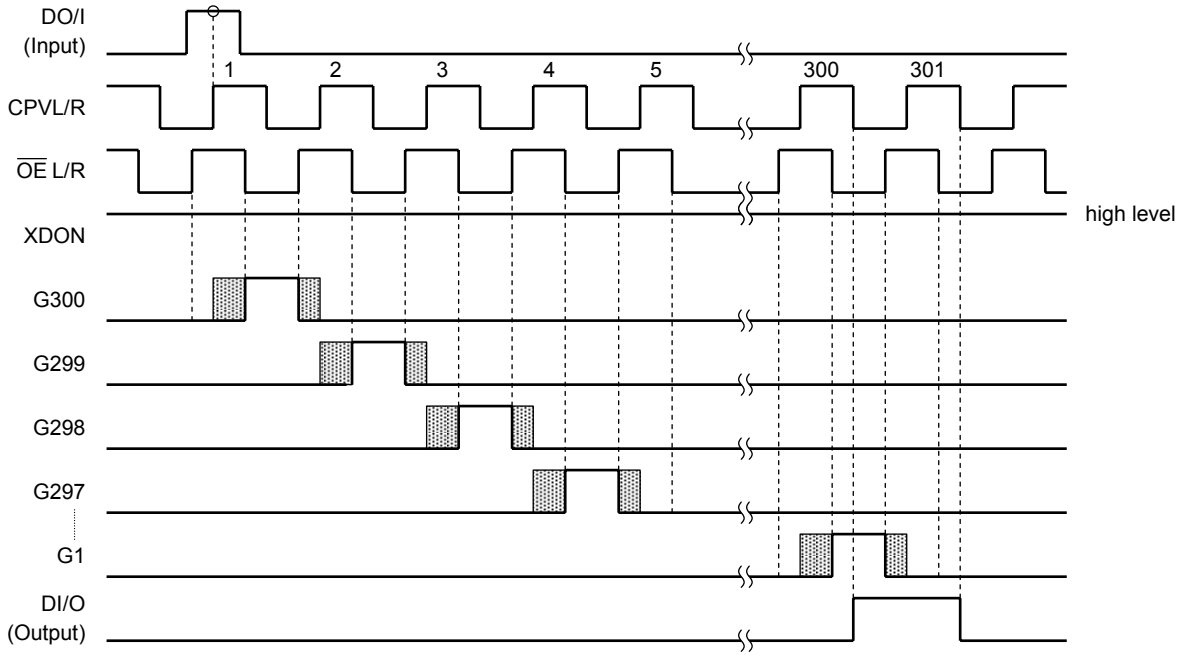
In the output operation, the data in the last shift register (G300 or G1) is output synchronously with the falling edge of CPV. (The output high voltage is the V_{DD} level; the output low voltage is the V_{SS} level.)

Timing Diagram 1
(300-out mode, U/D = high level, MODE1 = high level, MODE2 = high level)



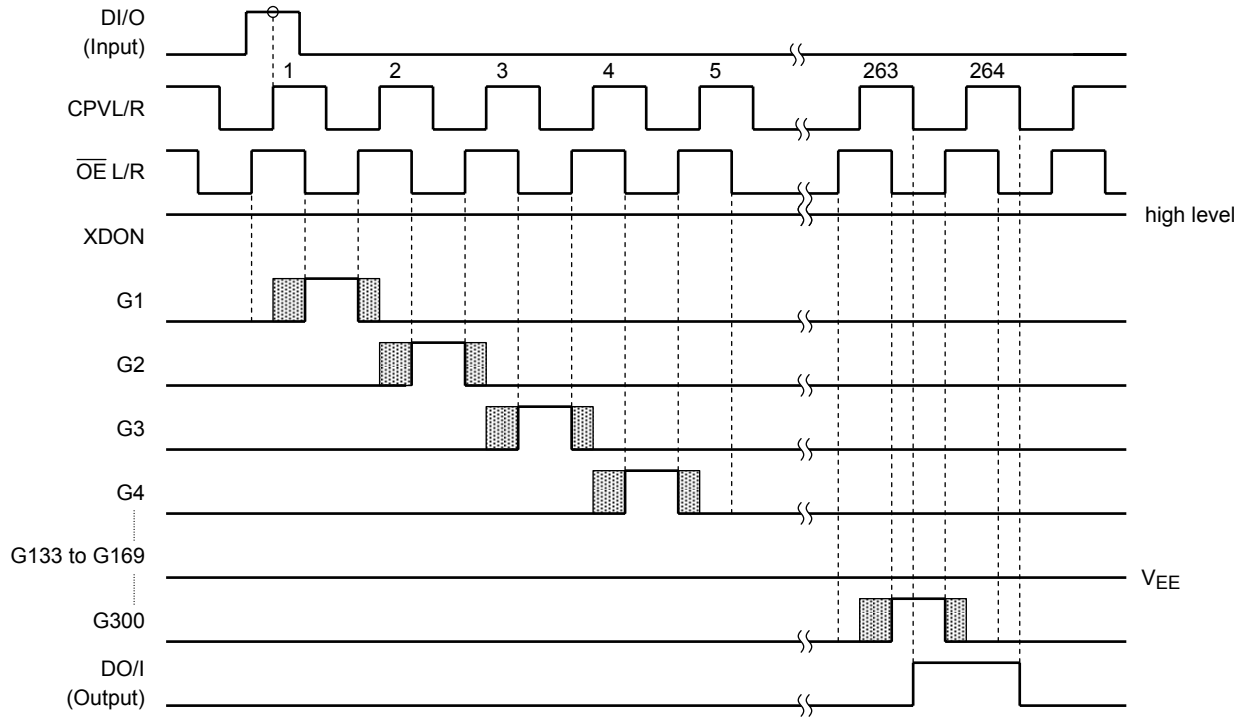
: This part is output which is controlled (fixed to V_{EE}) by $\overline{OE}$ pin

Timing Diagram 2
(300-out mode, U/D = low level, MODE1 = high level, MODE2 = high level)



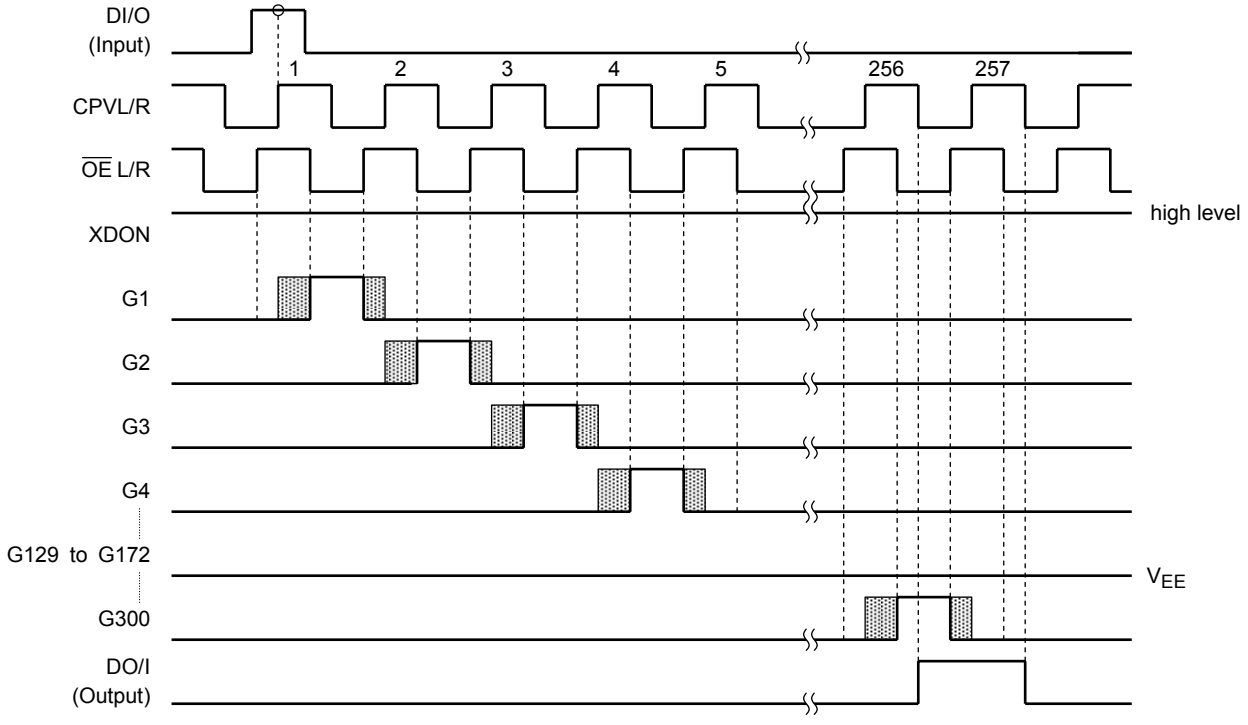
: This part is output which is controlled (fixed to V_{EE}) by $\overline{OE}$ pin

Timing Diagram 3
(263-out mode, U/D = high level, MODE1 = high level, MODE2 = low level)



: This part is output which is controlled (fixed to V_{EE}) by $\overline{OE}$ pin

Timing Diagram 4
(256-out mode, U/D = high level, MODE1 = low level, MODE2 = high level)



: This part is output which is controlled (fixed to V_{EE}) by $\overline{OE}$ pin

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	−0.3 to 4.0	V
Supply voltage (2)	V_{GG}	−0.3 to 48.0	
Supply voltage (3)	V_{EE}	−20.0 to 0.3	
Supply voltage (4)	$V_{GG} - V_{EE}$	−0.3 to 45.0	
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	
Storage temperature	T_{stg}	−55 to 125	°C

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	2.3 to 3.6	V
Supply voltage (2)	V_{GG}	10 to 35	
Supply voltage (3)	V_{EE}	−15 to −5	
Supply voltage (4)	$V_{GG} - V_{EE}$	15.0 to 43.5	
Operating temperature	T_{opr}	−20 to 75	°C
Operating frequency	f_{CPV}	150 (max)	kHz
Output Load capacitance	C_L	300 (max)	pF/PIN

Electrical Characteristics

DC Characteristics
($V_{GG} - V_{EE}$ = 30.0 to 43.5 V, V_{DD} = 2.3 to 3.6 V, V_{SS} = 0 V, Ta = −20 to 75°C)

Parameter		Symbol	Test circuit	Test Conditions	Min	Max	Unit	Relevant
Input voltage (1)	Low Level	V_{IL1}	—	—	V_{SS}	$0.3 \times V_{DD}$	V	(Note1)
	High Level	V_{IH1}		—	$0.7 \times V_{DD}$	V_{DD}		
Input voltage (2)	Low Level	V_{IL2}	—	—	V_{SS}	$(0.3 \times V_{DD})$	V	XDON
	High Level	V_{IH2}		—	$(0.7 \times V_{DD})$	V_{DD}		
Output voltage	Low Level	V_{OL}	—	I_{OL} = 40 μA	V_{SS}	V_{SS} + 0.4	V	DI/O DO/I
	High Level	V_{OH}		I_{OH} = −40 μA	V_{DD} − 0.4	V_{DD}		
Output resistance	Low Level	R_{OL}	—	$V_{OUT} = V_{EE}$ + 0.5 V	—	1000	Ω	G1 to G300
	High Level	R_{OH}		$V_{OUT} = V_{GG}$ − 0.5 V				
Input leakage current		I_{IN1}	—	—	−1	1	μA	(Note1)
		I_{IN2}		$V_{IN} = V_{DD}$	−1	1		XDON
Current consumption (1)		I_{GG}	—	no load (Note2)	—	T.B.D.	μA	V_{GG}
Current consumption (2)		I_{DD}			—	T.B.D.		V_{DD}
Current consumption (3)		I_{EE}			—	T.B.D.		V_{EE}

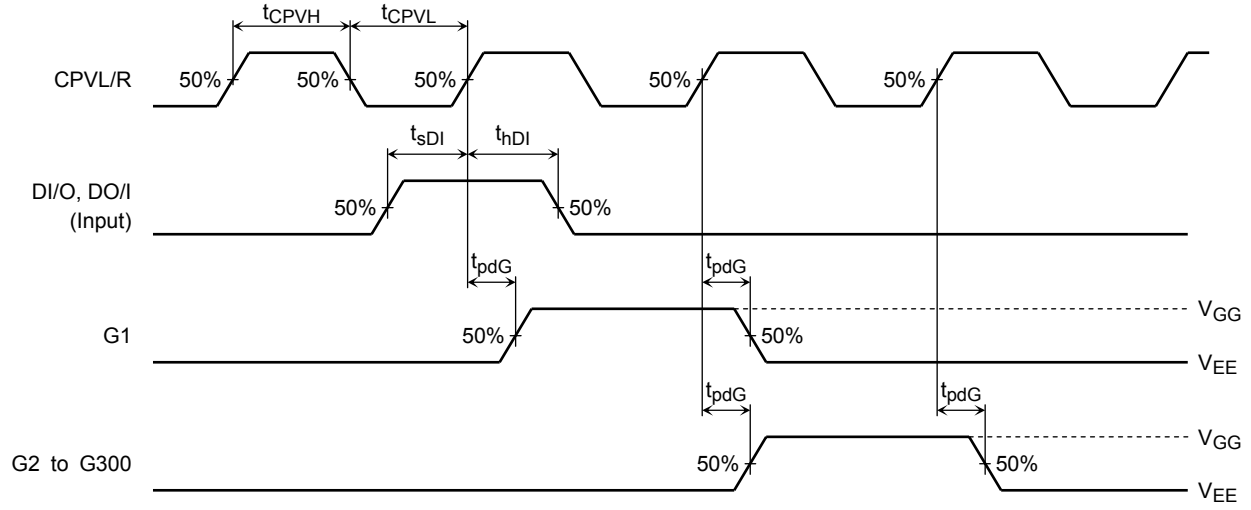
Note1: Input pins : DI/O, DO/I, CPVL/R, $\overline{OE}$ L/R

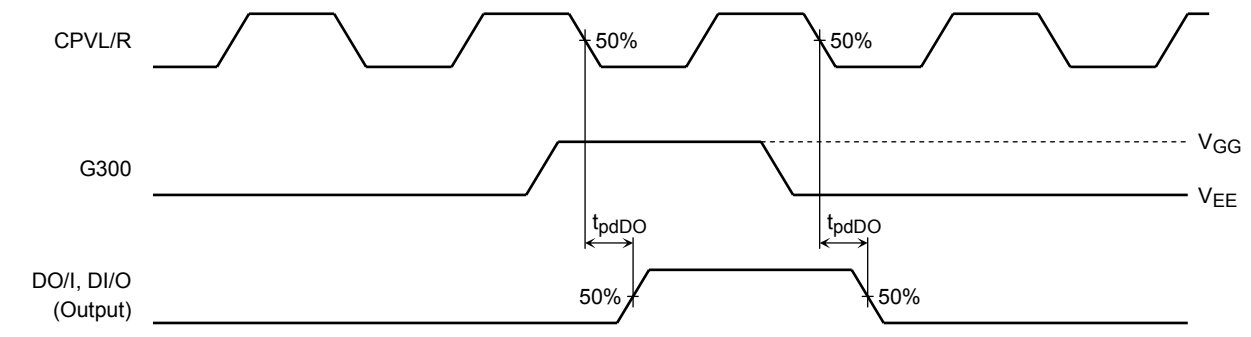
Note2: f_{CPV} = 50kHz, Shift data input : 60Hz, $\overline{OE}$ = low level, XDON = high level, MODE1 / MODE2 = high level

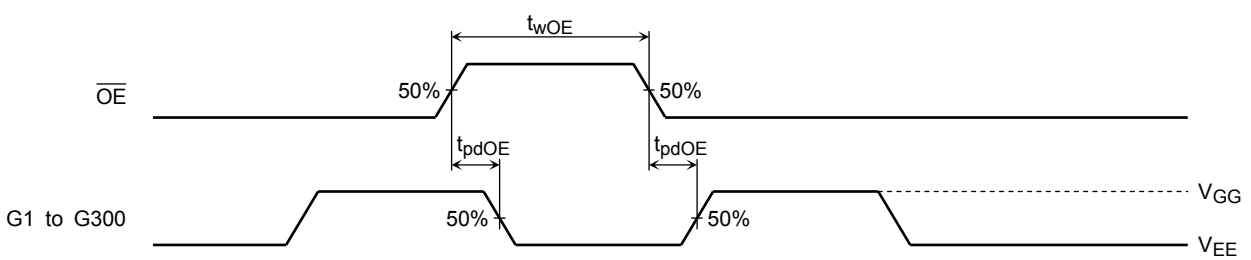
AC Characteristics

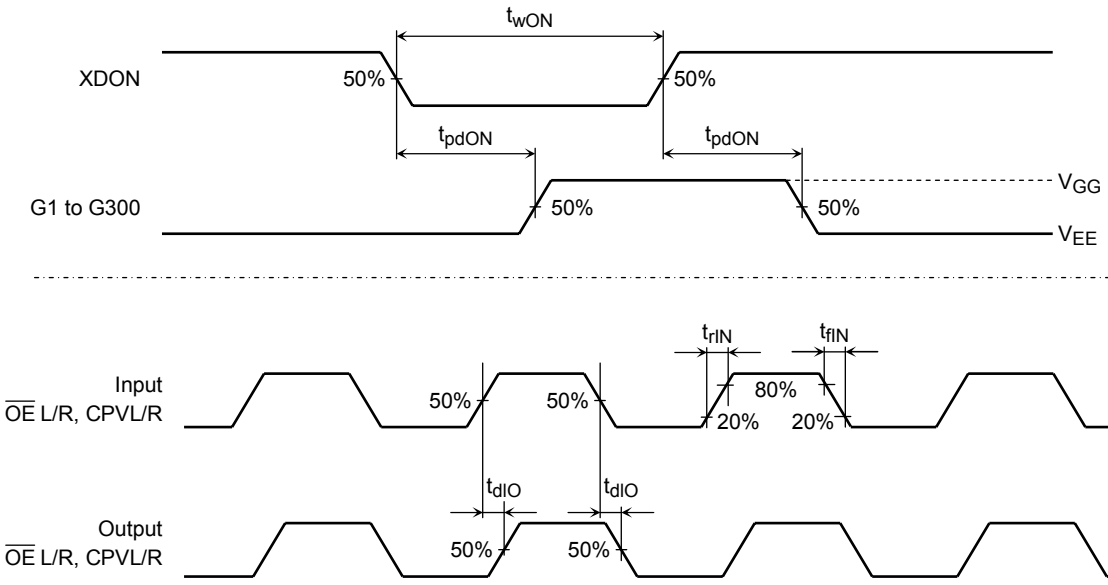
($V_{GG} - V_{EE}$ = 30.0 to 43.5 V, V_{DD} = 2.3 to 3.6 V, V_{SS} = 0 V, Ta = –20 to 75°C
t_{rIN} = 100ns (Max)、t_{fIN} = 100ns (Max)

Parameter	Symbol	Test circuit	Test Conditions	Min	Max	Unit
Clock frequency	t_{CPV}	—	—	—	150	kHz
CPV pulse width (H)	t_{CPVH}	—	—	500	—	ns
CPV pulse width (L)	t_{CPVL}	—	—	500	—	
Data set-up time	t_{sDI}	—	—	200	—	
Data hold time	t_{hDI}	—	—	200	—	
OE enable time	t_{wOE}	—	—	1	—	μs
Display-ON pulse width	t_{wON}	—	C_L = 300 pF	100	—	
Output delay time (1)	t_{pdDO}	—	C_L = 30 pF	—	250	ns
Output delay time (2)	t_{pdG}	—	C_L = 300 pF	—	800	
Output delay time (3)	t_{pdOE}	—	C_L = 300 pF	—	800	
Output delay time (4)	t_{pdON}	—	C_L = 300 pF	—	10	μs
Output delay time (5)	t_{dIO}	—	C_L = 30 pF	—	50	ns



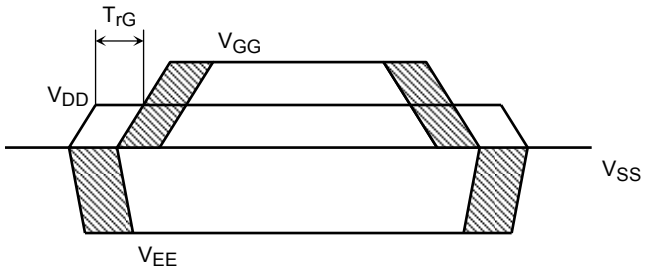






Power Supply Sequence

Turn power on in the order $V_{DD} \rightarrow V_{EE} \rightarrow$ Input signal $\rightarrow V_{GG}$. Turn power off in th reverse order.
However, if can be turned off at the same time, V_{GG}, V_{DD}, Input signals and V_{EE} under the condition of $V_{EE} \leq V_{SS} \leq$ Input signals $\leq V_{DD} \leq V_{GG}$.
The T6LE2 has a self Power on reset function. Keep the reset period : $T_{rG} \geq 10\mu s$



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- Light striking a semiconductor device can generate electromotive force due to photoelectric effects. In some cases this may cause the device to malfunction.
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