TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6B65AFG

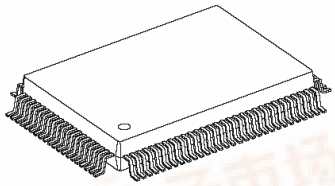
Column Driver LSI for Dot Matrix Graphic LCD's

Manufactured using the CMOS process, the T6B65AFG is a column (segment) driver for small-to-medium-sized dot matrix graphic LCDs. Use of the T6B65AFG enables power dissipation to be reduced. It is designed to connect directly to an 8-bit microprocessor unit. The MPU can program all operating modes for the T6B65AFG asynchronously.

The T6B65AFG stores display data transferred from an MPU in its internal display RAM. The contents of the internal display RAM correspond to the image on the LCD screen and are used to generate the LCD drive signal.

Three T6B65AFGs can be combined with a Toshiba T6B66BFG row (common) driver to drive a 240-dot by 65-dot LCD screen.

The T6B65AFG is lead (Pb)-free product.



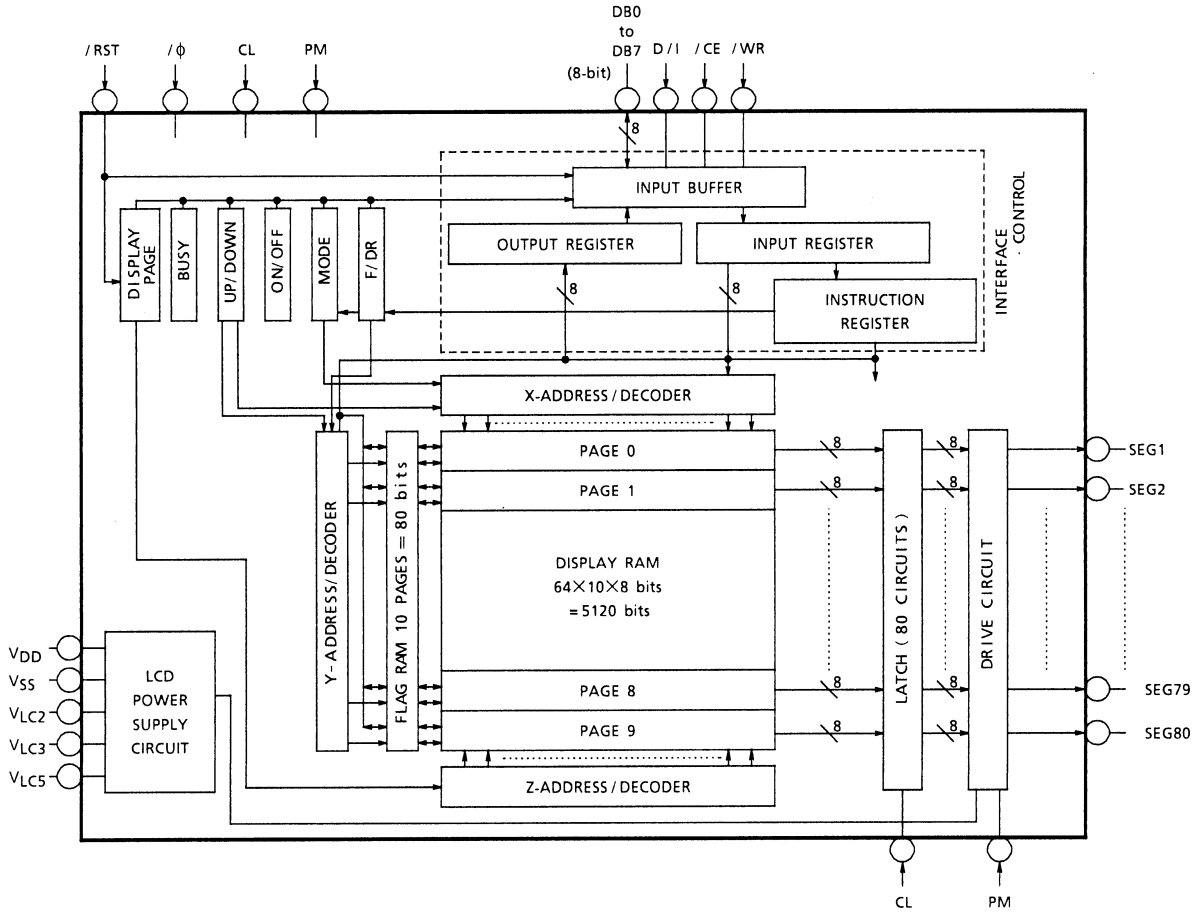
QFP100-P-1420-0.65Q

Weight: 1.6 g (typ.)

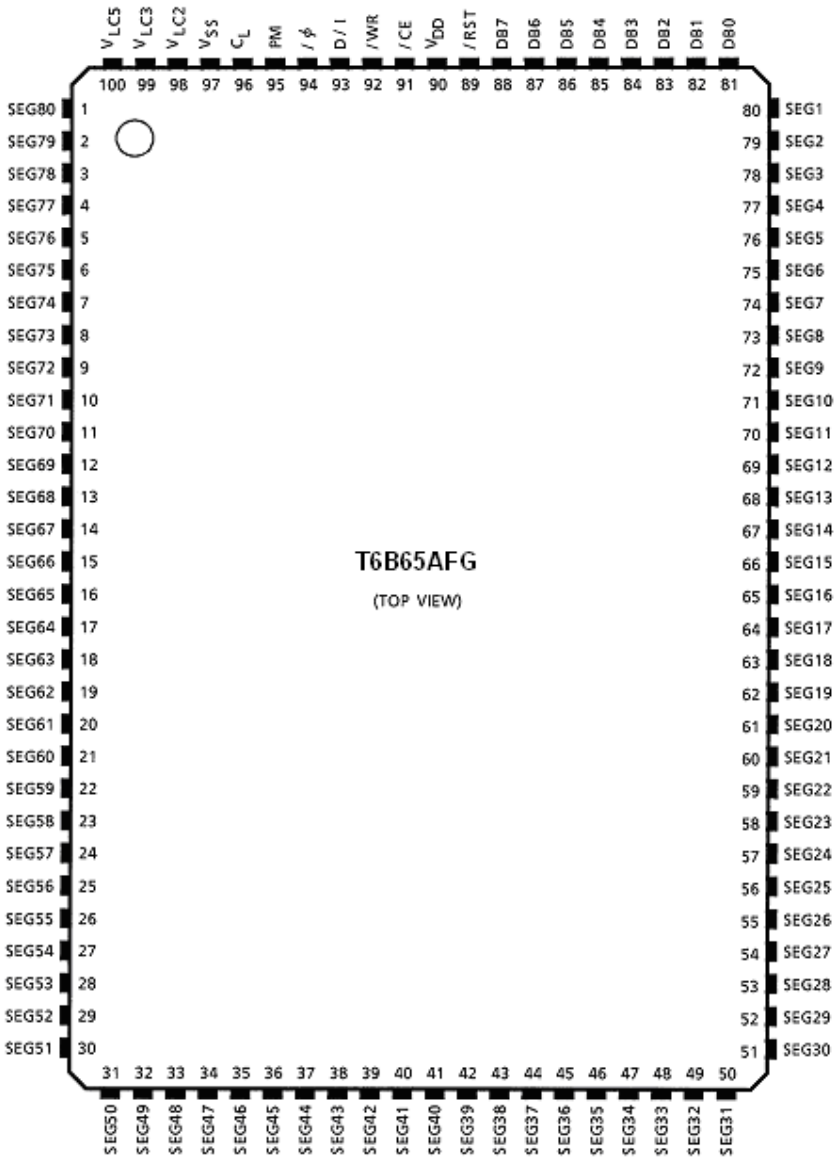
Features

- Dot matrix graphic LCD column driver with display RAM
- Display RAM capacity : 64 lines × 10 pages × 8 bits = 5120 bits (display area)
  1 line × 10 pages × 8 bits = 80 bits (flag area)
  Total = 5200 bits
- LCD drive outputs : 80
- Interface : 80-family MPU (8-bit)
- RAM data directly echoed to LCD
  (1) RAM bit data = 1 ..... ON
  (2) RAM bit data = 0 ..... OFF
- Duty: Can be controlled by the T6B66BFG.
- Display OFF functions
- Various functions
  X/Y-counter selection, Up/Down mode selection, X-address setting,
  Y-address setting, Display Start Line setting, "Status Read", display data read/write
- Low power consumption
- Logic power supply : 2.7 to 5.5 V
- CMOS Si-Gate process
- 100-pin-plastic flat package

Block Diagram



Pin Assignment



Pin Functions

Pin Name	Pin No .	I / O	Function
SEG1 to SEG80	1 to 80	Output	Column driver outputs
CL	96	Input	Shift clock pulse
PM	95	Input	Pre-frame signal input
/φ	94	Input	Clock signal
DB0 to DB7	81 to 88	I / O	Data bus
D / I	93	Input	Data/instruction select signal input (Note 1)
/ WR	92	Input	Write select signal input (Note 2)
/ CE	91	Input	Chip enable signal input (Note 3)
/ RST	89	Input	Reset signal input: / RST = L ..... Reset state
V_{DD}, V_{SS}	90, 97	—	Power supply
$V_{LC2, 3, 5}$	98, 99, 100	—	Power supply for LCD drive

Note 1: D / I = H …… Indicates that the data on DB0 to DB7 is display data.
D / I = L …… Indicates that the data on DB0 to DB7 is control data.

Note 2: / WR = H ……..…… Read is selected.
/ WR = L ……..…… Write is selected.

Note 3: When writing…… Data on DB0 to DB7 is latched on the rising edge of / CE.
When reading…..…… Data appears at DB0 to DB7 while / CE is LOW.

Function of Each Block

● Interface

The T6B65AFG is equipped with interface logic enabling interfacing to an 8-bit (80-family) MPU.

● Input register

This register holds 8-bit data from the MPU. Instruction and display data are distinguished by the D / I signal and the 8-bit data.

● Output register

This register holds 8-bit data from the display RAM. When display data is read, the display data in the address is copied to this register. The address is then automatically incremented or decremented. When an address is set, therefore, the correct data does not appear on the first data reading. The data at the specified address appears on the second data reading.

● X, Y (Page)-address counter

The X, Y (Page)-address counter holds a display RAM address. Reading or writing to the display RAM causes the X / Y-address to increment or decrement automatically.

- **Z-address counter**

The Z-address counter holds the 6-bit datum that indicates the display start line. This value is preset by the PM signal. The value indicates the address of the display start line, which is the line that appears at the top of the screen.

- **Counter Up / Down register**

This register determines the counter and Up / Down mode. When the X-counter / Up mode is selected, reading or writing to the RAM causes the X-counter to increment automatically.

When the X-counter / Down mode is selected, reading or writing to the RAM causes the X-counter to decrement automatically. When the Y-counter / Up mode is selected, reading or writing to the RAM causes the Y-counter to increment automatically. When the Y-counter / Down mode is selected, reading or writing to the RAM causes the Y-counter to decrement automatically.

- **Display ON / OFF register**

This 1-bit register holds the ON / OFF state. In the OFF state, the output is ignored. In the ON state, the data in the display RAM is displayed.

The data in the display RAM is independent of the value of the display ON / OFF setting.

- **Busy flag**

The Busy flag is set when an instruction other than the Status Read instruction is executed. Using Status Read, you can find out whether the Busy flag has been set or not. While the Busy flag is set, the T6B65A cannot accept any instruction other than Status Read.

Ensure, therefore, that the Busy flag is reset before an instruction is issued.

The Busy state time (T) is always as follows:

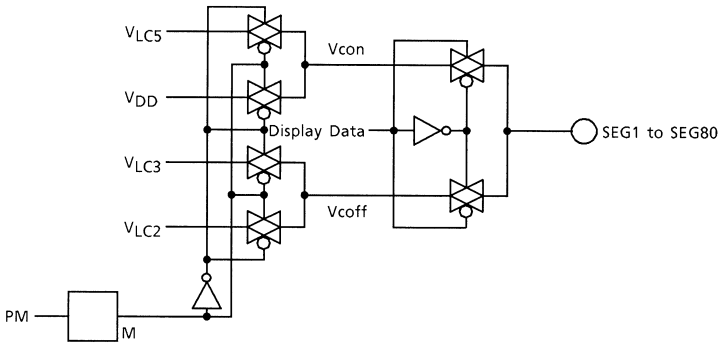
$1 / F \leq T \leq 2 / F$ [seconds] F: φ frequency (one half of the T6B66BFG's oscillation frequency)

- **Latch**

The rising edge of CL latches data from the display RAM.

- **Column driver circuit and LCD voltage generation circuit**

The column driver circuit consists of 80 driver circuits. The combination of display data from latches and the M signal selects one of the four LCD levels. Details of the voltage generation circuit and column driver circuit are shown in the diagram below:



Command Definitions

Code										
/ WR	D / I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
0	0	0	0	0	0	0	0	1	1 / 0	Display ON (1) / OFF (0)
0	0	0	0	0	0	0	1	Y / X	U / D	Y (1) / X (0) Counter Select UP (1) / Down (0) Mode Select
0	0	0	0	0	0	1	*	*	*	Test Mode Select
0	0	0	1	Z-Address (0 to 63)						Set Z-Address
0	0	1	0	X-Address (0 to 63)						Set X-Address
0	0	1	1	*	F / DR	Y (Page) −Address (0 to 9)				Set Y (Page) −Address
1	0	B	0	D	R	0	F / DR	Y / X	U / D	Status Read (Note)
0	1	Write Data								Write Display Data
1	1	Read Data								Read Display Data

*: INVALID

Note: B : Busy flag
D : Display ON (1) / OFF (0)
R : Reset
Y / X : Counter Select 1: Y-Counter 0: X-Counter
U / D : Up / Down Select 1: Up 0: Down
F / DR : Flag Mode 1: Flag Mode 0: Display RAM Mode

- **Display ON / OFF**

	/ WR	D / I	DB7	.....	DB0	
Code	0	0	0	0	0	0	0	0	1	1	Display ON
	0	0	0	0	0	0	0	0	1	0	Display OFF

This command controls the display ON / OFF setting. Display ON / OFF does not change the display RAM data. When / RST = L, Display = OFF (all the segment outputs are at the V_{DD} level when Display = OFF).
The T6B65A is in display OFF mode after a reset operation.

- **Counter UP / DOWN select**

	/ WR	D / I	DB7	.....	DB0						
Code	0	0	0	0	0	0	0	1	0	0	X-Counter / Down Mode
	0	0	0	0	0	0	0	1	0	1	X-Counter / Up Mode
	0	0	0	0	0	0	0	1	1	0	Y-Counter / Down Mode
	0	0	0	0	0	0	0	1	1	1	Y-Counter / Up Mode

This command selects the counter and Up / Down mode. When / RST = L, Y-Counter / Up mode is selected.

- **Test mode select**

	/ WR	D / I	DB7							DB0	
Code	0	0	0	0	0	0	1	*	*	*	*: INVALID

This command selects the Test mode. Do not use this command.

- **Set Z-address (Display Start Line)**

	/ WR	D / I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

This command specifies which RAM line (0 to 63) is displayed at the top of the screen. When the display duty is more than 1 / 64 (e.g., 1 / 33, 1 / 49), display begins at a line within the range 1 to 33 or 1 to 49. This command only applied to display RAM. The line following the last line of the display RAM is the flag RAM.

- **Set X-address**

	/ WR	D / I	DB7							DB0
Code	0	0	1	0	A	A	A	A	A	A

This command sets the X-address (0 to 63). When the Counter Up / Down Select command selects this address counter, reading or writing to the RAM causes the X-address to increment or decrement automatically.

In X-Counter / Up mode, if the previous X-address is 63, the new X-address after the increment will be 0 and the Y (page)-address will be incremented. In Y-Counter / Down mode, if the previous X-address is 0, the new X-address after the decrement will be 63 and the Y (page)-address will be decremented.

- **Set Y (Page)-address**

	/ WR	D / I	DB7							DB0	
Code	0	0	1	1	*	1	A	A	A	A	Flag mode
	0	0	1	1	*	0	A	A	A	A	Display RAM mode *: INVALID

This command sets the Y (page) -address and also selects Flag mode or Display RAM mode.

In Flag mode, you can read data from or write data to Flag RAM only but cannot access the Display RAM.

In Display RAM mode, you can read data from or write data to the Display RAM only but cannot access the Flag RAM.

When the Counter Up / Down Select command selects this address counter, reading from or writing to the RAM causes the Y-address to increment or decrement automatically.

In Y-Counter / Up mode, if the previous Y-address is 9, the new Y-address after the increment will be 0 and the X-address will be incremented. In Y-Counter / Down mode, if the previous Y-address is 0, the new Y-address after the decrement will be 9 and the X-address will be decremented.

In Flag mode, only Y-Counter / Up or Down mode is permitted.

- **Status Read**

	/ WR	D / I	DB7	·····						DB0
Code	0	0	B	0	D	R	0	F / DR	Y / X	U / D

B (Busy) : When B = 1, an instruction is being executed and no other instructions may be accepted.
When B = 0, instructions can be accepted.

D (Display) : When D = 1, display is ON.
When D = 0, display is OFF.

R (Reset) : When R = 1, the T6B65A is in the Reset state.
When R = 0, the T6B65A is in the Operating state.

Y / X (Counter) : When Y / X = 1, Y-Counter is selected.
When Y / X = 0, X-Counter is selected.

U (Up) / D (Down) : When U / D = 1, Up mode is selected.
When U / D = 0, Down mode is selected.

F (Flag) / DR (Display RAM) : When F / DR = 1, Flag mode is selected.
When F / DR = 0, Display RAM is selected.

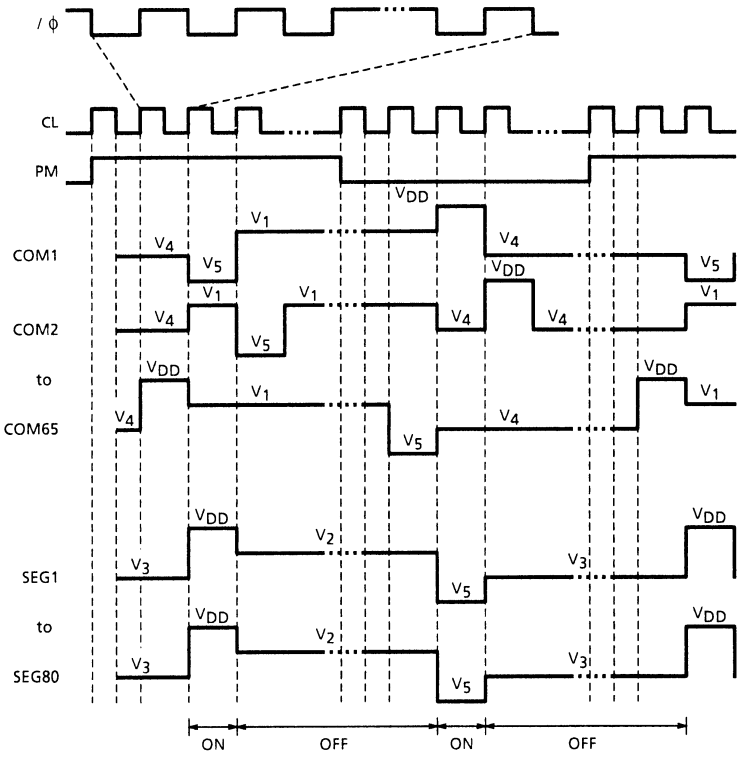
- **Read / Write display data**

	/ WR	D / I	DB7	·····						DB0	
Code	0	1	D	D	D	D	D	D	D	D	Write Data
	1	1	D	D	D	D	D	D	D	D	Read Data

This command sends data to or receives data from the LCD RAM address that was specified. However, the correct data does not appear on the first read of the display data.

Refer to the description of the Output Register in the section FUNCTION OF EACH BLOCK.

LCD Drive Waveform



LCD driver timing chart (1 / 65 duty)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V_{DD} (Note 1)	−0.3 to 7.0	V
Supply Voltage (2)	$V_{LC2, 3, 5}$ (Note 3)	V_{DD} − 18.0 to V_{DD} + 0.3	V
Input Voltage	V_{IN} (Note 1, 2)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−20 to 75	°C
Storage Temperature	T_{stg}	−55 to 125	°C

Note 1: Referenced to V_{SS}
Note 2: Applies to all data bus pins and input pins except V_{LC2}, V_{LC3} and V_{LC5}
Note 3: Ensure that the following condition is always maintained:
$V_{DD} \geq V_{LC2} \geq V_{LC3} \geq V_{LC5}$

Electrical Characteristics
DC Characteristics
Test Conditions (1)
(Unless otherwise specified, V_{SS} = 0, V_{DD} = 3.0 V ± 10%, V_{LC5} = V_{DD} − 16 V, Ta = −20 to 75°C)

Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	2.7	—	3.3	V	V_{DD}
Operating Supply (2)		V_{LC5}	—	—	V_{DD} −16.0	—	V_{DD} −4.0	V	V_{LC5}
Input Voltage	H Level	V_{IH}	—	—	0.8 V_{DD}	—	V_{DD}	V	CL, PM, / φ DB0 to DB7, D / I, / WR, / CE, / RST
	L Level	V_{IL}	—	—	0	—	0.2 V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} −0.2	—	—	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 μA	—	—	0.2	V	
Column Driver Output Resistance		R_{col}	—	V_{DD} − V_{LC5} = 11.0 V Load current = ±100 μA	—	—	7.5	KΩ	SEG1 to SEG80
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	−1	—	1	μA	DB0 to DB7, D / I, / WR, / CE, / RST, CL, PM, / φ
Operating Frequency		fφ	—	—	10	—	250	kHz	/ φ
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	100	140	μA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	20	30	μA	V_{DD}
Current Consumption (3)		I_{DD3}	—	(Note 3)	−1	—	1	μA	V_{DD}

Note 1: Current consumption while the internal data receiver is operating:
V_{DD} = 2.7 to 3.3 V, V_{LC5} = V_{DD} − 16 V, Ta = 25°C
1/9 bias, 1/65 duty, no load, f_{PM} = 35 Hz, f_{CE} = 1 MHz

Note 2: Current consumption while the internal data receiver is inactive:
V_{DD} = 2.7 to 3.3 V, V_{LC5} = V_{DD} −16 V, Ta = 25°C
1/9 bias, 1/65 duty, no load

Note 3: Current consumption in low power mode (/ STB pin of T6B66BFG = L):
V_{DD} = 3.0V, V_{LC5} = 0 V, Ta = 25°C, no load

Test Conditions (2)
(Unless otherwise noted, V_{SS} = 0, V_{DD} = 5.0 V ± 10%, V_{LC5} = V_{DD} − 16 V, Ta = −20 to 75°C)

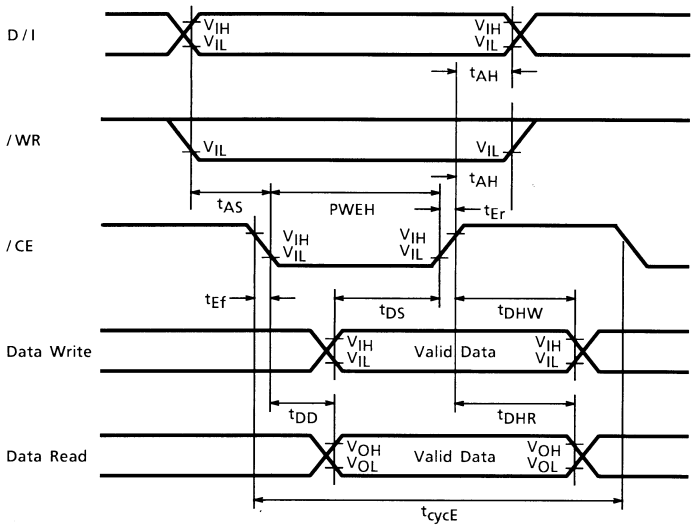
Item		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)		V_{DD}	—	—	4.5	—	5.5	V	V_{DD}
Operating Supply (2)		V_{LC5}	—	—	V_{DD} −16.0	—	V_{DD} −4.0	V	V_{LC5}
Input Voltage	H Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V	CL, PM, /φ DB0 to DB7, D / I, / WR, / CE, / RST
	L Level	V_{IL}	—	—	0	—	0.3 V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	I_{OH} = −400 μA	V_{DD} −0.4	—	—	V	DB0 to DB7
	L Level	V_{OL}	—	I_{OL} = 400 μA	—	—	0.4	V	
Column Output Resistance		R_{col}	—	V_{DD} − V_{LC5} = 11.0 V Load current = ±100 μA	—	—	7.5	kΩ	SEG1 to SEG80
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} to GND	−1	—	1	μA	DB0 to DB7, D / I, / WR, / CE, / RST, CL, PM, /φ
Operating Frequency		fφ	—	—	10	—	250	kHz	/ φ
Current Consumption (1)		I_{DD1}	—	(Note 1)	—	220	330	μA	V_{DD}
Current Consumption (2)		I_{DD2}	—	(Note 2)	—	35	50	μA	V_{DD}
Current Consumption (3)		I_{DD3}	—	(Note 3)	−1	—	1	μA	V_{DD}

Note 1: Current consumption while the internal data receiver is operating:
V_{DD} = 4.0 to 5.5 V, V_{LC5} = V_{DD} − 16 V, Ta = 25°C
1/9 bias, 1/65 duty, no load, f_{PM} = 35 Hz, f_{CE} = 1 MHz

Note 2: Current consumption while the internal data receiver is inactive:
V_{DD} = 4.0 to 5.5 V, V_{LC5} = V_{DD} − 16 V, Ta = 25°C
1/9 bias, 1/65 duty, no load

Note 3: Current consumption in Low Power mode (/ STB pin of T6B66BFG = L):
V_{DD} = 5.0 V, V_{LC5} = 0 V, Ta = 25°C, no load

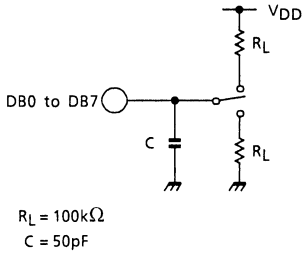
AC Characteristics



Test Conditions (1)
(V_{SS} = 0 V , V_{DD} = 3.0 V ± 10%, V_{LC5} = 0 V , Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{cycE}	1000	—	ns
Enable Pulse Width	PWEH	450	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	25	ns
Address Set-up Time	t_{AS}	40	—	ns
Address Hold Time	t_{AH}	10	—	ns
Data Set-up Time	t_{DS}	280	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD} (Note)	—	300	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

Load Circuit

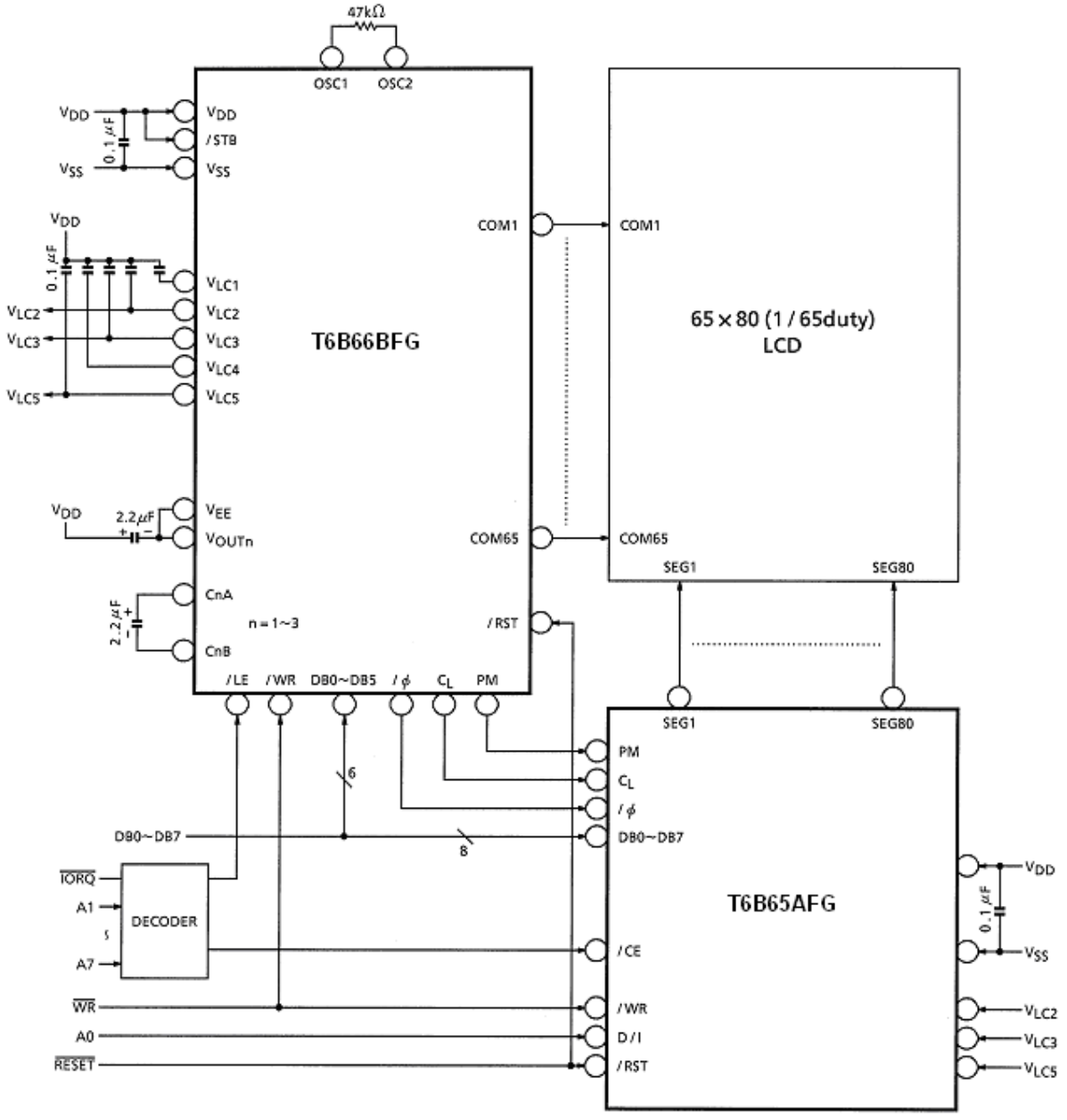


Test Conditions (2)
(V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, V_{LC5} = 0 V, Ta = −20 to 75°C)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{cycE}	500	—	ns
Enable Pulse Width	PWEH	220	—	ns
Enable Rise / Fall Time	t_{Er}, t_{Ef}	—	20	ns
Address Set-up Time	t_{AS}	40	—	ns
Address Hold Time	t_{AH}	0	—	ns
Data Set-up Time	t_{DS}	60	—	ns
Data Hold Time	t_{DHW}	10	—	ns
Data Delay Time	t_{DD} (Note)	—	120	ns
Data Hold Time	t_{DHR} (Note)	20	—	ns

Note: With load circuit connected

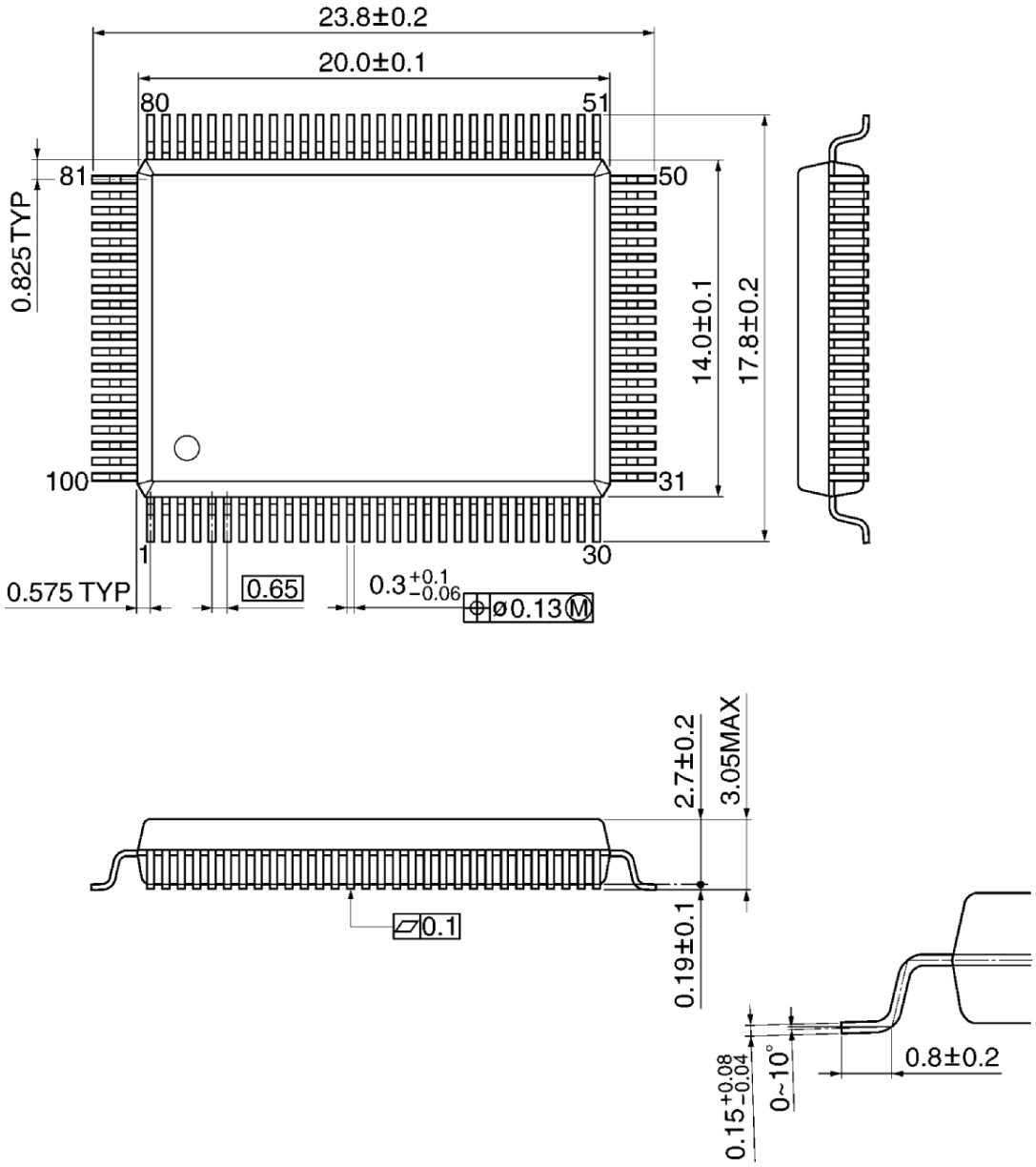
Application Circuit



Package Dimensions

QFP100-P-1420-0.65Q

Unit: mm



Weight :1.6g (Typ.)

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