ANALOG DEVICES

Quad SPST JFET Analog Switches

SW-201/SW-202

FEATURES

SW-201

- **Normally "ON" for Logic 0 Input**
- **Improved Performance and Pin Compatible With DG-201, LF11201/13201, HI201, and IH201**

SW-202

- **Normally "OFF" For Logic 0 Input**
- **Improved Performance and Pin Compatible With LF11202/12202/13202 and IH202**

Both SW-201 and SW-202

- **Highly Resistant to Static Discharge Destruction**
- **Guaranteed Break-Before-Make Switching ($t_{OFF} < t_{ON}$)**
- **Low "ON" Resistance ..... 80Ω Max**
- **Guaranteed R_{ON} Matching ..... 15% Max**
- **Low R_{ON} Variation from Analog Input Voltage 5%**
- **High Analog Current Operation ..... 10mA Min**
- **Low Leakage Currents at High Temperatures:**
  - **T_A = 125°C ..... 60nA Max**
  - **T_A = 85°C ..... 30nA Max**
- **Guaranteed Switching Speeds:**
  - **t_{ON} = 500ns Max t_{OFF} = 400ns Max**
- **Digital Inputs are TTL and CMOS Compatible**
- **Dual or Single Supply Operation**
- **Available in Die Form**

ORDERING INFORMATION †

DIP PACKAGE	SWITCH CONFIGURATION NC	SWITCH CONFIGURATION NO	OPERATING TEMPERATURE RANGE
16-PIN EPOXY	SW201GP	SW202GP	XIND
16-PIN SOL	SW201GS	SW202GS	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

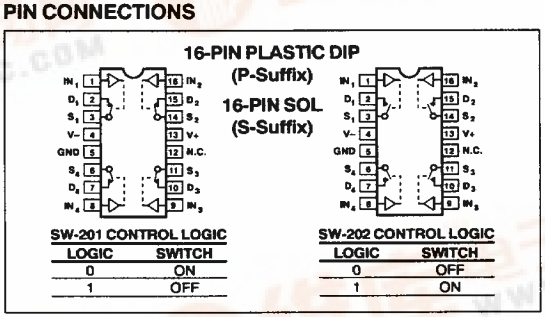
The SW-201 and SW-202 each consist of four independent, single-pole, single-throw (SPST) analog switches, which may be independently digitally controlled. Each SW-201 switch is normally closed (NC), whereas each SW-202 is normally open (NO) when the corresponding digital control input is a zero. The SW-201 and SW-202 are otherwise identical.

The judicious combination of bipolar and FET devices in a single monolithic IC results in a product with performance characteristics and ruggedness that are superior to those of a similar circuit fabricated using CMOS technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V− = 0V, the analog signal range will extend from ground to +32V.

The PNP logic inputs are TTL and CMOS compatible. Logic input currents are at micro-ampere levels which improves circuit fan in.

PIN CONNECTIONS



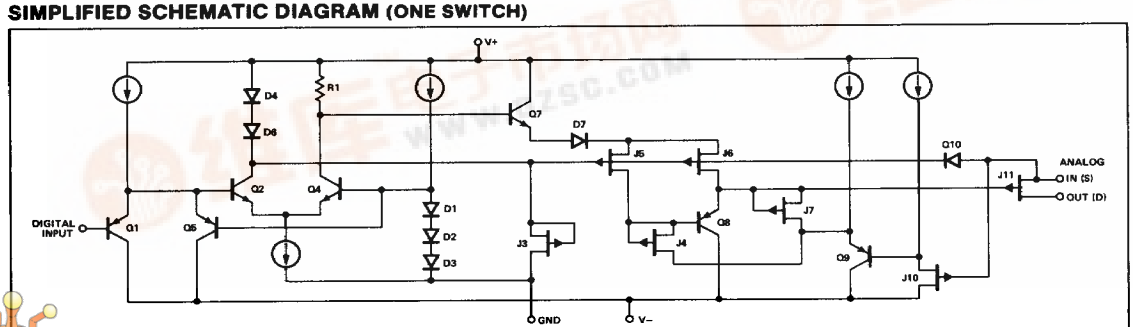
SW-201 CONTROL LOGIC

LOGIC	SWITCH
0	ON
1	OFF

SW-202 CONTROL LOGIC

LOGIC	SWITCH
0	OFF
1	ON

SIMPLIFIED SCHEMATIC DIAGRAM (ONE SWITCH)



Manufactured under the following patent: 4,228,367

REV. A

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
SW-201GP, GS, SW202GP, GS ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
P-Suffix ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Maximum Junction Temperature ..... +150°C
V+ Supply to V– Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... (–4V or V–) to V+ Supply
Analog Input Voltage Range
Continuous ..... V– Supply to V+ Supply + 20V
1% Duty Cycle and Driving All 4 Inputs with
500µsec Pulse ..... V– Supply –15V to V+ Supply + 20V
Maximum Current Through Any Pin 30mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	82	39	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V\pm = \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201G SW-202G MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_A = 0V$, $I_S = 1mA$ $V_A = \pm 10V$, $I_S = 1mA$	— —	100 100	150 150	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_D = 100\mu A$; (Note 1)	—	—	20	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ (Note 6) $I_S = 1.0mA$	+10 −10	+11 −15	— —	V
Analog Current Range	I_A	$V_S = \pm 10V$	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	$V_S \leq 10V$, $I_S = 1mA$	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 5)	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$, (Note 5)	—	—	10	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$, (Note 5)	—	—	10	nA
Logical "1" Input Current	I_{INH}	$V_{IN} = 2V$ to 15V, (Note 4)	—	—	10	µA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8$	—	1.5	10.0	µA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit, (Note 7)	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit, (Note 7)	—	200	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	(Note 3)	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	$V_A = 0V$, (Note 5)	—	7	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_A = 0V$, (Note 5)	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)} + C_{S(ON)}$	$V_S = V_D = 0V$, (Note 5)	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	$V_S = 5V_{RMS}$, $R_L = 680\Omega$, $C_L = 7pF$, f = 500kHz, (Note 5)	—	58	—	dB
Crosstalk	C_T	$V_S = 5V_{RMS}$, $R_L = 680\Omega$, $C_L = 7pF$, f = 500kHz, (Note 5)	—	70	—	dB
Positive Supply Current	I+	All Channels "ON", (Note 5)	—	4	12	mA
Negative Supply Current	I–	All Channels "ON", (Note 5)	—	1	6.5	mA
Positive Supply Current	I+	All Channels "OFF", (Note 5)	—	6	12	mA
Negative Supply Current	I–	All Channels "OFF", (Note 5)	—	4	8	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	3	6	mA

ELECTRICAL CHARACTERISTICS at V± = ±15V; −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

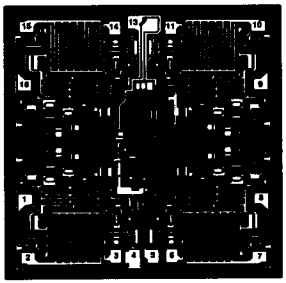
PARAMETER	SYMBOL	CONDITIONS	SW-201G SW-202G MIN	TYP	MAX	UNITS
Temperature Range	T_A	Operating	0	—	70	°C
"ON" Resistance	R_{ON}	V_A = 0V, I_D = 1mA V_A = ±10V, I_D = 1mA	— —	— —	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_A = 0V, I_D = 100μA; (Note 1)	—	10	—	%
Analog Voltage Range	V_A	I_S = 1.0mA (Note 6) I_S = 1.0mA	+10 −10	+11 −15	— —	V
Analog Current Range	I_A	V_S = ±10.0V	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$V_S \leq +10V$ I_S = 1mA	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = −10V, (Note 5) T_A = Max. Operating Temp.	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = −10V, (Note 5) T_A = Max. Operating Temp.	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$ + $I_{D(ON)}$	V_S = V_D = ±10V, (Note 5) T_A = Max. Operating Temp.	—	—	60	nA
Logical "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	V
Logic "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 2V to 15V, (Note 4)	—	—	15	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Test Circuit, (Note 2)	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Test Circuit, (Note 2)	—	—	500	ns
Break-Before-Make Time	t_{ON}-t_{OFF}	(Note 3)	—	50	—	ns
Positive Supply Current	I+	All Channels "ON", (Note 5)	—	—	15.8	mA
Negative Supply Current	I−	All Channels "ON", (Note 5)	—	—	14.5	mA
Positive Supply Current	I+	All Channels "OFF", (Note 5)	—	—	18	mA
Negative Supply Current	I−	All Channels "OFF", (Note 5)	—	—	14.5	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	—	10.0	mA

NOTES:

1. V_A = 0V, I_D = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$
2. Guaranteed by design.
3. Switch is guaranteed by design to provide break-before-make operation.
4. Current tested at V_{IN} = 2V. This is worst case condition.
5. Switch being tested ON or OFF as indicated, V_{INH} = 2V or V_{INL} = 0.8V, per logic truth table.
6. Guaranteed by R_{ON} and leakage tests. For normal operation analog signal voltages should be restricted to less than (V+) −4V.
7. Sample tested.

5

DICE CHARACTERISTICS



DIE SIZE 0.101 × 0.097 inch, 9797 sq. mils
(2.565 × 2.464 mm, 6.320 sq. mm)

1. IN1
2. D1
3. S1
4. V– (SUBSTRATE)
5. GND
6. S2
7. D2
8. IN2
9. IN3
10. D3
11. S3
13. V+
14. S4
15. D4
16. IN4

WAFER TEST LIMITS at V+ = 15V, V– = –15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N LIMIT	SW-201G SW-202G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	80	100	Ω MAX
R_{ON} Mismatch	R_{ON} Match	$V_A = 0V$, $I_S \le 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_S \le 10V$, $I_S = 1mA$	15	20	% MAX
Positive Supply	I+	(Note 1)	9	10.5	mA MAX
Negative Supply Current	I–	(Note 1)	6	7	mA MAX
Ground Current	I_G		4	4	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$ (Note 3)	±10	±10	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2	2	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5	5	μA MAX
Logic "1" Input Current	I_{INH}	$2V \le V_{IN} \le 15V$, (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

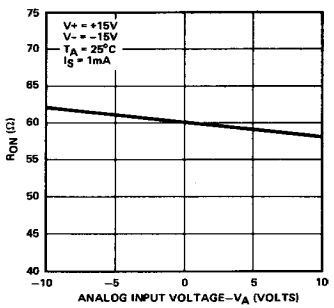
TYPICAL ELECTRICAL CHARACTERISTICS V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N TYPICAL	SW-201G SW-202G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

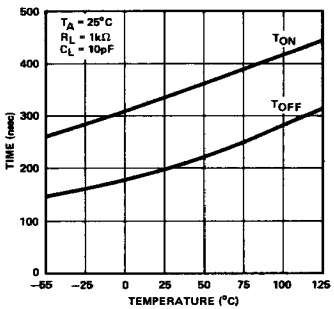
NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at V_{IN} = 2V. This is worst case condition.
3. Guaranteed by R_{ON} and leakage tests.

TYPICAL PERFORMANCE CHARACTERISTICS

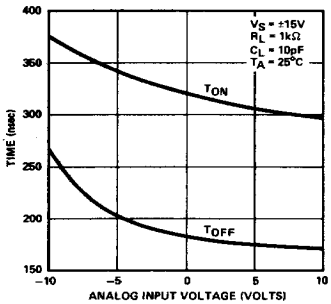
"ON" RESISTANCE vs ANALOG VOLTAGE (V_A)



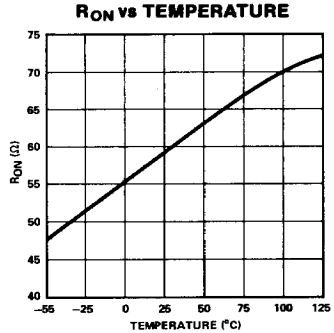
SWITCHING TIME vs TEMPERATURE



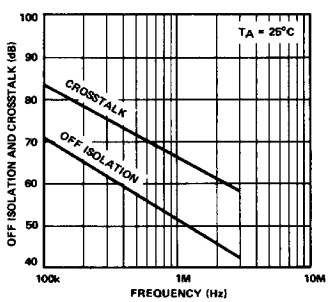
SWITCHING TIME vs ANALOG VOLTAGE



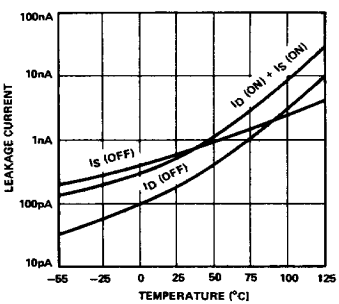
R_{ON} vs TEMPERATURE



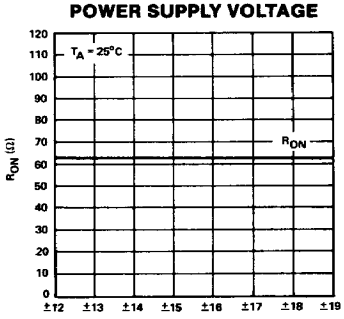
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



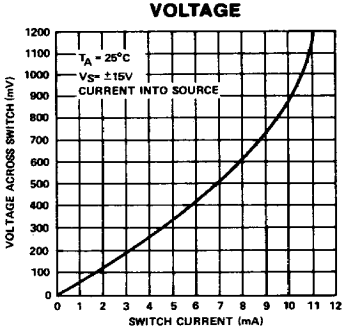
LEAKAGE CURRENT vs TEMPERATURE



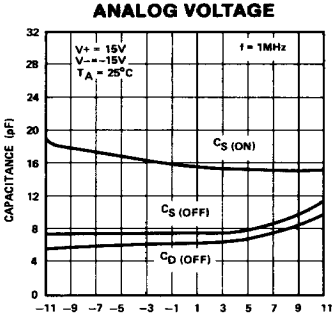
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



SWITCH CURRENT vs VOLTAGE



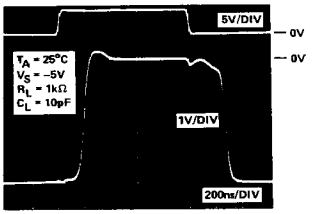
SWITCH CAPACITANCE vs ANALOG VOLTAGE



5

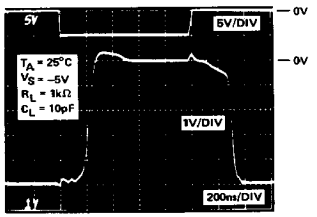
TYPICAL PERFORMANCE CHARACTERISTICS

SW-201
t_{ON}/t_{OFF} SWITCHING RESPONSE



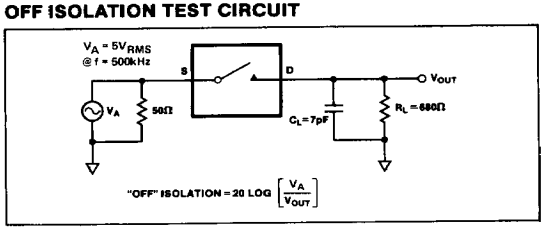
TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

SW-202
t_{ON}/t_{OFF} SWITCHING RESPONSE

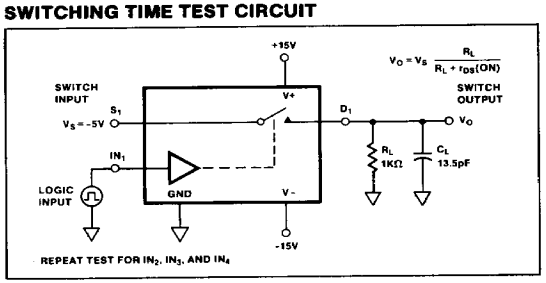


TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (1V/DIV)

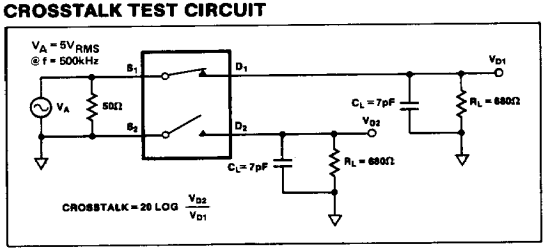
OFF ISOLATION TEST CIRCUIT



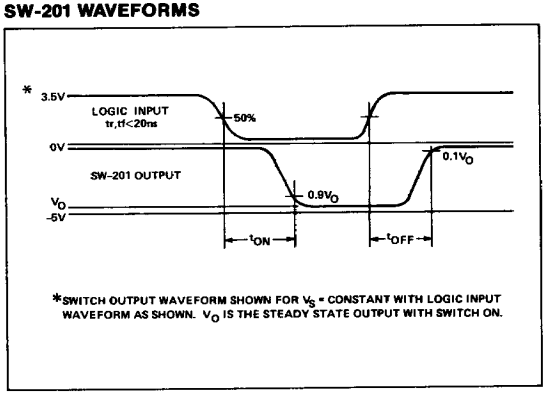
SWITCHING TIME TEST CIRCUIT



CROSSTALK TEST CIRCUIT

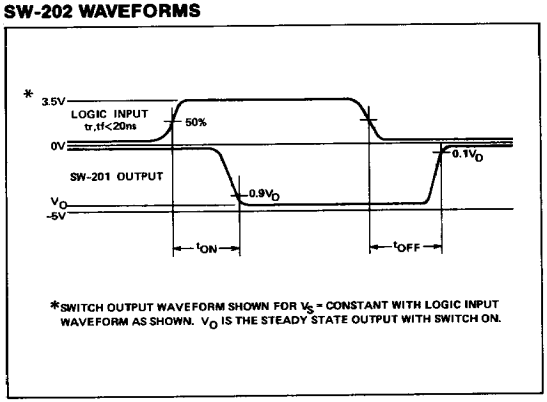


SW-201 WAVEFORMS



*SWITCH OUTPUT WAVEFORM SHOWN FOR V_S = CONSTANT WITH LOGIC INPUT WAVEFORM AS SHOWN. V_O IS THE STEADY STATE OUTPUT WITH SWITCH ON.

SW-202 WAVEFORMS



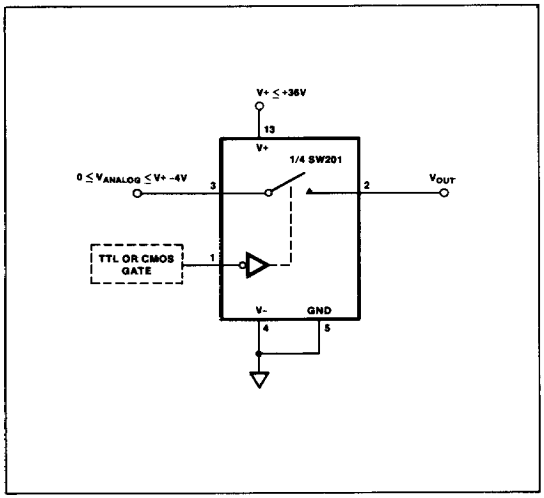
*SWITCH OUTPUT WAVEFORM SHOWN FOR V_S = CONSTANT WITH LOGIC INPUT WAVEFORM AS SHOWN. V_O IS THE STEADY STATE OUTPUT WITH SWITCH ON.

APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode as the input voltage is raised above ≈ 1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of −15V to +11V with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P, and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

OPERATION FROM SINGLE POSITIVE POWER SUPPLY



5

TYPICAL APPLICATIONS

PROGRAMMABLE GAIN NONINVERTING AMPLIFIER WITH SELECTABLE INPUTS