ANALOG DEVICES

Quad SPST JFET Analog Switch

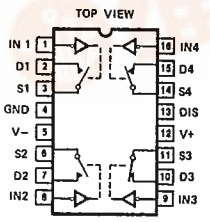
T-51-11 **SW-06**

FEATURES

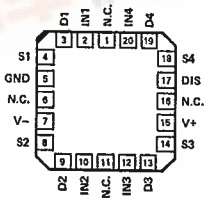
- Two Normally Open and Two Normally Closed SPST Switches with Disable
- Switches can be Easily Configured as a Dual SPDT or a DPDT
- Highly Resistant to Static Discharge Destruction
- Higher Resistance to Radiation Than Analog Switches Designed with MOS Devices
- Guaranteed R_{ON} Matching ..... 10% Max
- Guaranteed Switching Speeds ..... T_{ON} = 500ns Max
  T_{OFF} = 400ns Max
- Guaranteed Break-Before-Make Switching
- Low "ON" Resistance ..... 80Ω Max
- Low R_{ON} Variation from Analog Input Voltage 5%
- Low Total Harmonic Distortion 0.01%
- Low Leakage Currents at High Temperature:
  T_A = 125°C ..... 100nA Max
  T_A = 85°C ..... 30nA Max
- Digital Inputs TTL/CMOS Compatible and Independent of V+
- Improved Specifications and Pin Compatible to LF-11333/13333
- Dual or Single Power Supply Operation
- Available in Die Form

PIN CONNECTIONS

Switches are shown in the logic "0" input state and DIS = "1"



16-PIN DIP
(Q or P-Suffix)
16-PIN SOL
(S-Suffix)



SW-06BRC/883
LCC PACKAGE
(RC-Suffix)

ORDERING INFORMATION †

PLASTIC 16-PIN	CERDIP 16-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
–	SW06BQ*	SW06BRC/883	MIL
SW06GP	SW06FQ	–	XIND
SW06GS	–	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The SW-06 is a four channel single-pole, single-throw analog switch that employs both bipolar and ion-implanted FET devices. The SW-06 FET switches use bipolar digital logic inputs which are more resistant to static electricity than CMOS devices. Ruggedness and reliability are inherent in the SW-06 design and construction technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With V+ = 36V, V– = 0V, the analog signal range will extend from ground to +32V.

PNP logic inputs are TTL and CMOS compatible to allow the SW-06 to upgrade existing designs. The logic "0" and logic "1" input currents are at micro-ampere levels reducing loading on CMOS and TTL logic.

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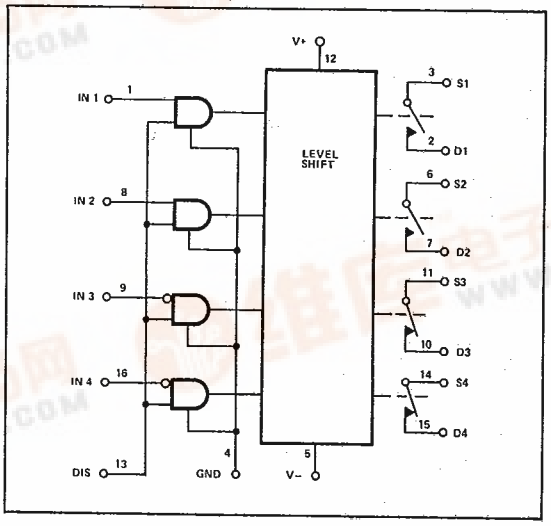
FUNCTIONAL DIAGRAM



TRUTH TABLE

DISABLE INPUT	LOGIC INPUT	SWITCH STATE CHANNELS 1 & 2	SWITCH STATE CHANNELS 3 & 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

SW-06

T-51-11

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range
- SW-06BQ, BRC ..... –55°C to +125°C
- SW-06FQ ..... –40°C to +85°C
- SW-06GP, GS ..... –40°C to +85°C

Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Maximum Junction Temperature ..... 150°C
V+ Supply To V– Supply 36V
V+ Supply to Ground 36V
Logic Input Voltage ..... (–4V or V–) to V+ Supply
Analog Input Voltage Range
Continuous ..... V– Supply to V+ Supply +20V

Maximum Current Through
Any Pin Including Switch 30mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted.

			SW-06B			SW-06F			SW-06G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1mA V_S = ±10V, I_S = 1mA	— —	60 65	80 80	— —	60 65	100 100	— —	100 100	150 150	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA (Note 1)	—	5	10	—	5	20	—	—	20	%
Analog Voltage Range	V_A	I_S = 1mA I_S = 1mA (Note 8)	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	V
Analog Current Range	I_A	V_S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ 10V, I_S = 1.0mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = –10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Source Current in "ON" Condition	$I_{S(ON)+}$ $I_{D(ON)}$	V_S = V_D = ±10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Logical "1" Input Voltage	V_{INH}	Full Temperature Range (Notes 6, 8)	2.0	—	—	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V_{INL}	Full Temperature Range (Notes 6, 8)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V (Note 4)	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input	I_{INL}	V_{IN} = 0.8V	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 6, 9)	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 6, 9)	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t_{ON}–t_{OFF}	(Note 3)	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	V_S = 0V (Note 5)	—	7.0	—	—	7.0	—	—	7.0	—	pF
Drain Capacitance	$C_{D(OFF)}$	V_S = 0V (Note 5)	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)}$+ $C_{S(ON)}$	V_S = V_D = 0V (Note 5)	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	V_S = 5V_{RMS}, R_L = 680Ω, C_L = 7pF, f = 500kHz (Note 5)	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C_T	V_S = 5V_{RMS}, R_L = 680Ω, C_L = 7pF, f = 500kHz (Note 5)	—	70	—	—	70	—	—	70	—	dB

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SW-06B MIN	SW-06B TYP	SW-06B MAX	SW-06F MIN	SW-06F TYP	SW-06F MAX	SW-06G MIN	SW-06G TYP	SW-06G MAX	UNITS
Positive Supply Current	I+	All Channels "OFF", DIS = "0" (Note 5)	–	5.0	6.0		5.0	9.0	–	6.0	9.0	mA
Negative Supply Current	I–	All Channels "OFF", DIS = "0" (Note 5)	–	3.0	5.0	–	4.0	7.0	–	4.0	7.0	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	–	3.0	4.0	–	3.0	4.0	–	3.0	5.0	mA

ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V, –55°C ≤ T_A ≤ +125°C for SW-06BQ, –40°C ≤ T_A ≤ +85°C for SW-06FQ and –40°C ≤ T_A ≤ +85°C for SW-06GP/GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06B MIN	SW-06B TYP	SW-06B MAX	SW-06F MIN	SW-06F TYP	SW-06F MAX	SW-06G MIN	SW-06G TYP	SW-06G MAX	UNITS
Temperature Range	T_A	Operating	–55	—	125	–25	—	85	0	—	70	°C
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 1.0mA V_S = ±10V, I_S = 1.0mA	— —	75 80	110 110	— —	75 80	125 125	— —	75 80	175 175	Ω
R_{ON} Match Between Switches	R_{ON} Match	V_S = 0V, I_S = 100μA (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	I_S = 1.0mA I_S = 1.0mA (Note 8)	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	+10 –10	+11 –15	— —	V
Analog Current Range	I_A	V_S = ±10.0V	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_S ≤ +10V, I_S = 1.0mA	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	V_S = 10V, V_D = –10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)}$+ $I_{D(ON)}$	V_S = V_D = ±10V, T_A = Max. Operating Temp. (Notes 5, 7)	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Current	I_{INH}	V_{IN} = 2.0V to 15.0V (Note 4)	—	—	10	—	—	10	—	—	15	μA
Logical "0" Input Current	I_{INL}	V_{IN} = 0.8V	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 2, 6)	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 2, 6)	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	t_{ON}–t_{OFF}	(Note 3)	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I+	All Channels "OFF" DIS = "0" (Note 5)	—	—	9.0	—	—	13.5	—	—	13.5	mA
Negative Supply Current	I–	All Channels "OFF" DIS = "0" (Note 5)	—	—	7.5	—	—	10.5	—	—	10.5	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	—	—	6.0	—	—	7.5	—	—	7.5	mA

NOTES:

1. V_S = 0V, I_S = 100μA. Specified as a percentage of $R_{AVERAGE}$ where:
$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$
2. Guaranteed by design.
3. Switch is guaranteed by design to provide break-before-make operation.
4. Current tested at V_{IN} = 2.0V. This is worst case condition.
5. Switch being tested ON or OFF as indicated, V_{INH} = 2.0V or V_{INL} = 0.8V, per logic truth table.
6. Also applies to disable pin.
7. Parameter tested only at T_A = +125°C for military grade device.
8. Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than (V+) –4V.
9. Sample tested.

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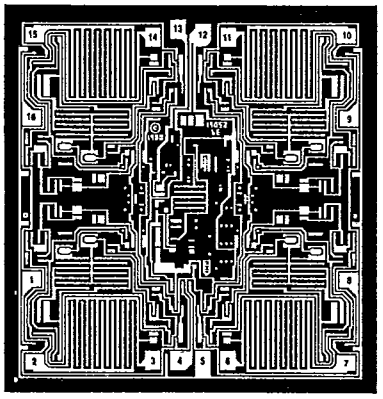
DICE CHARACTERISTICS



DIE SIZE 0.101 × 0.097 inch, 9797 sq. mils
(2.565 × 2.464 mm, 6.320 sq. mm)

1. IN (1)
2. D (1)
3. S (1)
4. GND
5. V– (SUBSTRATE)
6. S (2)
7. D (2)
8. IN (2)
9. IN (3)
10. D (3)
11. S (3)
12. V+
13. DISABLE
14. S (4)
15. D (4)
16. IN (4)

WAFER TEST LIMITS at V+ = 15V, V– = –15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N LIMIT	SW-06G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	80	100	Ω MAX
R_{ON} Match Between Switches	R_{ON} Match	V_A = 0V, $I_S \le 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	10	20	% MAX
Positive Supply Current	I+	(Note 1)	6.0	9.0	mA MAX
Negative Supply Current	I–	(Note 1)	5.0	7.0	mA MAX
Ground Current	I_G	(Note 1)	4.0	4.0	mA MAX
Analog Voltage Range	V_A	I_S = 1mA	±10.0	±10.0	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2.0	2.0	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \le V_{IN} \le 0.8V$	5.0	5.0	μA MAX
Logic "1" Input Current	I_{INH}	$2.0V \le V_{IN} \le 15V$ (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

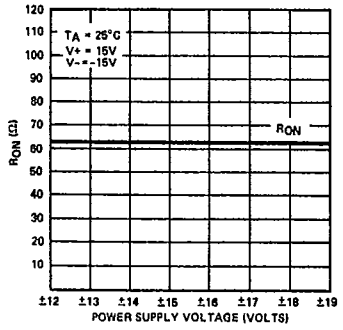
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V– = –15V and T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N TYPICAL	SW-06G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \le V_A \le 10V$, $I_S \le 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	V_S = 10V, V_D = –10V	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	f = 500kHz, R_L = 680Ω	58	58	dB
Crosstalk	C_T	f = 500kHz, R_L = 680Ω	70	70	dB

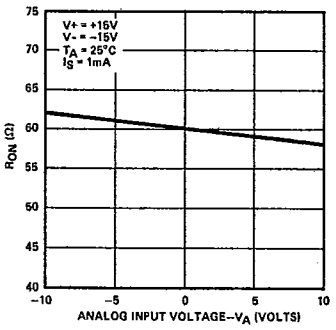
NOTES:
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at V_{IN} = 2.0V. This is worst case condition.
3. Guaranteed by R_{ON} and leakage tests.

TYPICAL PERFORMANCE CHARACTERISTICS

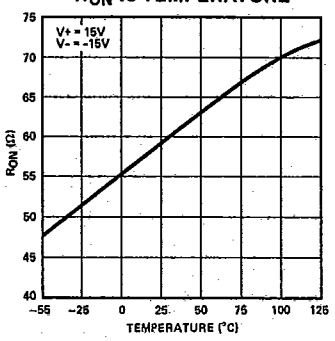
"ON" RESISTANCE vs POWER SUPPLY VOLTAGE



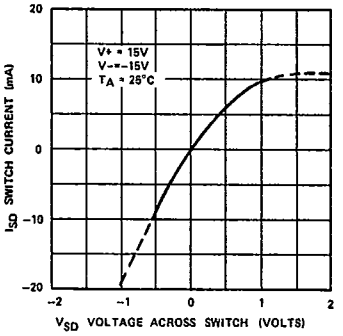
"ON" RESISTANCE vs ANALOG VOLTAGE



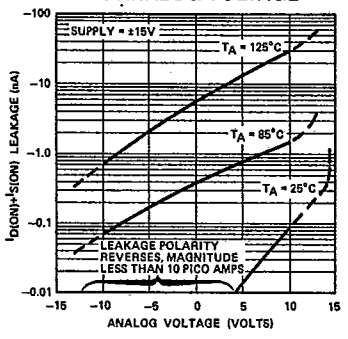
RON vs TEMPERATURE



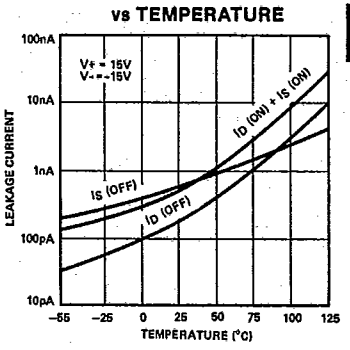
SWITCH CURRENT vs VOLTAGE



LEAKAGE CURRENT vs ANALOG VOLTAGE



LEAKAGE CURRENT vs TEMPERATURE



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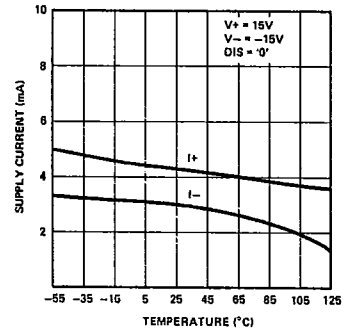
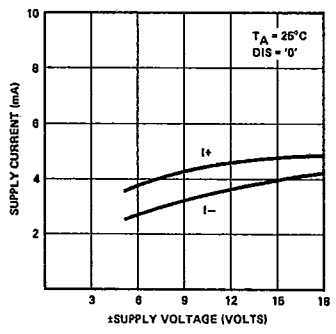
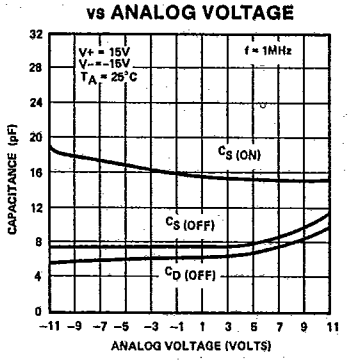
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE

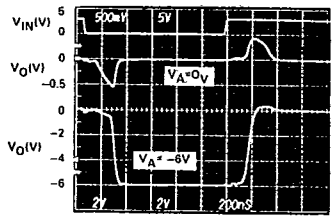


SWITCH CAPACITANCE vs ANALOG VOLTAGE

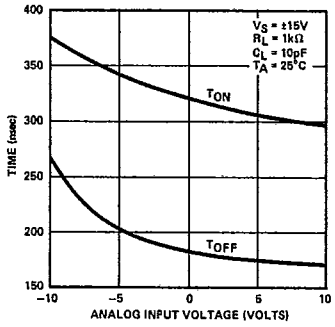


TYPICAL PERFORMANCE CHARACTERISTICS

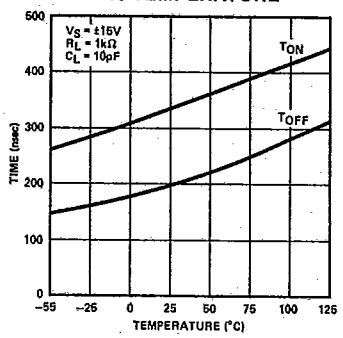
T_{ON}/T_{OFF} SWITCHING RESPONSE



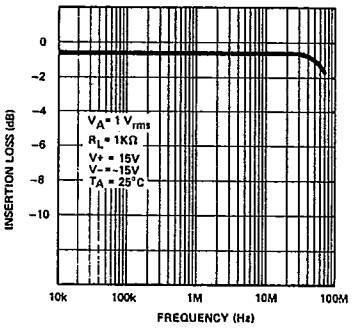
SWITCHING TIME vs ANALOG VOLTAGE



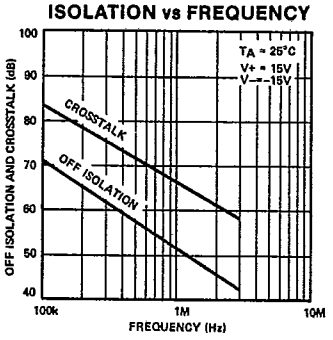
SWITCHING TIME vs TEMPERATURE



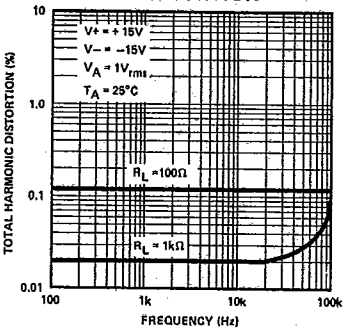
INSERTION LOSS vs FREQUENCY



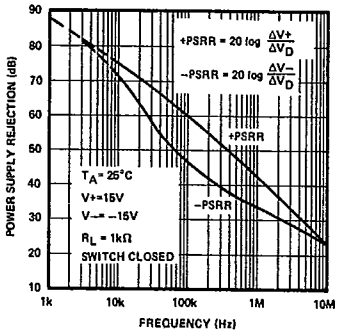
CROSSTALK AND "OFF" ISOLATION vs FREQUENCY



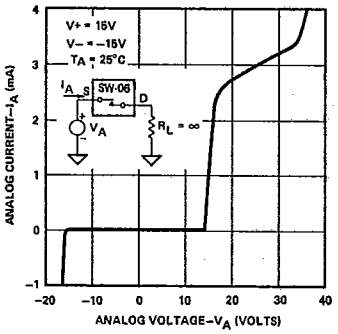
TOTAL HARMONIC DISTORTION



POWER SUPPLY REJECTION vs FREQUENCY

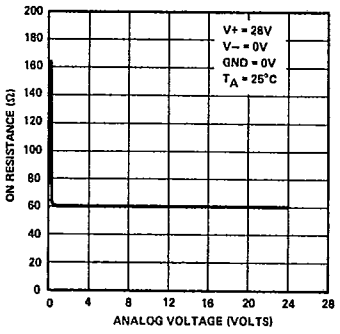


OVERVOLTAGE CHARACTERISTICS

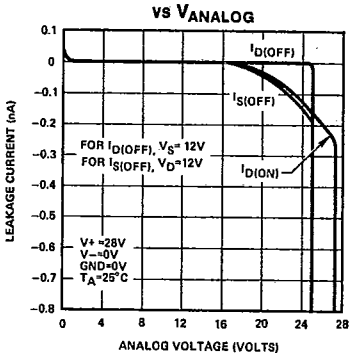


TYPICAL PERFORMANCE CHARACTERISTICS (OPERATING SINGLE SUPPLY)

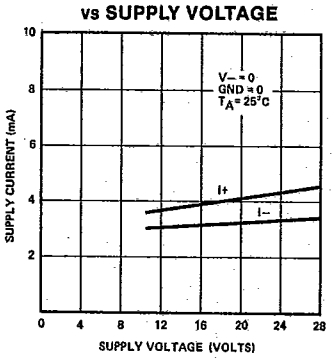
"ON" RESISTANCE vs ANALOG VOLTAGE



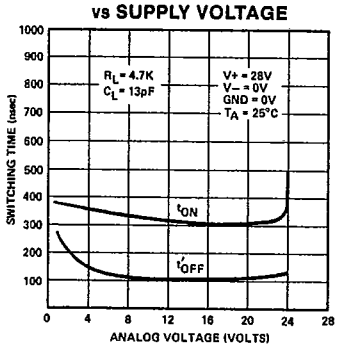
LEAKAGE CURRENT vs V_{ANALOG}



SUPPLY CURRENT vs SUPPLY VOLTAGE



SWITCHING TIME vs SUPPLY VOLTAGE



NOTE: These single-supply-operation characteristic curves are valid when the negative power supply V– is tied to the logic ground reference pin "GND". TTL input compatibility is still maintained when "GND" is the same potential as the TTL ground. t'_{OFF} is measured from 50% of logic input waveform to 0.9 V_O. The analog voltage range extends from 0 to V+ –4V, the switch will no longer respond to logic control when V_A is within 4 volts of V+.

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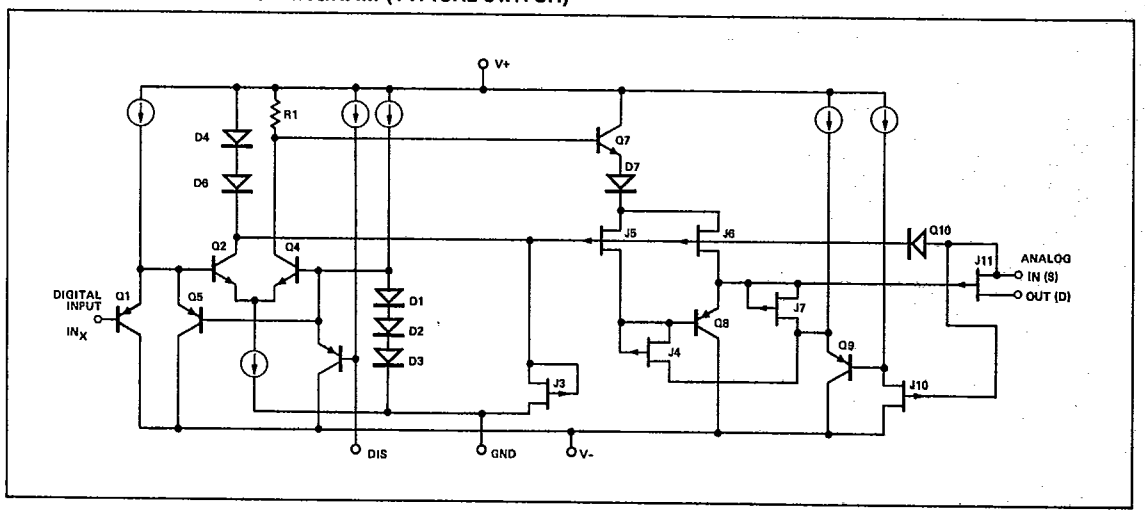
SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)



SW-06

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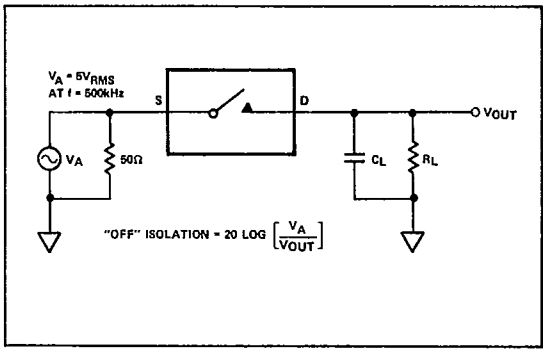
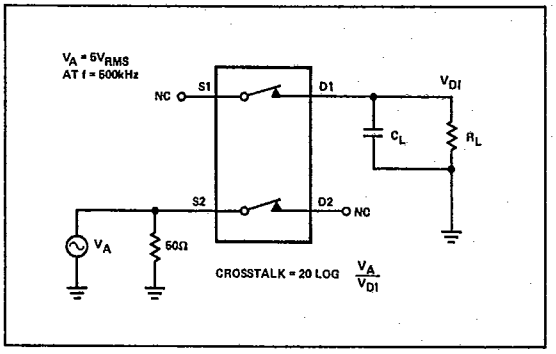
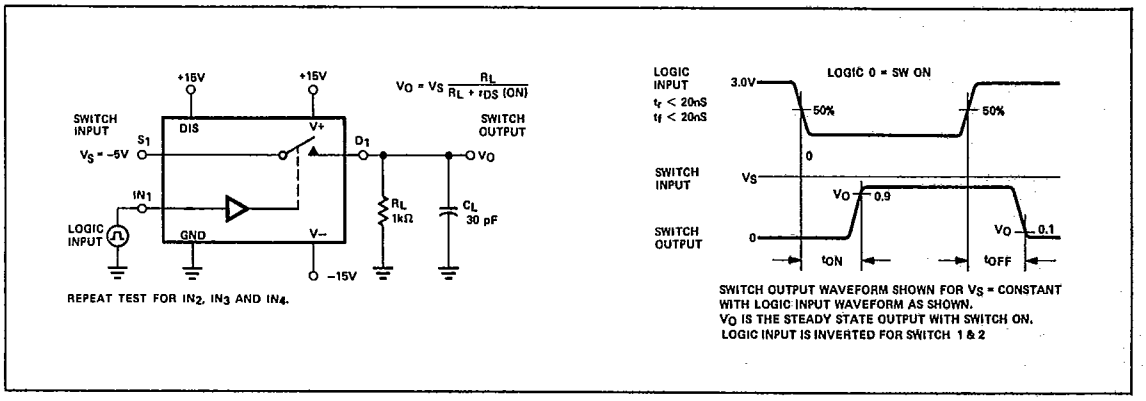
OFF ISOLATION TEST CIRCUIT



CROSSTALK TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



ANALOG CURRENT

The analog switches in the ON state are JFETs biased in their triode region and act as switches for analog current up to the I_A specification (see plot of I_{DS} vs V_{DS}). Some applications require pulsed currents exceeding the I_A spec. For example, an integrator reset switch discharging a shunt capacitor will produce a peak current of $I_{A(PEAK)} = V_{CAP}/R_{DS(ON)}$. In this application, it is best to connect the source to the most positive end of the capacitor, thereby achieving the lowest switch resistance and fastest reset times. The switch can easily handle any amount of capacitor discharge current subject only to the maximum heat dissipation of the package and the maximum operating junction temperature from which repetition rates can be established.

SWITCHING

Switching time t_{ON} and t_{OFF} characteristics are plotted versus V_{ANALOG} and temperature. In all cases, t_{OFF} is designed faster than t_{ON} to insure a break-before-make interval for SPDT and DPDT applications. The disable input (DIS) has the same switching times (t_{ON} and t_{OFF}) as the logic inputs (IN_X).

Switching transients occurring at the source and drain contacts results from AC coupling of the switching FETs gate-to-source and gate-to-drain coupling capacitance. The switch turn ON will cause a negative going spike to occur and the turn OFF will cause a positive spike to occur. These spikes can be reduced by additional capacitance loading, lower values of R_L, or switching an additional switch (with its extra contact floating) to the opposite state connected to the spike sensitive node.

DISABLE NODE

This TTL compatible node is similar to the logic inputs IN_X but has an internal 2μA current source pull-up. If disable is left unconnected, it will assume the logic "1" state, then the state of the switches is controlled only by the logic inputs IN_X.

POWER SUPPLIES

This product operates with power supply voltages ranging from ±12 to ±18 volts; however, the specifications only guarantee device parameters with ±15 volt ±5% power supplies. The power supply sensitive parameters have plots to indicate effects of supply voltages other than ±15 volts.

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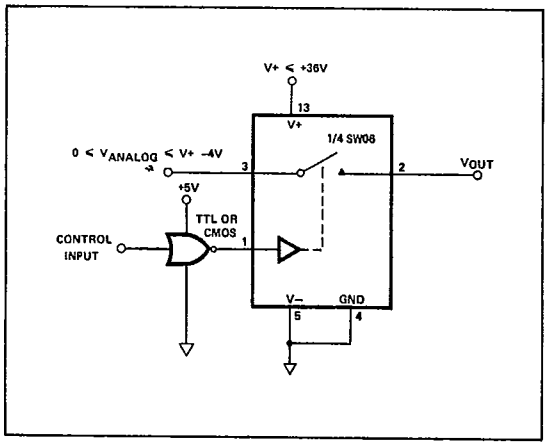
TYPICAL APPLICATIONS

OPERATION FROM SINGLE POSITIVE POWER SUPPLY



4-CHANNEL SAMPLE HOLD AMPLIFIER

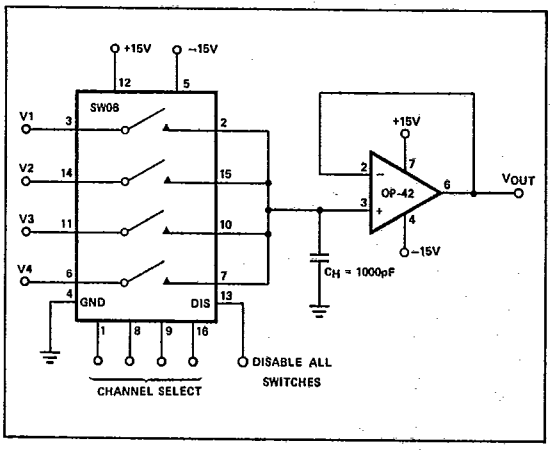


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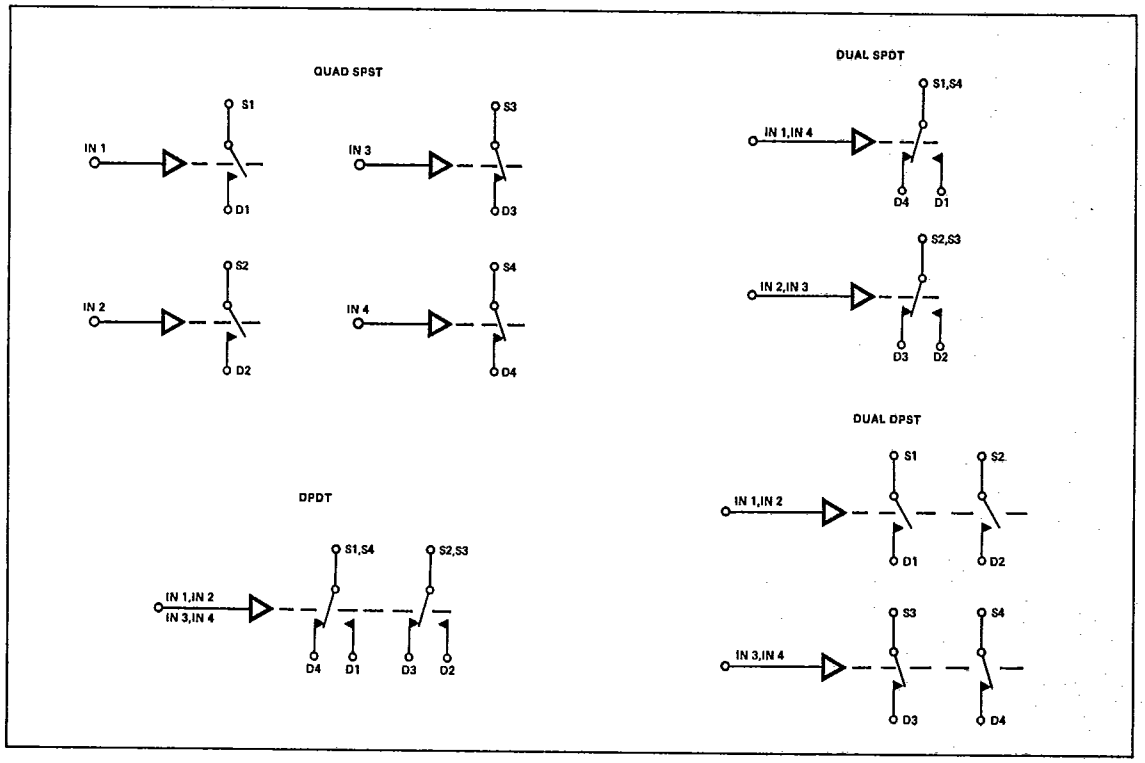
Figure 1: Functional Applications of SW-06



APPLICATIONS INFORMATION

This single analog switch product configures, by appropriate pin connections, into four switch applications. As shown in Figure 1, the SW-06 connects as a QUAD SPST, a DUAL SPDT, a DUAL DPST, or a DPDT analog switch. This versatility increases further when taking advantage of the disable input (DIS) which turns all switches OFF when taken active low.

Ion-implantation of the JFET analog switch achieves low ON resistance and tight channel to channel matching. Combining the low ON resistance and low leakage currents results in a worst case voltage error figure V_{ERROR} @ 125° C = $I_{D(ON)} \times R_{SD(ON)} = 100nA \times 100\Omega = 11$ microvolts. This amount of error is negligible considering dissimilar-metal thermally-induced offsets will be in the 5 to 15 microvolt range.

LOGIC INPUTS

The logic inputs (IN_X) and disable input (DIS) are referenced to a TTL logic threshold value of two forward diode drops (1.4V at 25° C) above the GND terminal. These inputs use PNP transistors which draw maximum current at a logic "0" level and drops to a leakage current of a reverse biased diode as the logic input voltage raises above 1.4 volts. Any logic input voltage greater than 2.0 volts becomes logic "1", less than 0.8 volts becomes logic "0" resulting in full TTL noise immunity not available from similar CMOS input analog switches. The PNP transistor inputs require such low input current that the SW-06 approaches fan-ins of CMOS input devices. These bipolar logic inputs exceed any CMOS input circuit in resistance to static voltage and radiation susceptability. No damage will occur to the SW-06 if logic high voltages are present when the SW-06 power supplies are OFF. When the V+ and V− supplies are OFF, the logic inputs present a reverse bias diode loading to active logic inputs. Input logic thresholds are independent of V+ and V− supplies making single V+ supply operation possible by simply connecting GND and V− together to the logic ground supply.

ANALOG VOLTAGE AND CURRENT

ANALOG VOLTAGE

These switches have constant ON resistance for analog voltages from the negative power supply (V−) to within 4 volts of the positive power supply. This characteristic shown in the plots results in good total harmonic distortion, especially when compared to CMOS analog switches that have a 20 to 30 percent variation in ON resistance versus analog voltage. Positive analog input voltages should be restricted to 4 volts less than V+ assuring the switch remains open circuit in the OFF state. No increase in switch ON resistance occurs when operating at supply voltages less than ±15 volts (see plot). Small signals have a 3dB down frequency of 70MHz (see insertion loss versus frequency plot).

SW-06

HIGH OFF ISOLATION SELECTOR SWITCH (Shunt-Series Switch)

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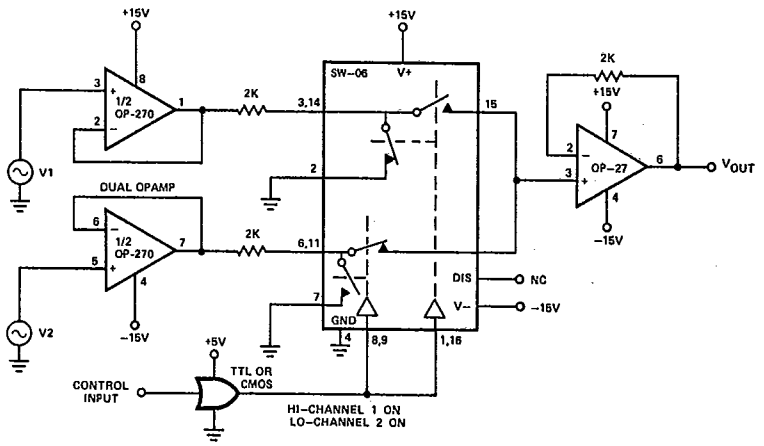

THIS SWITCH ARRANGEMENT IMPROVES OFF ISOLATION BY 30dB

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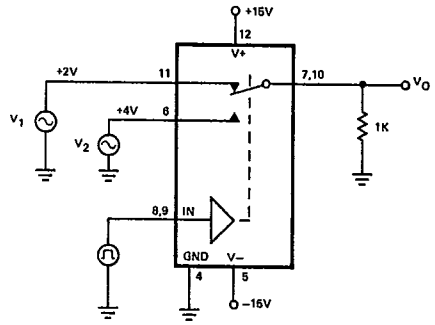
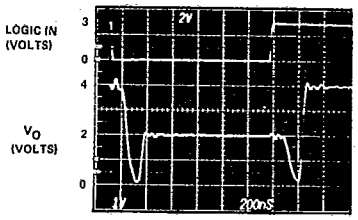
SINGLE POLE DOUBLE THROW SELECTOR SWITCH WITH BREAK-BEFORE-MAKE INTERVAL





During the BBM interval the 1kΩ resistor pulls the output to ground assuring that no shorting between V_1 and V_2 occurs.