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SV92P PCI Soft Modem Chip Set

Features

- Two-chip 3.3 V soft modem solution with an integrated 5 V tolerant PCI interface
- Data mode capabilities:
  - ITU-T V.92*: 56000 bits/s—28000 bits/s
  - ITU-T V.90*: 56000 bits/s—28000 bits/s
  - ITU-T V.34: 33600 bits/s—2400 bits/s
  - V.32bis, and fallbacks
  - V.42 and *MNP* error correction (LAPM)
  - V.44, V.42bis and *MNP* Class 5 data compression
- FAX mode capabilities:
  - ITU-T V.17, V.29, V.27ter, and V.21 Ch 2
  - ITU-T T.31 Class 1 FAX
- Compatible with transformer-based and silicon DAA circuits:
  - High-precision sigma-delta codec (CSP1034C)
  - Line-powered silicon DAA (CSP1035A)
- Bit I/Os to support domestic and international DAAs
- Supports standard PCI and mini PCI buses with PCI version 2.2
- Ideal for mobile computing and high-performance/low-power applications
- Flexible power management modes
- Common driver across multiple platforms
- Operating system support:
  - *Windows* 98, *Windows* 2000, *Windows ME* ™, and *Windows XP* ™
  - PC 2001 compliant

Introduction

The SV92P chip set is Agere Systems' latest soft modem solution. The chip set features the new SV92P PCI interface device, the CSP1034C line codec or the CSP1035A data access arrangement (DAA), and a soft modem stack.

The SV92P device provides an interface between the host system running the soft modem stack and line codec or DAA. The SV92P defers all modem protocol processing to the soft modem stack and functions primarily as a buffering interface.

SV92P is both pin and footprint compatible with the *Mars* 3 host-based controller modems. Designs based on the DSP1648x products are easily migrated to the SV92P with the addition of the soft modem stack.

The soft modem stack performs all of the modem protocol processing including support for ITU-T recommendation V.92/V.44. V.92 and V.44 have four innovative features, designed to improve modem performance in the internet environment. The features are as follows:

- Modem fast connect: faster start-up times on recognized connections.
- Modem on hold†: switch between modem and an incoming phone call without losing the data connections.
- PCM upstream: send data to central site at rates approaching 48 kbits/s.
- Data compression enhancement focused on todays internet traffic.

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* Due to FCC limitations, speeds of 53 kbits/s are the maximum permissible transmit power levels during download transmission. Actual data speeds will vary depending on the line conditions.

† Modem on hold functionality is dependent on country specific call waiting services. Not all countries are supported.

Functional Description

The Agere Systems SV92P chip set is a two-chip solution consisting of a Agere Systems SV92P PCI interface device and a CSP1035 silicon DAA or the CSP1034 line codec. It supports V.92, V.90, V.34 data, and FAX rates up to 14.4 kbits/s.

The SV92P is an interface device with the memory required for receiving, transmitting, and buffering data sent between the host system (soft modem stack) and the DAA or line codec. The SV92P has the following three interfaces:

- PCI: SV92P uses the PCI interface to communicate with the host system or soft modem stack. This interface has two bus mastering streams and 5 V tolerant buffers. With this interface, the SV92P can take control of the local bus and exchange data directly with the host system RAM.

- Serial input/output (SIO): SV92P uses the SIO port to interface with the CSP1034C line codec. The CSP1034C uses a transformer to interface the high-voltage analog portion of the circuit.

- Differential input/output: SV92P uses the DIO port to interface with the CSP1035A DAA. The CSP1035A has an integrated line codec and is part of the line interface. The CSP1035A sits on the high voltage side of the modem circuit. It interfaces with the SV92P via a digital isolation barrier connected to the DIO port (For more information on the CSP1035A and the digital isolation barrier see the *Line Powered DAA-CSP1035A* Data Sheet.)

    The DIO port is multiplexed with the SIO port.

Integrated SV92P with PCI

The SV92P incorporates a PCI interface which is compliant with PCI local bus specification revision 2.2. The interface also supports two full-duplex bus master streams for greater access to host system resources. The interface supports both 3.3 V and 5 V signaling systems. However, the device supply must come from a 3.3 V PCI supply, Vaux, or a regulated 3.3 V supply.

I/O Voltage Considerations

The system supply voltage requirement is 3.3 V ± 0.3 Vdc. This device also employs 5 V tolerant PCI buffers. To support this 5 V tolerant I/O, the VIO pin is provided as an indicator to the device of the signaling voltage being used on the bus.
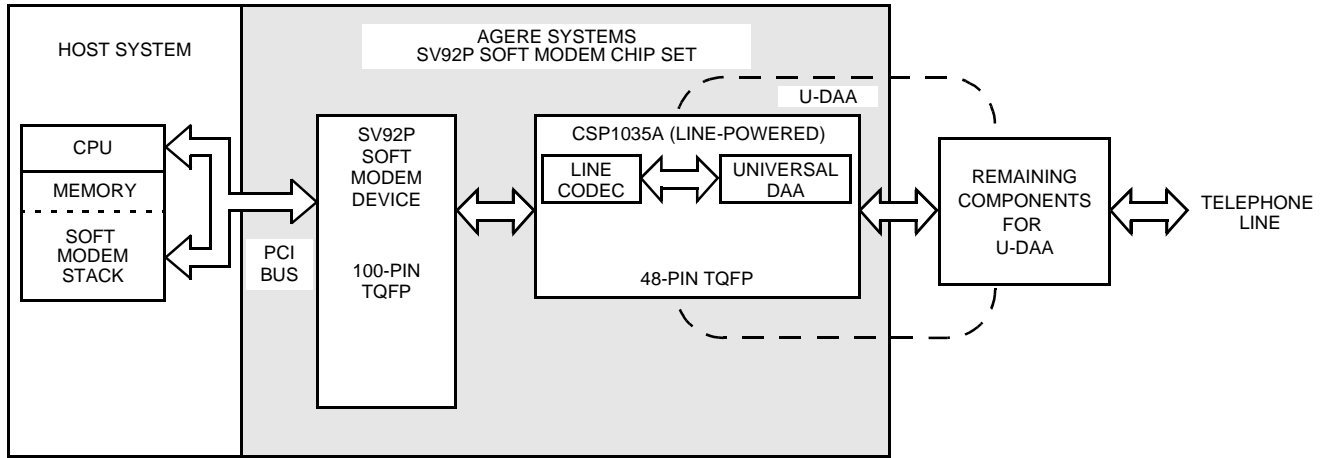
System Support and Requirements

The SV92P supports *Windows* 98, *Window*s *ME*, *Windows* 2000, *Windows NT* 4.0, and *Windows XP*. It is designed to operate on any *pentium* class CPU which meets the following system requirements:

- *Pentium*® 200 MHz with 32 Mbytes of RAM
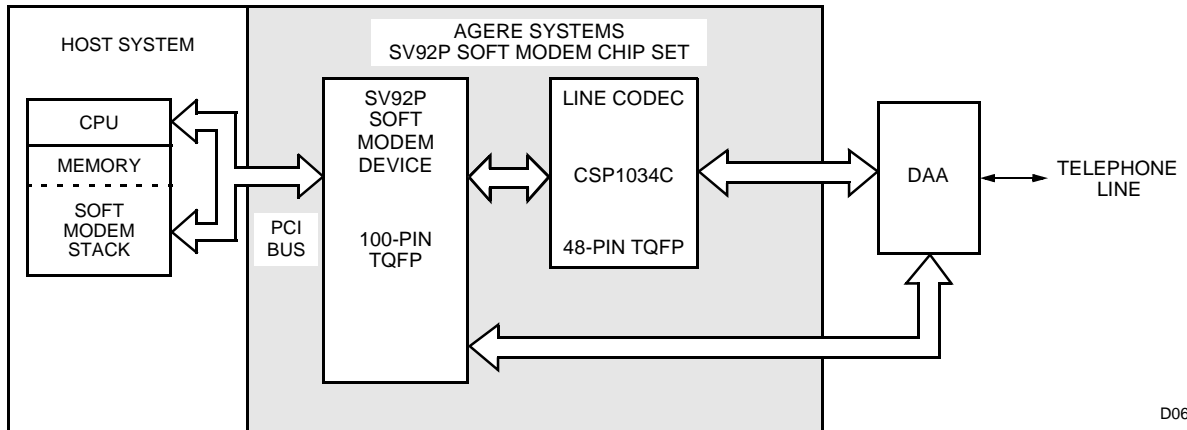- *AMD* ® K6 200 MHz with 32 Mbytes of RAM

Functional Description (continued)

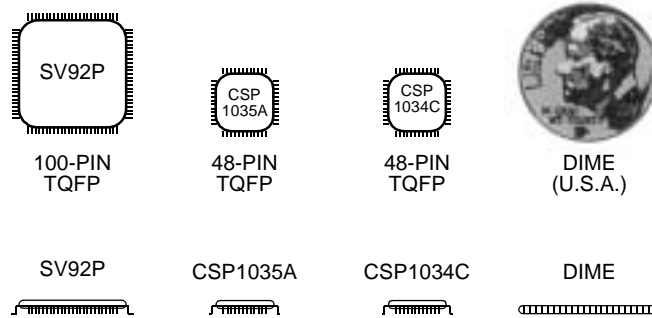### SV92P Block Diagram

0670.b (F)

Figure 1. Agere Systems SV92P/CSP1035A Soft Modem Chip Set Block Diagram

D0670 (f)e

Figure 2. Agere Systems SV92P/CSP1034 Soft Modem Chip Set Block Diagram

Package Information

Figure 3. SV92P Chip Set Package Options

0671.a (f)

Ordering Information

Device	Part Number	Package	Comcode	Voltage
SV92P	SV92P-T00-SV-DB	100-Pin TQFP	108889445	3.3 V with 5 V tolerant buffers
CSP1034C	CSP1034C-T11-DB	48-Pin TQFP	108159542	3.3 V nominal
CSP1035A	CSP1035A-T11-DB	48-Pin TQFP	108877069	Line powered

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