



SPICE Device Model SUM110P04-05

Vishay Siliconix

P-Channel 40-V (D-S) MOSFET

CHARACTERISTICS

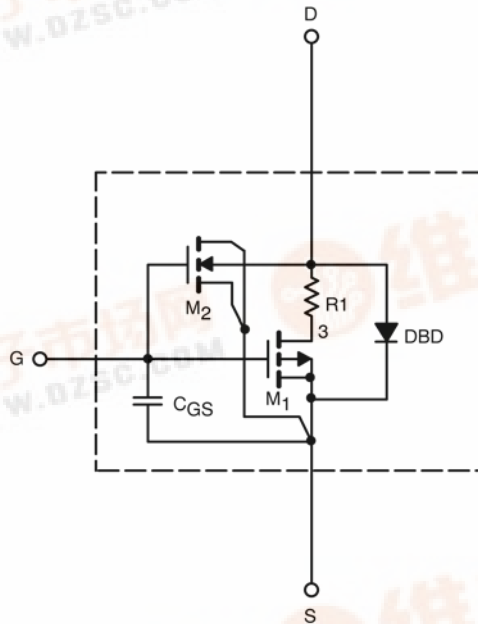
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



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| SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---------------------|--|----------------|---------------|------|
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
| Static | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = -250 μA | 2.8 | | V |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} ≥ -5 V, V _{GS} = -10 V | 982 | | A |
| Drain-Source On-State Resistance ^a | r _{DS(on)} | V _{GS} = -10 V, I _D = -20 A | 0.0040 | 0.0041 | Ω |
| Forward Transconductance ^a | g _{fs} | V _{DS} = -15 V, I _D = -20 A | 126 | 75 | S |
| Diode Forward Voltage ^a | V _{SD} | I _S = -20 A | -0.88 | -80 | V |
| Dynamic^b | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = -25 V, f = 1 MHz | 9687 | 11300 | pF |
| Output Capacitance | C _{oss} | | 1524 | 1510 | |
| Reverse Transfer Capacitance | C _{rss} | | 844 | 1000 | |
| Total Gate Charge ^c | Q _g | V _{DS} = -20 V, V _{GS} = -10 V, I _D = -20 A | 195 | 185 | nC |
| Gate-Source Charge ^c | Q _{gs} | | 48 | 48 | |
| Gate-Drain Charge ^c | Q _{gd} | | 42 | 42 | |

Notes

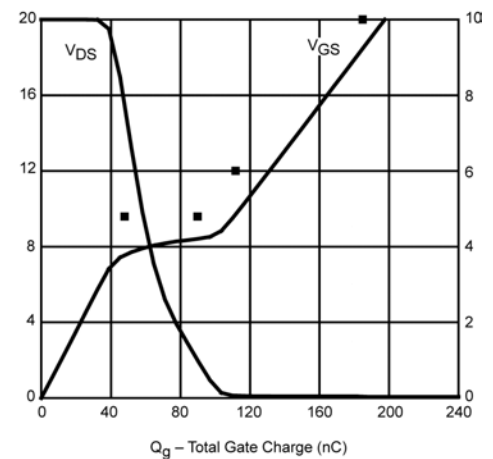
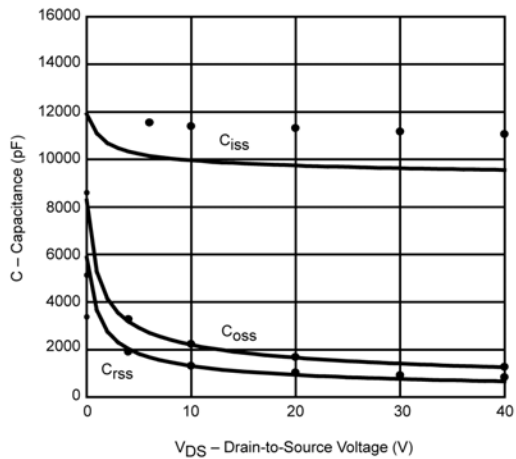
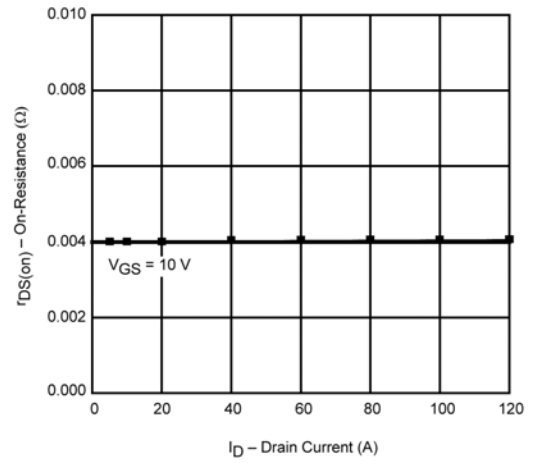
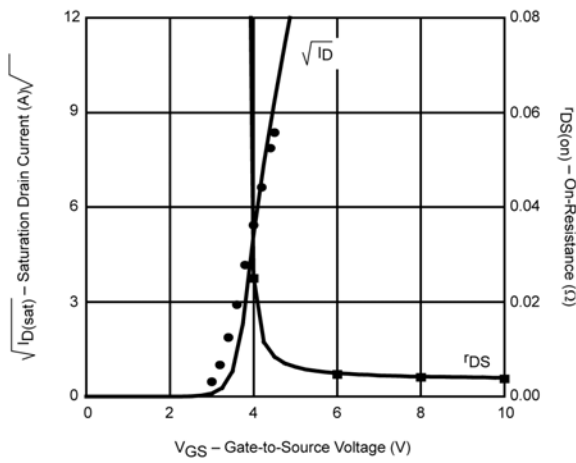
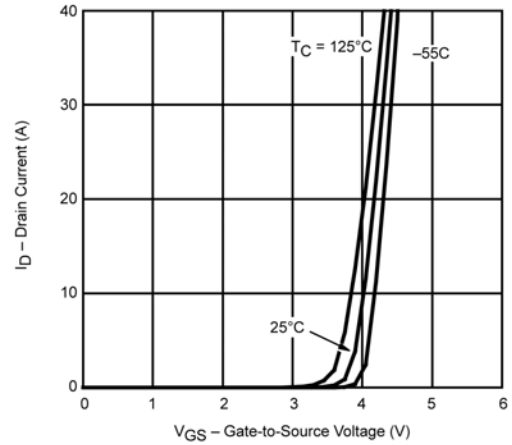
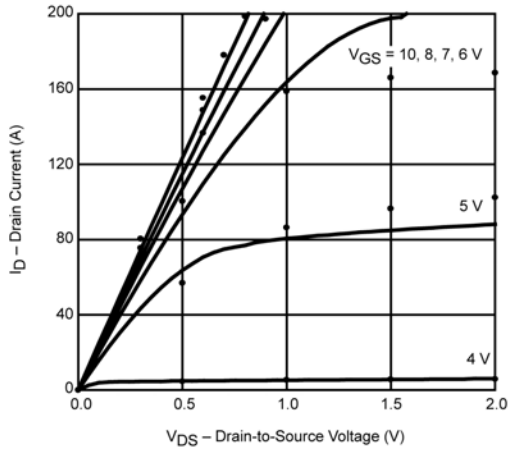
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.