STV0042A/Z

Analog Satellite Sound and Video Processor

Sound Features

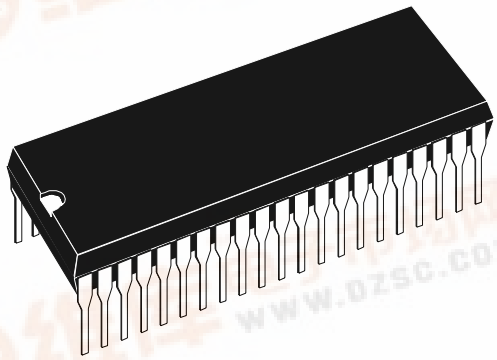
- Two Independent Sound Demodulators
- PLL Demodulation with 5-10 MHz Frequency Synthesis
- Programmable FM Demodulator Bandwidth accommodating FM Deviations between ±30 and ±400 kHz
- Programmable 50/75 µs or No De-emphasis
- Dynamic Noise Reduction (ANRS)
- One or Two Auxiliary Audio Inputs and Outputs
- Gain-controlled and Mutable Audio Outputs
- High-impedance Mode Audio Outputs for Twin Tuner Applications

Video Features

- Composite 6-bit Video with 0 to 12.7 dB Gain Control
- Selectable Composite Video Inverter
- Two Selectable Video De-emphasis Networks
- 4 x 2 Video Matrix
- High-impedance Mode Video Outputs for Twin Tuner Applications

Miscellaneous Features

- 22 kHz Tone Generation for LNB Control
- I²C Bus Control: Chip Addresses = 06h
- Low Power Stand-by Mode with Active Audio and Video Matrices



SHRINK42
(Shrink Plastic Dual In-Line Package)

ORDER CODE: STV0042A/Z

General Description

The STV0042 BICMOS integrated circuit is designed for low-cost analog satellite receiver applications.

The STV0042A/Z performs all the necessary signal processing from the tuner to the Audio/Video input and output connectors regardless of the satellite system.

Table of Contents

1 General Information

1.1 Pin Description

Figure 1: Pin Connections

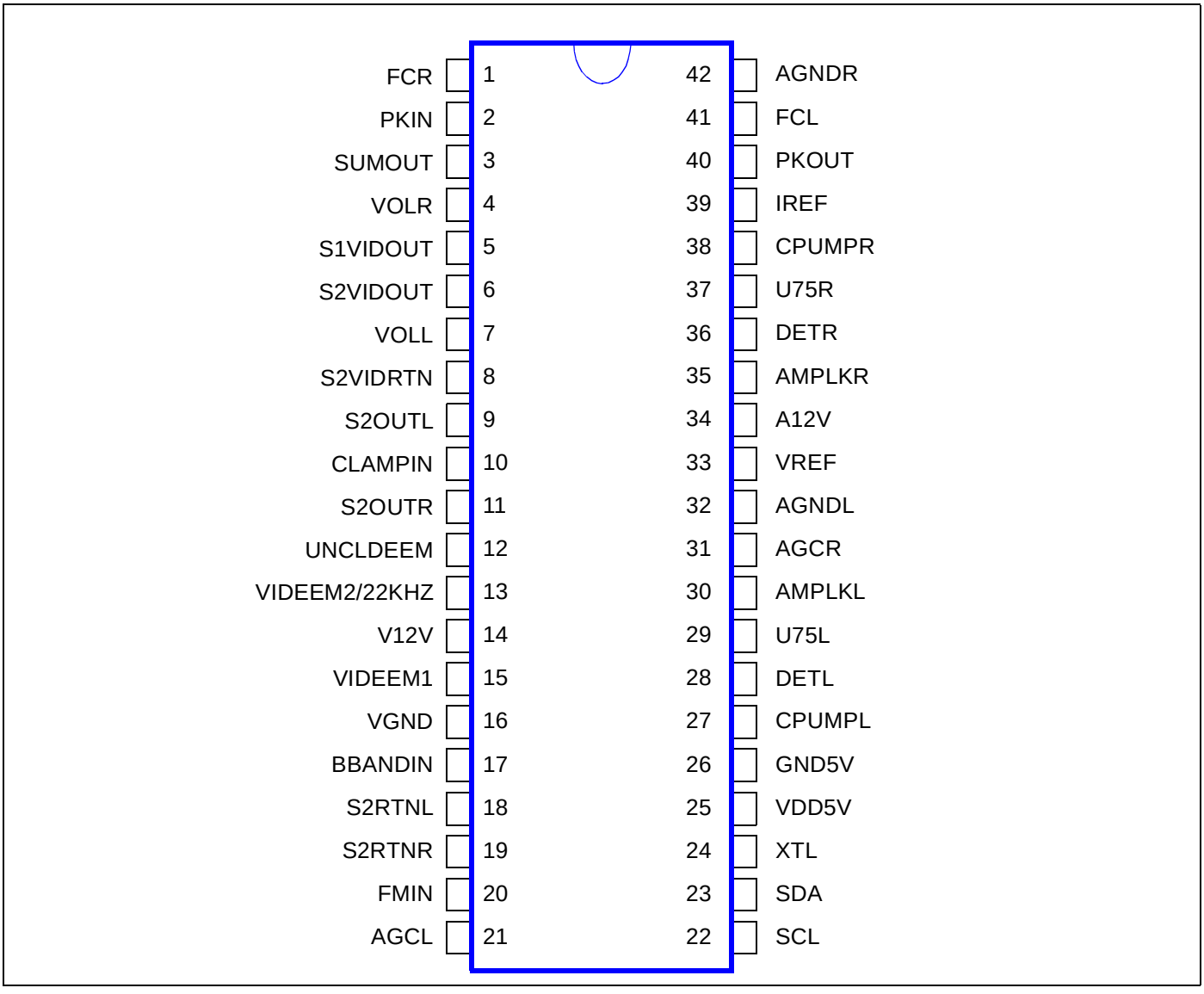


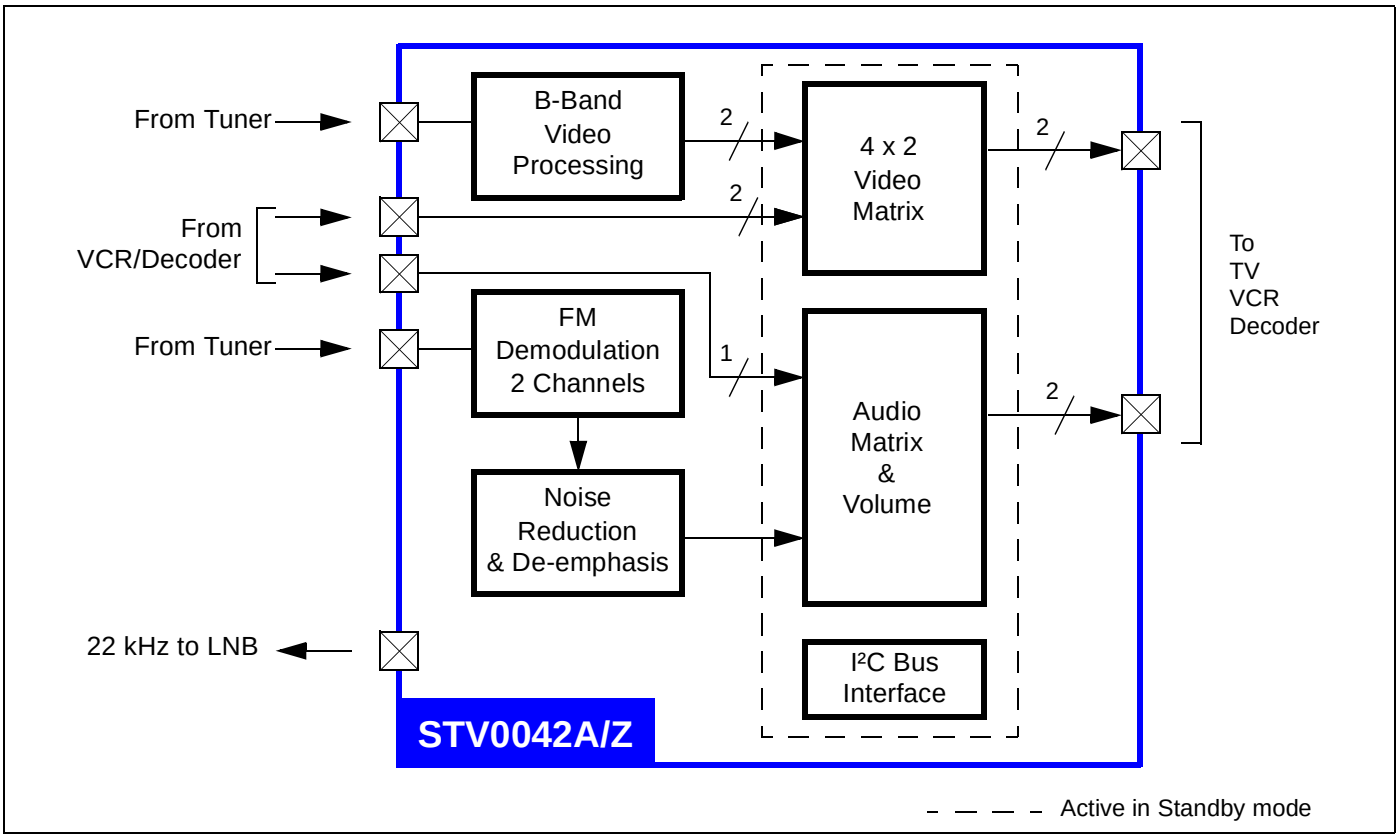
Table 1: Pin Description (Sheet 1 of 2)

Pin No.	Name	Function
1	FCR	Audio Roll-off Right
2	PKIN	Noise Reduction Peak Detector Input
3	SUMOUT	Noise Reduction Summing Output
4	VOLR	Right Volume-controlled Audio Output
5	S1VIDOUT	TV SCART Video Output 1
6	S2VIDOUT	VCR SCART Video Output 2
7	VOLL	Left Volume-controlled Audio Output

Table 1: Pin Description (Sheet 2 of 2)

Pin No.	Name	Function
8	S2VIDRTN	VCR SCART Video Return 2
9	S2OUTL	Left Fixed Level Audio Output
10	CLAMPIN	Sync Tip Clamp Input
11	S2OUTR	Right Fixed Level Audio Output
12	UNCLDEEM	Unclamped De-emphasized Video Output
13	VIDEEM2/22KHZ	Video De-emphasis 2 or 22 kHz Output
14	V12V	12 V Video Power Supply
15	VIDEEM1	Video De-emphasis 1
16	VGND	Video Ground
17	BBANDIN	Base Band Input
18	S2RTNL	Left Auxiliary Audio Return
19	S2RTNR	Right Auxiliary Audio Return
20	FMIN	FM Demodulator Input
21	AGCL	Left AGC Peak Detector Capacitor
22	SCL	I²C Bus Clock
23	SDA	I²C Bus Data
24	XTL	4/8 MHz Crystal Oscillator or Clock Input
25	VDD5V	Digital 5 V Power Supply
26	GND5V	Digital Ground
27	CPUMPL	Left FM PLL Charge Pump Capacitor
28	DETL	Left FM PLL Filter
29	U75L	Left De-emphasis Time Constant
30	AMPLKL	Left Amplitude Detector Capacitor
31	AGCR	Right AGC Peak Detector Capacitor
32	AGNDL	Left Audio Ground
33	VREF	2.4 V Reference Power Supply
34	A12V	12 V Audio Power Supply
35	AMPLKR	Right Amplitude Detector Capacitor
36	DETR	Right FM PLL Filter
37	U75R	Right De-emphasis Time Constant
38	CPUMPR	Right FM PLL Charge Pump Capacitor
39	IREF	Current Reference Resistor
40	PKOUT	Noise Reduction Peak Detector Output
41	FCL	Left Audio Roll-off
42	AGNDR	Right Audio Ground

Figure 2: STV0042A/Z General Block Diagram



1.1.1 Sound Detection

1.1.1.1 FM Demodulators

A block diagram of the FM Demodulation block is shown in Figure 3.

Pin FMIN (pin 20) is the input to the two FM demodulators. It feeds two AGC amplifiers with a bandwidth of at least 5 to 10 MHz. There is one amplifier for each channel. Both channels have the same input. The AGC amplifiers have a range between 0 and +40 dB.

The input impedance (Z_{IN}) is 5 kΩ with a minimum input of 2 mV_{PP} per subcarrier and a maximum input of 500 mV_{PP}. This is the maximum value when all inputs are added together, when their phases coincide.

1.1.1.2 AGC Peak Detector Capacitors

Pins AGCL and AGCR (pins 21 and 31, respectively) are the AGC amplifier peak detector capacitor connections. The output current has an attack/decay ratio of 1:32. This means that the ramp-up current is approximately 5 µA and decay current is approximately 160 µA. 11V gives maximum gain. These pins are also driven by a circuit monitoring the voltage on pins AMPLKL and AMPLKR, respectively.

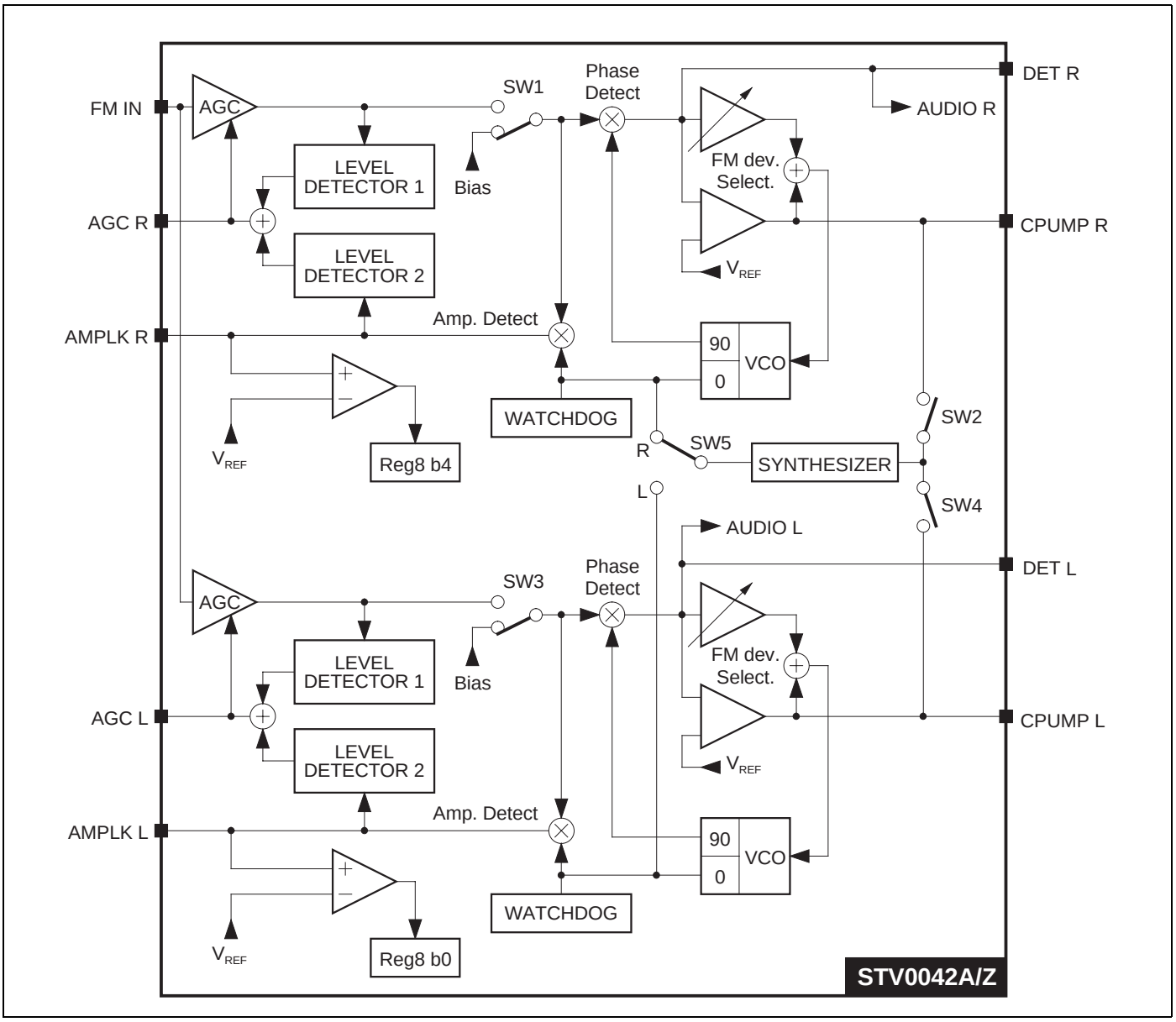
1.1.1.3 Amplitude Detector Capacitors

Pins AMPLKL and AMPLKR (pins 30 and 35, respectively) are the left and right outputs of their respective amplitude detectors. Each pin requires a capacitor and a resistor to GND. The voltage across these pins is used to decide whether a signal is being received by the FM detector. The level detector output drives a bit in the I²C bus detector control block. Pins AMPLKL and AMPLKR drive also respectively pins AGCL and AGCR. For instance, when the voltage on pin AMPLKL is > (V_{REF} + 1 V_{BE}) it sinks current to V_{REF} from pin AGCL in order to reduce the AGC gain.

1.1.1.4 FM PLL Filters

Pins DETL and DETR (pins 28 and 36, respectively) are the left and right outputs of their respective FM phase detectors. These pins are used to connect an external PLL loop filter. The output is a push-pull current source.

Figure 3: FM Demodulation



1.1.1.5 FM PLL Charge Pump Capacitors

Pins CPUMPL and CPUMPR (pins 27 and 38, respectively) are the FM PLL Charge Pump Capacitors. The output from the frequency synthesizer is a push-pull current source which requires capacitors to pull each VCO to the target frequency. The output is ±100 µA to achieve lock and ±2 µA during lock to provide a tracking time constant of approximately 10 Hz.

In order to prevent a false locking in certain marginal conditions, it is best to add a 8.2 V Zener diode to pins CPUMPL and CPUMPR.

1.1.1.6 Voltage Reference

Pin VREF (pin 33) is the audio processor voltage reference used throughout the FM/audio section of the chip. This pin must be correctly decoupled from to ground in order to reduce as much as possible the risk of crosstalk and noise injection. This voltage reference is directly derived from the bandgap reference of 2.4 V. The V_{REF} output can sink up to 500 µA in normal operation and 100 µA when in Standby mode.

1.1.1.7 Current Reference Resistor

Pin IREF (pin 39) is a buffered V_{REF} output to an off-chip resistor used to produce an accurate current reference, within the chip, for the biasing of amplifiers with current outputs into filters. It also provides accurate roll-off frequencies for the Noise Reduction circuit.

This pin should not be decoupled as this would inject current noise. The target current is 50 µA ±2%, therefore a 47.5 kΩ ±1% resistor is required.

1.1.1.8 12 V Audio Power Supply

Pin A12V (pin 34) is a double-bonded main power pin used by the Audio/FM section of the chip. The two bond connections are used for the ESD and to power the circuit and on-chip regulators/ references.

1.1.1.9 Audio Ground

Pins AGNDL and AGNDR (pins 32 and 42, respectively) are double-bonded ground pins.

Pin	Pad 1	Pad 2
AGNDL	Left Channel: RF Section and VCO	Both AGC Amplifiers, Channel Left and Right Audio Filter Section.
AGNDR	Right Channel: RF Section and VCO	Volume Control, Noise Reduction System, ESD + Multiplexer + V_{REF}

1.1.2 Baseband Audio Processing

1.1.2.1 Noise Reduction Peak Detector

The Noise Reduction Control Loop Peak Detector output (PKOUT pin (pin 40)) is connected to a capacitor to ground and to a resistor to the VREF pin in order to provide an accurate decay time constant. An on-chip 5 kΩ ±25% resistor and external capacitor give the attack time.

Pin PKIN (pin 2) is an input to a control loop peak detector and is connected to the output of the off-chip control loop band pass filter.

1.1.2.2 Noise Reduction Summing Output

A 0.5-gain amplifier is used to sum together the two audio demodulated signals. This value is then output on pin SUMOUT (pin 3). For example, if both inputs are equal to 1 V, then the output is 1 V. This amplifier has an input follower buffer which provides a V_{BE} offset in the DC bias voltage. Therefore, the filter driven by this amplifier must include AC coupling to the next stage (pin PKIN).

1.1.2.3 Audio Roll-off

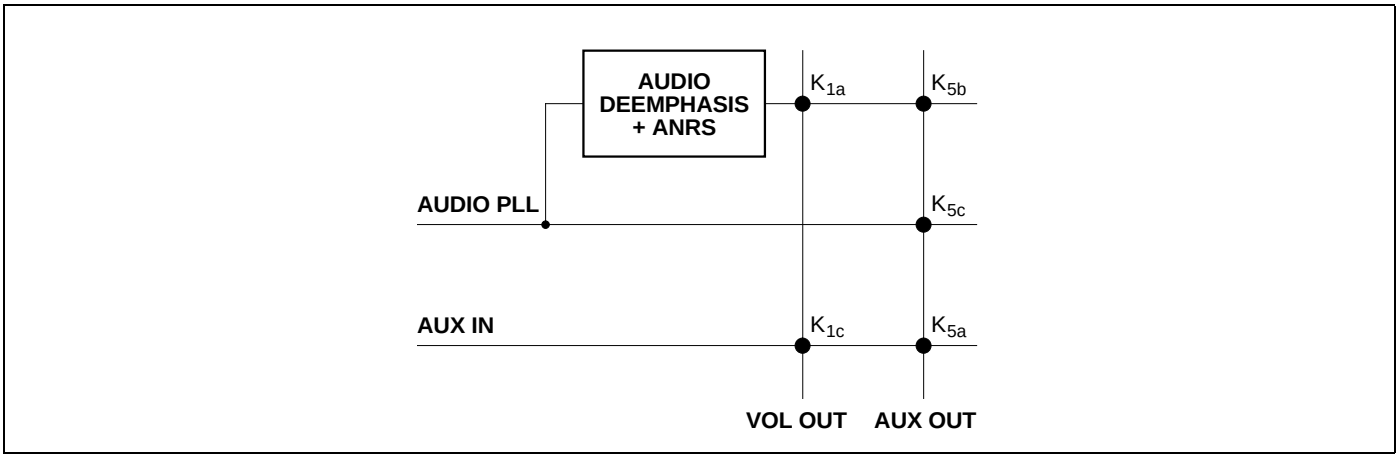
The variable bandwidth transconductance amplifier has a current output which is variable depending on the input signal amplitude as defined by the ANRS control loop. The output current is then dumped into an off-chip capacitor which together with the accurate current reference define

the minimum/maximum roll-off frequencies. A resistor in series with a capacitor is connected to the ground via pins FCL and FCR (pins 41 and 1, respectively).

1.1.2.4 De-emphasis Time Constants

Pins U75L and U75R (pins 29 and 37, respectively) are external de-emphasis networks for left and right channels. For each channel, a capacitor and resistor in parallel with a 75 µs time constant are connected to the V_{REF} to provide a 75 µs de-emphasis. An internal resistor can be programmed to be added in parallel thereby converting the network to approximately 50 µs de-emphasis. The value of the internal resistors is 30 kΩ ±30%. The amplifier for this filter is voltage input, current output; with ±500 mV input the output will be ±55 µA.

Figure 4: Audio Switching



K_2	K_3	
a	On	No ANRS, No de-emphasis
b_1	On	No ANRS, 50 µS
b_2	On	No ANRS, 75 µS
a	Off	ANRS, No de-emphasis
b_1	Off	ANRS, 50 µS
b_2	Off	ANRS, 75 µS

1.1.2.5 Volume-controlled Audio Outputs

Pins VOLL and VOLR (pins 7 and 4, respectively) are the main audio outputs from the volume control amplifier. Output signals may be as high as 2 V_{RMS} (+12 dB) with a DC bias of 4.8 V. The volume control is between +12 dB and -26.75 dB in steps of 1.25 dB with possible Mute. This amplifier has short-circuit protection and is intended to drive a SCART connector directly via AC coupling and meets the standard SCART drive requirements. These outputs feature high impedance mode for parallel connections.

1.1.2.6 Fixed-level Audio Outputs

Pins S2OUTL and S2OUTR (pins 9 and 11, respectively) are audio outputs that are directly sourced from the audio multiplexer, and as a result do not include any volume control functions. They will output a 1 V_{RMS} signal biased at 4.8 V. They are short-circuit protected. These outputs feature high impedance mode for parallel connections and meet SCART drive requirements.

1.1.2.7 Auxiliary Audio Returns

Pins S2RTNL and S2RTNR (pins 18 and 19, respectively) allow auxiliary audio signals to be connected to the audio processor and therefore make use of the on-chip volume control. For additional details please refer to the audio switching table.

Figure 5: Audio Signal Processing Diagram (Left)

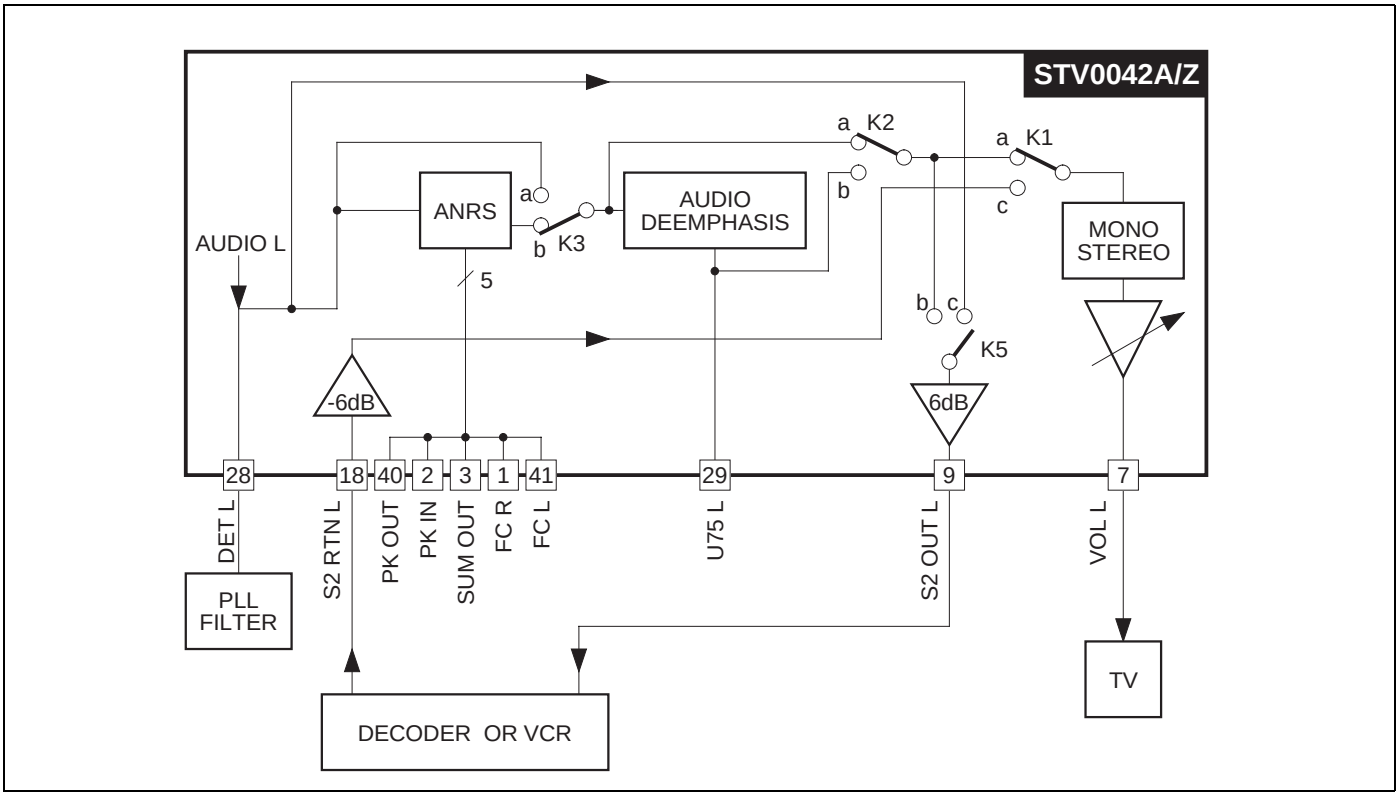
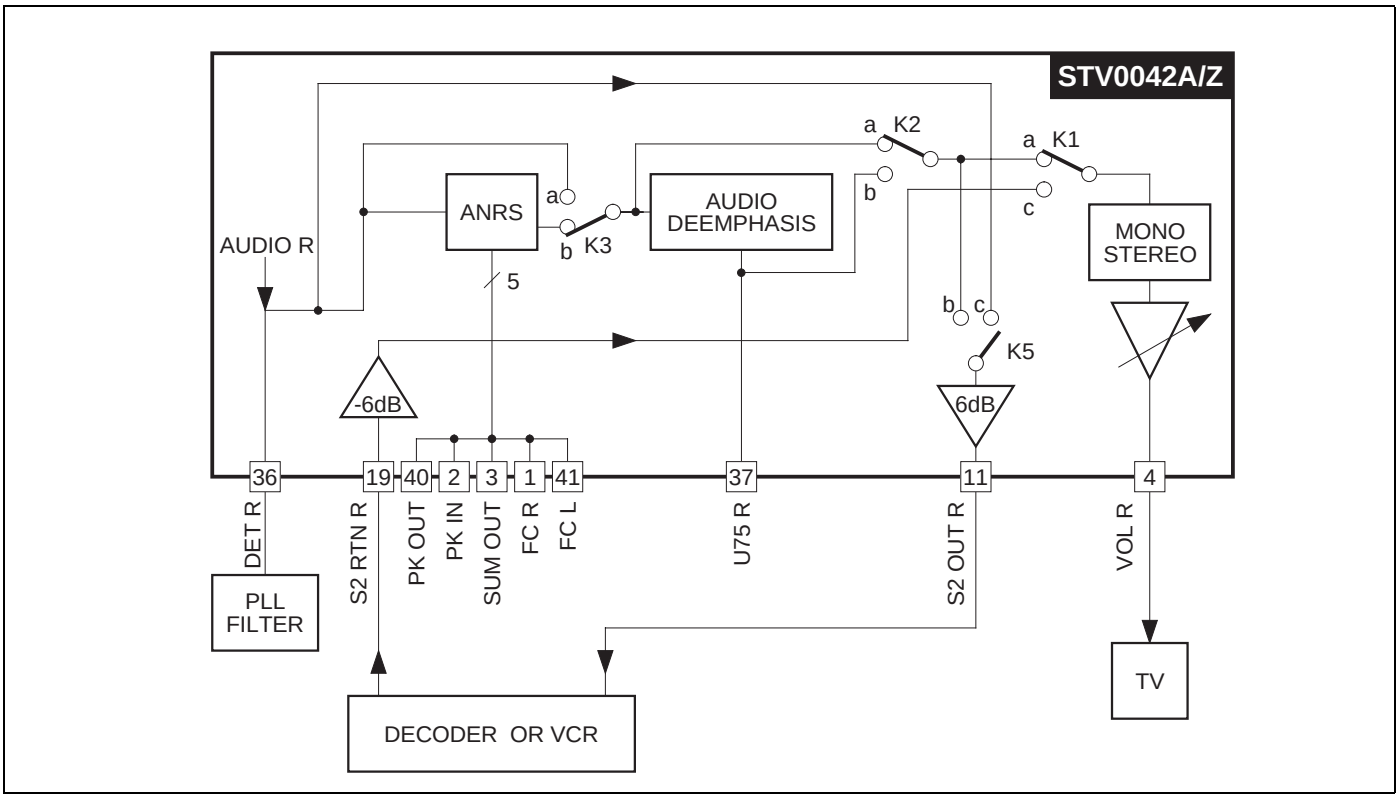


Figure 6: Audio Signal Processing Diagram (Right)



1.1.3 Video Processing

A block diagram of the Video Processing block is shown in Figure 7.

1.1.3.1 Base Band Input

Pin BBANDIN (pin 17) is an AC-coupled video input from a tuner with an impedance greater than 10 kΩ ±25%. This pin drives an on-chip video amplifier. The other input of this amplifier is AC grounded via an internal connection to pin VREF. The video amplifier has selectable gain from 0 dB to 12.7 dB in 63 steps and its output signal can be selected as normal or inverted.

1.1.3.2 Unclamped De-emphasized Video Output

Pin UNCLDEEM (pin 12) is an unclamped de-emphasized video output. It is also an input of the video matrix.

1.1.3.3 Sync Tip Clamp Input

Pin CLAMPIN (pin 10) clamps the extreme negative values (the sync tips) of the input signal to 2.7 V_{DC} (or the appropriate voltage). The video at the clamp input is only $1V_{PP}$. This clamped video which is de-emphasized, filtered and clamped (energy dispersal removed), is a normal video signal with negative synchronization. This signal drives the Video Matrix input called Normal Video. It has a weak (1.0 µA ±15%) stable current source pulling the input towards the ground. Otherwise, the input impedance is very high at DC to 1 kHz Z_{IN}> 2 MΩ. Video bandwidth through this pin is -1 dB at 5.5 MHz. The clamp input DC restore voltage is then used to obtain the correct DC voltage on the SCART outputs.

1.1.3.4 Video De-emphasis 1

Pin VIDEEM1 (pin 15) is connected to an external de-emphasis network (for instance, 625 lines PAL de-emphasis).

1.1.3.5 Video De-emphasis 2 or 22 kHz Output

Pin VIDEEM2/22KHZ (pin 13) is connected to an external de-emphasis network (for instance, 525 lines NTSC or other video de-emphasis). Alternatively, a precise 22 kHz tone may be output by I²C bus control.

1.1.3.6 VCR SCART Video Return

Pin S2VIDRTN (pin 8) is an external video input 1.0 V_{PP} AC-coupled 75 Ω source impedance. This input has a DC restoration clamp on its input. The clamp sink current is 1 µA ±15% with the input buffer impedance greater than 1 MΩ. This is the input signal to the Video Matrix.

1.1.3.7 SCART Video Outputs

Pins S1VIDOUT and S2VIDOUT (pins 5 and 6, respectively) are video drivers for SCART 1 and SCART 2. An external emitter follower buffer is required to drive a 150-Ω load. The average DC voltage must be 1.5 V on the outputs. The video signal is 2.0 V_{PP} with a 5.5 MHz bandwidth with 1.2 V sync tips. These pins receive the signals sent from the Video Matrix. The signal that will be output from the Video Matrix is controlled by a control register. These outputs also feature High Impedance mode for parallel connections.

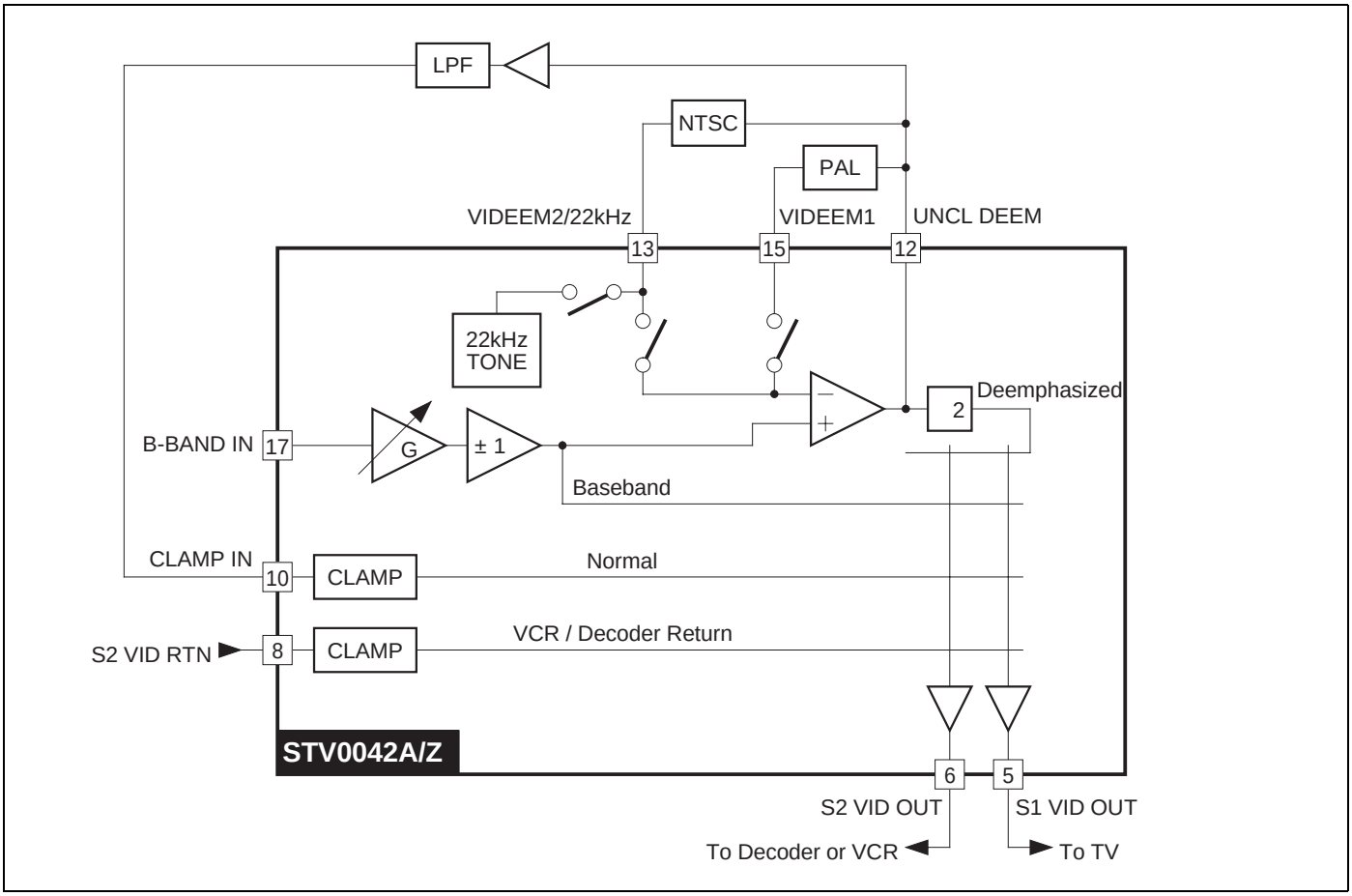
1.1.3.8 12V Video Power Supply

Pin V12V (pin 14) is a double-bonded 12-V video power supply with ESD and guard rings.

1.1.3.9 V GND

Pin VGND (pin 16) a strategically placed double-bonded video power ground connection used to reduce video currents getting into the rest of the circuit.

Figure 7: Video Processing Block Diagram



1.1.4 Control Block

1.1.4.1 5-V Ground

Pin GND5V (pin 26) is the main power ground connection for the control logic registers, the I²C bus interface, synthesizer, watchdog and the crystal oscillator.

1.1.4.2 5-V Digital Power Supply

Pin VDD5V (pin 25) is a digital 5-V power supply.

1.1.4.3 SCL

This pin (pin 22) is the I²C bus clock line. It requires an external pull-up (for example, 10 kΩ at 5V). Clock = DC to 100 kHz.

1.1.4.4 SDA

This pin (pin 23) is the I²C bus data line. It requires an external pull-up (for example, 10 kΩ at 5V).

1.1.4.5 4/8 MHz Quartz Crystal or Clock Input

Pin XTL (pin 24) allows the on-chip oscillator to be either used with a 4 MHz or 8 MHz crystal oscillator connected to ground or to be driven by an external clock source. The external source can be either 4 MHz or 8 MHz. A programmable bit in the control block removes a ÷2 block when the 4 MHz option is selected.

2 Circuit Description

2.0.1 Video Section

The composite video is first set to a standard level by means of a 64-step gain-controlled amplifier. If the modulation is negative, an inverter can be switched in.

One of two different external video de-emphasis networks (for instance PAL and NTSC) is selectable by an integrated bus controlled switch. Then energy dispersal is removed by a sync tip clamping circuit, which is used on all inputs to a video switching matrix, thus making sure that no DC steps occur when switching video sources.

The matrix can be used to feed video to and from decoders, VCRs and TVs.

Additionally, all the video outputs are tri-state type (high impedance mode is supported), allowing a simple parallel connections to the SCARTs (Twin tuner applications).

2.0.2 Audio Section

The two audio channels are totally independent except for the possibility given to output on both channels only one of the selected input audio channels.

To allow a very cost-effective application, each channel uses PLL demodulation. Neither external complex filter nor ceramic filters are needed.

The frequency of the demodulated subcarrier is chosen by a frequency synthesizer which sets the frequency of the internal local oscillator by comparing its phase with the internally generated reference. When the frequency is reached, the microprocessor switches in the PLL and the demodulation starts. At any moment the microprocessor can read from the device (watchdog registers) the actual frequency to which the PLL is locked. It can also verify that a carrier is present at the wanted frequency (by reading AMPLK status bit) thanks to a synchronous amplitude detector, which is also used for the audio input AGC.

In order to maintain constant amplitude of the recovered audio regardless of variations between satellites or subcarriers, the PLL loop gain may be programmed from 56 values.

Any frequency deviation can be accommodated between ±30 and ±400 kHz.

In the typical application, the STV0042A/Z offers two audio de-emphasis 75 µs and 50 µs. When required a J17 de-emphasis can be implemented by using specific application diagram (see Application Note: AN838, Chapter 4.2).

A dynamic noise reduction system (ANRS) is integrated into the STV0042A/Z using a low-pass filter, the cut-off frequency of which is controlled by the amplitude of the audio after insertion of a bandpass filter.

Two types of audio outputs are provided: one is a fixed $1V_{RMS}$ and the other is a gain-controlled $2V_{RMS}$max. The control range is between +12 and -26.75 dB in steps of 1.25 dB. This output can also be muted.

A matrix is implemented to feed audio to and from decoders, VCRs and TVs.

Noise reduction system and de-emphasis can be inserted or by-passed through bus control.

Also all the audio outputs are tri-state-type (high impedance mode is supported), allowing a simple parallel connections to the SCARTs (Twin tuner applications).

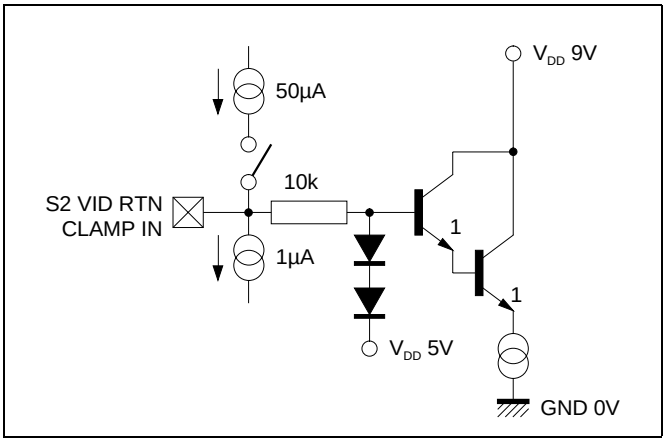
2.0.3 Other Features

A 22kHz tone is generated for LNB control. It is selectable by bus control and available on one of the two pins connected to the external video de-emphasis networks.

By means of the I^2C bus there is the possibility to drive the ICs into a low power consumption mode with active audio and video matrixes. Independently from the main power mode, each individual audio and video output can be driven to high impedance mode.

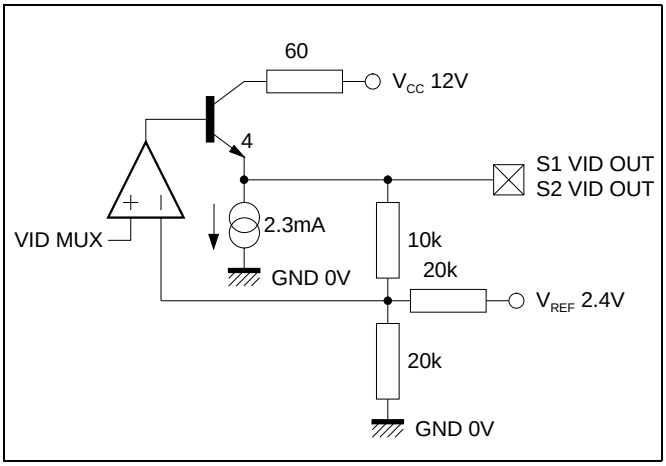
3 Input/Output Diagrams

Figure 8: S2VIDRTN and CLAMPIN Pins[1]



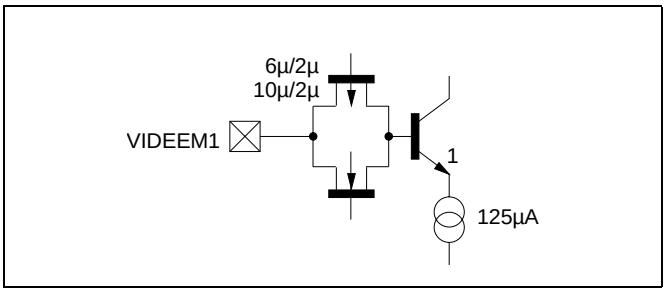
1. The 50 µA source is active only when VIDIN < 2.7 V.

Figure 9: S1VIDOUT and S2VIDOUT Pins[1]



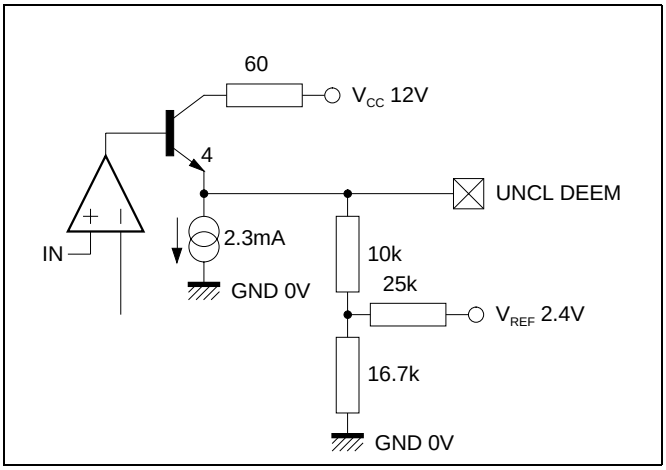
1. Same as Figure 8, but with no Black Level Adjustment.

Figure 10: VIDEEM1 Pin[1]



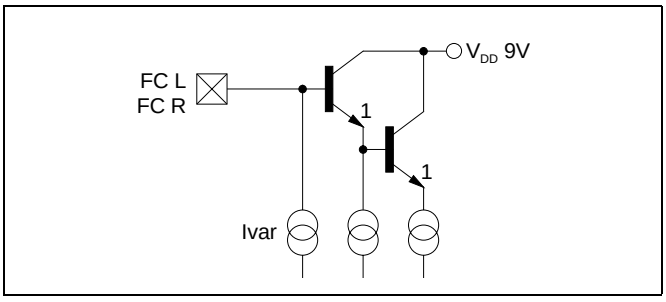
1. R_{ON} of the transistor gate is ≈10 kΩ.

Figure 11: UNCLDEEM Pin[1]



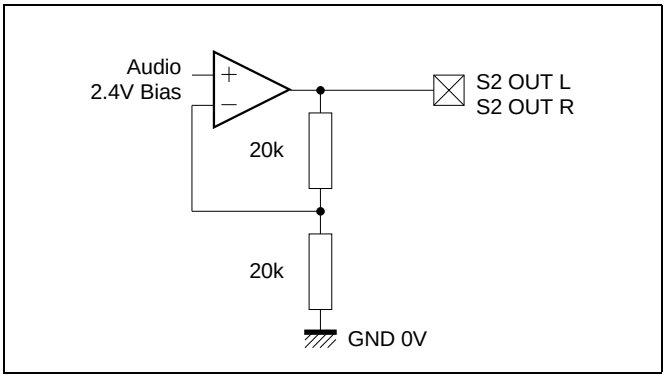
1. Same as Figure 9, but with a slightly different gain.

Figure 12: FCL and FCR Pins[1]



1. I_{VAR} is controlled by the maximum peak detection audio level ±15 µA (1 V_{PP} audio).

Figure 13: S2OUTL and S2OUTR Pins[1]



1. Same as Figure 17, but with gain fixed at +6 dB.

Figure 14: VIDIN Pin

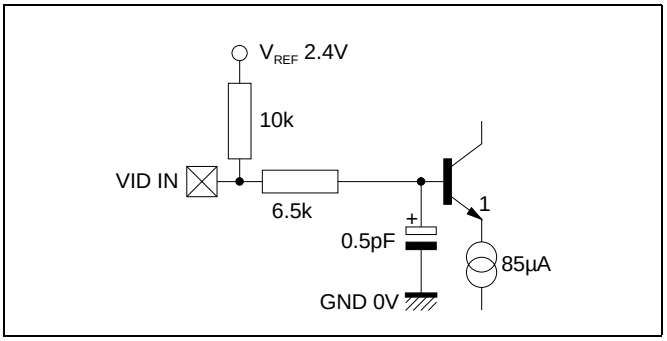


Figure 15: PKOUT Pin

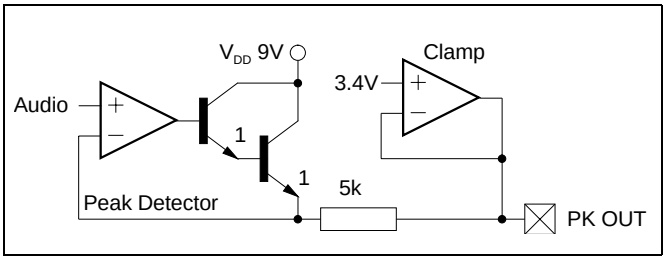
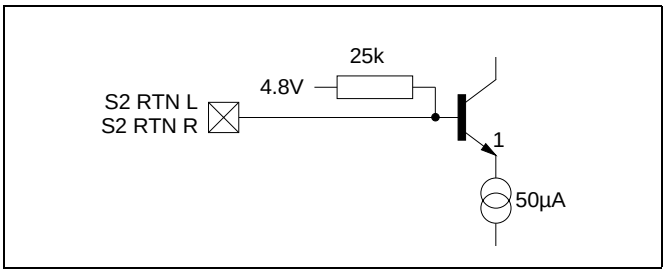
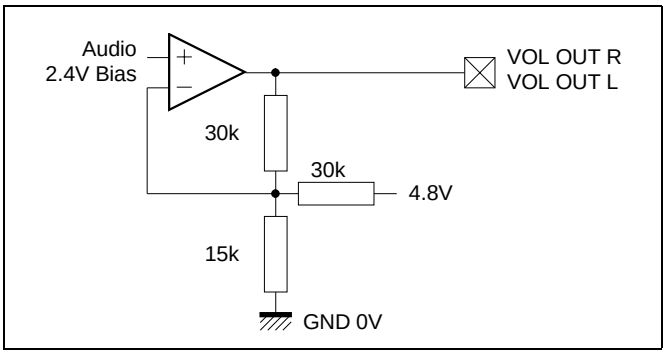


Figure 16: S2RTNL and S2RTNR Pins[1]



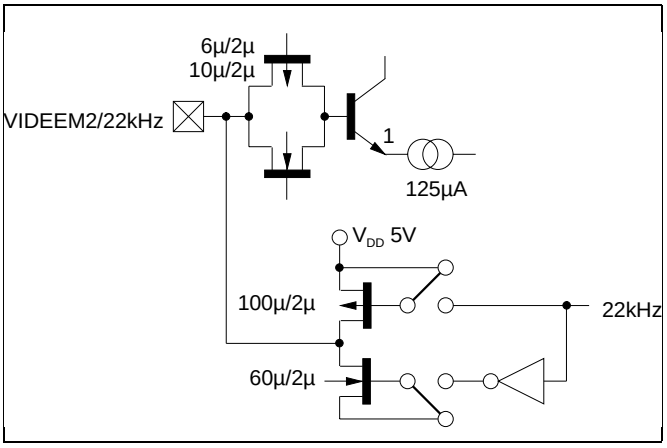
1. 4.8V bias voltage is the same as the bias level on the audio outputs.

Figure 17: VOLOUTR and VOLOUTL Pins[1]



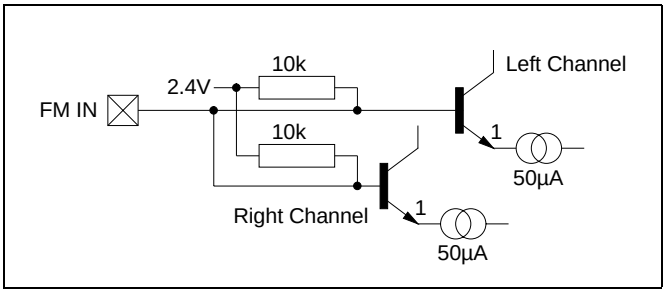
1. Audio output with volume and SCART driver with +12 dB gain for up to 2 V_{RMS}. The Op Amp has a push-pull output stage.

Figure 18: VIDEEM2 / 22kHz Pin[1]



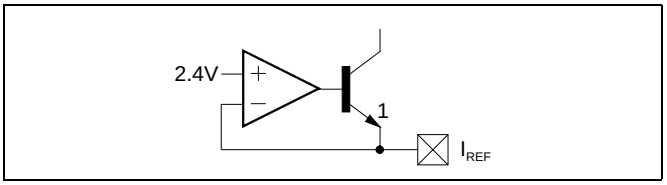
1. R_{ON} of the transistor gate is ≈10 kΩ.

Figure 19: FMIN Pin[1]



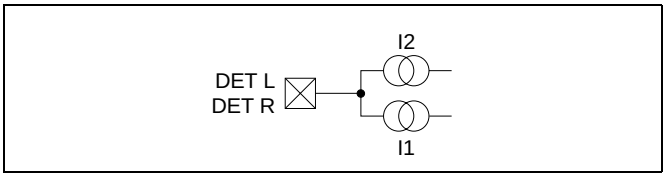
1. The other input for each channel is internally biased in the same way via 10 kΩ to the 2.4 V VREF.

Figure 20: IREF Pin[1]



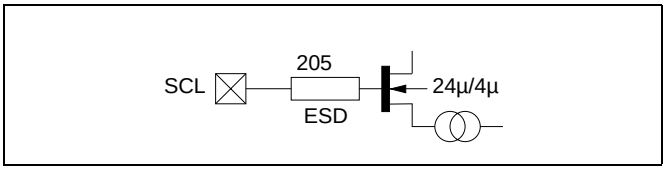
1. The optimum value if IREF is 50 µA ±2% so an ext. resistor of 47.5 kΩ ±1% is required.

Figure 21: DETL and DETR Pins[1]



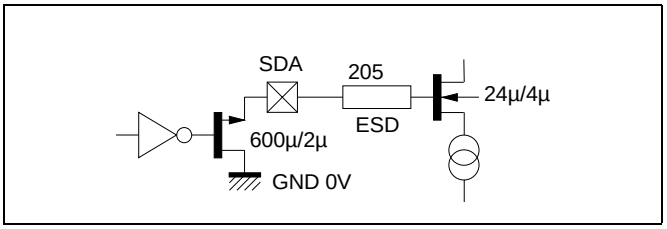
1. I_2 - I_1 = f (phase error).

Figure 22: SCL Pin[1]



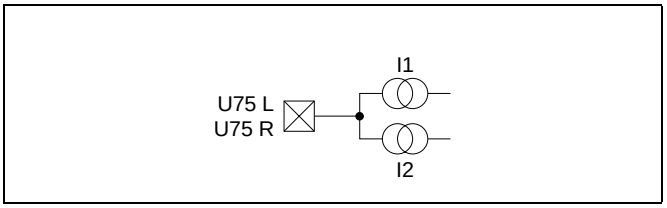
1. This is the input to a Schmitt input buffer made with a CMOS amplifier.

Figure 23: SDA Pin[1]



1. Input same as above. Output pull down only, relies on external resistor for pull-up.

Figure 24: U75L and U75R Pins[1]



1. I_1 - I_2 = 2 x Audio / 18 kΩ. e.g. 1 V_{PP} Audio: ±55 µA. There are internal switches to match the audio level of the different standards.

Figure 25: XTL Pin

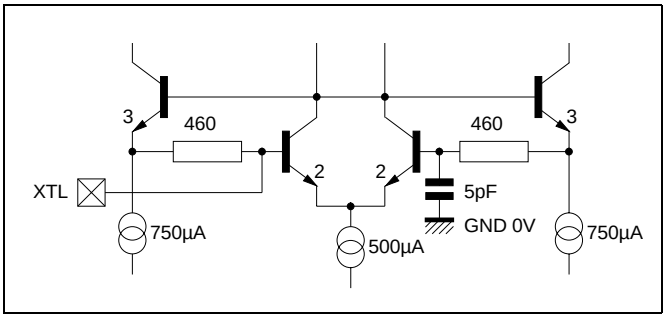
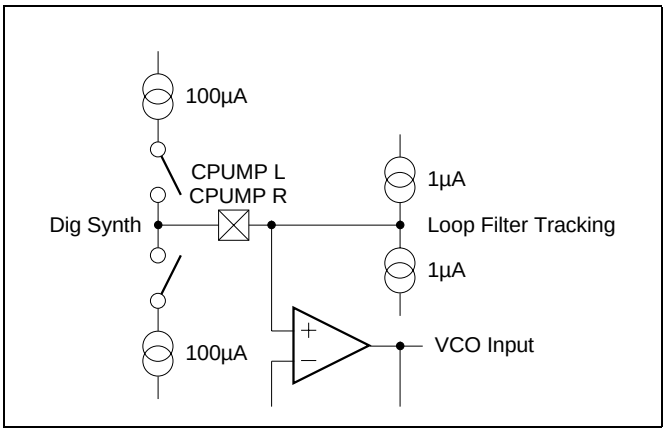
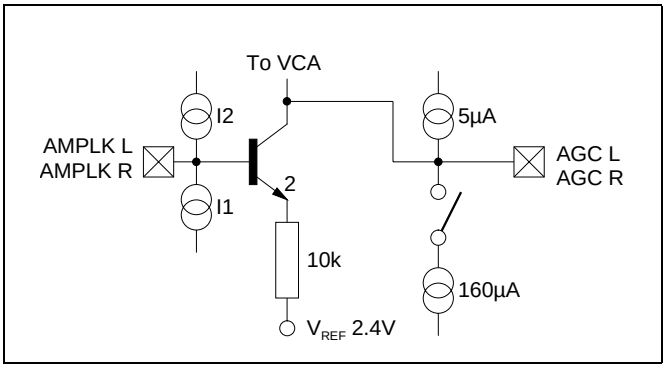


Figure 26: CPUMPL and CPUMPR Pins[1]



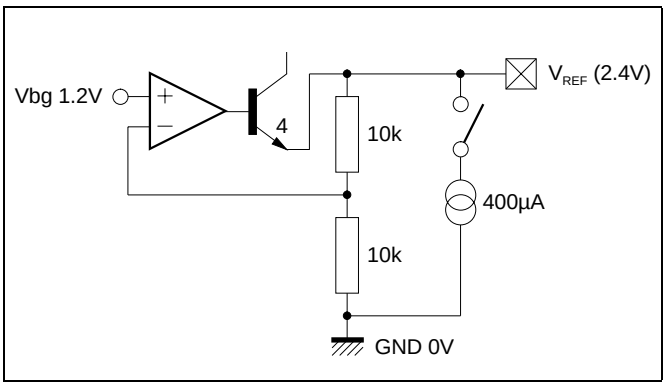
1. An offset on the PLL loop filter will cause an offset in the two 1 µA currents that will prevent the PLL from drifting-off frequency.

Figure 27: AMPLKL, AMPLKR, AGCL and AGCR Pins[1]



1. I_2 and I_1 from the amplitude detecting mixer.

Figure 28: VREF Pin[1]



1. The 400 µA source is off during stand-by mode.

Figure 29: SUMOUT Pin

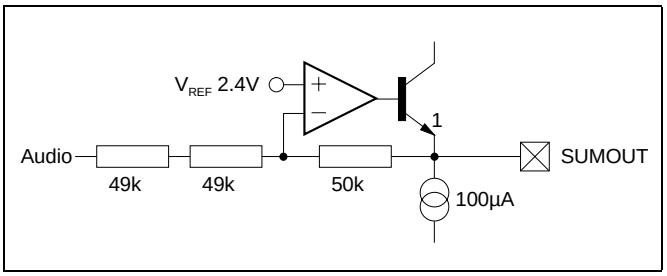


Figure 30: PKIN Pin

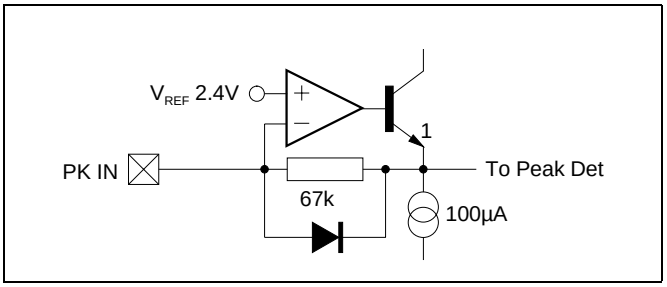
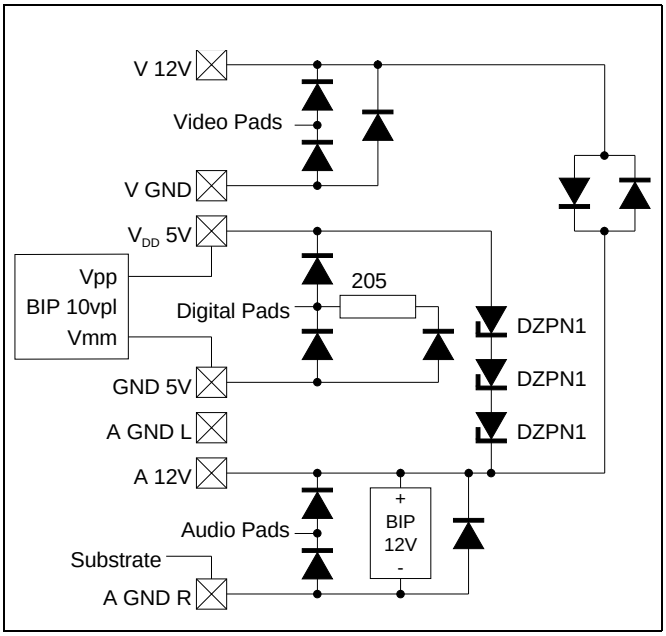


Figure 31: V12V, VGND, VDD5V, GND5V, AGNDL, A12V and AGNDR Pins[1]



1. Refer to Table 2.

Table 2: Double-buffered Supply Pins

Pin	Comment	Pad 1	Pad 2
V12V	Double-bonded	Connected to all of the 12V ESD and video guard rings	Connected to power up the video block
VGND	Double-bonded	Connected to power-up all of the video multiplexer and I/O.	Used only as a low noise GND for the video input.
VDD5V & GND5V	Connected to the crystal oscillator and the bulk of the CMOS logic and 5V ESD.		
AGNDL	Double-bonded	Connected to the left VCO, dividers, mixers and guard ring. the guard connection is star connected directly to the pad.	Connected to both AGC amps and the de-emphasis amplifiers, frequency synthesis and FM deviation selection circuit for both channels.
A12V	Double-bonded	Connected to the ESD and guard ring.	Connected to the main power for all of the audio parts.
AGNDR	Double-bonded[1]	Connected to the right VCO, dividers, mixers and guard ring. The guard connection is star connected directly to the pad.	Connected to the bias block, audio noise reduction, volume, multiplexer and ESD.

1. A third bond wire on this pin is connected directly to the die pad (substrate).

4 I²C Protocol

4.1 Writing to the Chip

S-Start Condition

P-Stop Condition

CHIP ADDR - 7 bits. 06H

W	Write/Read bit is the 8th bit of the chip address.
A	ACKNOWLEDGE after receiving 8 bits of data/address.
REG ADDR	Address of register to be written to, 8 bits of which bits 3, 4, 5, 6 & 7 are 'X' or don't care i.e. only the first 3 bits are used.
DATA	8 bits of data being written to the register. All 8 bits must be written to at the same time.
REG ADDR/A/DATA/A	Can be repeated, the write process can continue until terminated with a STOP condition. If the **REG ADDR** is higher than 07 then IIC PROTOCOL will still be met (i.e. an **A** generated).

Table 3: Example

S	06	W	A	00	A	55	A	01	A	8F	...	A	P

4.2 Reading from the Chip

When reading, there is an auto-increment feature. This means any read command always starts by reading Reg 8 and will continue to read the following registers in order after each acknowledge or until there is no acknowledge or a stop. This function is cyclic that is it will read the same set of registers without re-addressing the chip. There are two modes of operation as set by writing to bit 7 of register 0. Read 3 registers in a cyclic fashion or all 5 registers in a cyclic fashion. Note only the last 5 of the 11 registers can be read.

Reg0 bit 7 = L → Start / chip add / R / A / Reg 8 / A / Reg 9 / A / Reg 0A / A / Reg 8 / A / Reg 9 / A / Reg 0A /... / P /

Reg0 bit 7 = H → Start / chip add / R / A / Reg 8 / A / Reg 9 / A / Reg 0A / A / Reg 7 / A / Reg 6 / A / Reg 8 / A / Reg 9 / A / Reg 0A / A / Reg 7 / A / Reg 6 / ... / P /

5 Control Registers

Register 0 Write Only

Bit Name	Reset	Function
Bit 7	0h	Read Register 0: Read 3 registers 1: Read 5 registers
Bit 6	0h	Audio Multiplexer - ANRS Noise Reduction Select (Switch K3) (Refer to Figure 5 and Figure 6) 0: ANRS not active 1: ANRS active
Bit 5	0h	Not to be used
Bits[4:0]	0h	Audio Volume Control Select 00h: Mute 01h: -26.75 dB 1.25 dB steps up to 1Fh: +12 dB

Register 1 WrIte Only

Bit Name	Reset	Function
Bit 7	0h	Video De-emphasis 1 / Video De-emphasis 2 0: Video De-emphasis 1 1: Video De-emphasis 2
Bit 6	0h	Selected Video Invert 0: Non-inverted 1: Inverted
Bits[5:0]	0h	Select Video Gain 00h = 0 dB 01h = +0.202 dB 02h = +0.404 dB 0.202 dB steps up to 3Fh = +12.73 dB

Register 2 Write Only

Bit Name	Reset	Function
Bits[7:6]	3h	Select Left/Right/Stereo for Volume Output 00: Mono Left / Channel 1 10: Mono Right / Channel 2 11: Stereo Left and Right (Default)
Bits[5:4]	3h	Select Audio Source for Volume Output (Switch K1) (Refer to Figure 5 and Figure 6) 00: Audio De-emphasis (Switch K2 output) (position of Switch K1: a) 10: SCART 2 return (position of Switch K1: c) 01: Not to be used (position of Switch K1: b) 11: High Impedance or Low Power mode (Default)

Bit Name	Reset	Function
Bit 3	0h	Select Clock Speed 0: 8 MHz 1: 4 MHz
Bits[2:0]	7h	Select Video Source for SCART 1 Output 000: Baseband video 001: De-emphasized video 010: Normal video 011: Not to be used 100: SCART 1 return 101: Not to be used 110: Nothing selected 111: High Impedance or Low Power mode (Default)

Register 3 Write Only

Bit Name	Reset	Function
Bits[7:6]	3h	Audio De-emphasis Select (Switch K2) (Refer to Figure 5 and Figure 6) 00: No de-emphasis (position of Switch K2: a) 10: Not to be used (position of Switch K2: c) 01: 50 µs de-emphasis (position of Switch K2: b) 11: 75 µs de-emphasis (position of Switch K2: b) (Default)
Bits[5:4]	3h	Select Audio Source for SCART 2 Output (Switch K5) (Refer to Figure 5 and Figure 6) 00: PLL output (position of Switch K5: c) 10: Not to be used (position of Switch K5: a) 01: Audio De-emphasis (Switch K2 output) (position of Switch K5: b) 11: High Impedance or Low Power mode (Default)
Bit 3	0h	22 kHz Select 0: No Tone 1: 22 kHz Tone Out if bit 7 of Register 1 = 0
Bits[2:0]	7h	Select Video Source for SCART 2 Output 000: Baseband video 001: De-emphasized video 010: Normal video 011: Not to be used 100: SCART 2 Return 101: Not to be used 110: Nothing selected 111: High Impedance or Low Power mode (Default)

Register 4 Write Only

Bit Name	Reset	Function
Bits[7:4]	Dh	Not to be used.
Bit 3	1h	Standby or Low Power Mode Select 0: Standby mode 1: Low Power mode
Bits[2:0]	7h	Not to be used.

Register 5 Write Only

Bit Name	Reset	Function
Bits[7:6]	2h	Not to be used.
Bits[5:0]	35h	FM Deviation Selection Bit 5 = 0, double the FM Deviation 110101: Default value

Table 4: FM Deviation Selection Table

Selected Nominal Carrier Modulation		Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 5 = 1	Bit 5 = 0					
Do not use. Calibration Setting = 0.3373 V Offset on VCO	Do not use.	0	0	0	0	0
Do not use. Calibration Setting = 0.3053 V Offset on VCO	Do not use.	0	0	0	0	1
Do not use. Calibration Setting = 0.2763 V Offset on VCO	Do not use.	0	0	0	1	0
Calibration Setting = 1 V Offset on VCO	Calibration Setting (2 V)	0	0	0	1	1
296 kHz	592 kHz	0	0	1	0	0
267 kHz	534 kHz	0	0	1	0	1
242 kHz	484 kHz	0	0	1	1	0
218 kHz	436 kHz	0	0	1	1	1
198 kHz	396 kHz	0	1	0	0	0
179 kHz	358 kHz	0	1	0	0	1
161 kHz	322 kHz	0	1	0	1	0
146 kHz	292 kHz	0	1	0	1	1
133 kHz	266 kHz	0	1	1	0	0
120 kHz	240 kHz	0	1	1	0	1
109 kHz	218 kHz	0	1	1	1	0
98.3 kHz	196 kHz	0	1	1	1	1
89.7 kHz	179 kHz	1	0	0	0	0
80.9 kHz	161 kHz	1	0	0	0	1
73.1 kHz	146 kHz	1	0	0	1	0
66.0 kHz	122 kHz	1	0	0	1	1
60.0 kHz	120 kHz	1	0	1	0	0
54.4 kHz (Default)	109 kHz	**1**	**0**	**1**	**0**	**1**
49.1 kHz	98 kHz	1	0	1	1	0
44.3 kHz	89 kHz	1	0	1	1	1

Table 4: FM Deviation Selection Table

Selected Nominal Carrier Modulation		Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 5 = 1	Bit 5 = 0					
39.8 kHz	78 kHz	1	1	0	0	0
35.9 kHz	71 kHz	1	1	0	0	1
32.4 kHz	65 kHz	1	1	0	1	0
29.1 kHz	58 kHz	1	1	0	1	1
26.7 kHz	53 kHz	1	1	1	0	0
24.3 kHz	48.6 kHz	1	1	1	0	1
21.9 kHz	43.8 kHz	1	1	1	1	0
19.7 kHz	39.6 kHz	1	1	1	1	1

Register 6 Write/Read

Bit Name	Reset	Function
Bits[7:6]	2h	Select Frequency for PLL Synthesizer Bit 6: LSB (Bit 0) of 10-bit value Bit 7: Bit 1 of 10-bit value
Bits[5:4]	0h	Select RF Source x1: FM Detector 1 enabled 1x: FM Detector 2 enabled
Bits[3:2]	1h	Select Frequency Synthesizer x1: Frequency Synthesizer 1 enabled 1x: Frequency Synthesizer 2 enabled
Bit 1	1h	I/O Data Direction Select 0: Input 1: Output
Bit 0	0h	I/O Status

Register 7 Write/Read

Bit Name	Reset	Function
Bits[7:0]	AFh	Select Frequency for PLL Synthesizer Bit 0: Bit 2 of 10-bit value Bit 7: MSB (bit 10) of 10-bit value

Register 8 Read Only

Bit Name	Reset	Function
Bits[7:6]		Read Frequency of Watchdog 2 Bit 6: LSB (Bit 0) of 10-bit value Bit 7: Bit 1 of 10-bit value
Bit 5		Not to be used.
Bit 4		Subcarrier Detection (Detector 2) 0: No Subcarrier 1: Subcarrier Detected
Bits[3:2]		Read Frequency of Watchdog 1 Bit 2: LSB (Bit 0)of 10-bit value Bit 3: Bit 1 of 10-bit value
Bit 1		Not to be used.
Bit 0		Subcarrier Detection (Detector 1) 0: No Subcarrier 1: Subcarrier Detected

Register 9 Read Only

Bit Name	Reset	Function
Bits[7:0]		Read Frequency of Watchdog 1 Bit 0: Bit 2 of 10-bit value Bit 7: MSB (bit 10) of 10-bit value

Register 0A Read Only

Bit Name	Reset	Function
Bits[7:0]		Read Frequency of Watchdog 2 Bit 0: Bit 2 of 10-bit value Bit 7: MSB (bit 10) of 10-bit value

6 FM Demodulation Software Routine

With the STV0042A/Z circuit, for each channel, three steps are required to achieve a FM demodulation:

1 To set the demodulation parameters:
   - ➢ FM deviation selection,
   - ➢ Subcarrier frequency selection.

2 To implement a waiting loop to check the actual VCO frequency.

3 To close the demodulation phase locked loop (PLL).

Referring to Figure 3: FM Demodulation on page 6, the frequency synthesis block is common to both channels (left and right); consequently two complete sequences have to be done one after the other when demodulating stereo pairs.

6.1 Detailed Description

Conventions:

- R = Stands for Register
- B = Stands for Bit

Example: R5B2 = Register 5, Bit 2

For clarity, the explanations are based on the following example: stereo pair 7.02 MHz/L and 7.20 MHz/R and ±50 kHz maximum deviation

6.1.1 1st Step (Left): Setting the Demodulation Parameters

1 The FM deviation is selected by loading Register 5 with the appropriate value.

Corresponding bandwidth can be calculated as follows:
BW ≈ 2 (FM deviation and audio bandwidth)
BW ≈ 2 (value given in table and audio bandwidth)

In the example:

R5	Bits	7	6	5	4	3	2	1	0
		X	X	1	1	0	1	1	0

Note: Very wide deviations (up to ±592 kHz) can be accommodated when R5B5 is low.

2 The subcarrier frequency is selected by launching a frequency synthesis (the VCO is driven to the desired frequency). This operation requires two actions:

2.1 Connect the VCO to the frequency synthesis loop. See Figure 3 on page 6.

- ➢ Switch K4 closed → R6 B2 = 1
- ➢ Switch K3 to bias → R6 B4 = 0
- ➢ Switch K2 to bias → R6 B3 = 0
- ➢ Switch K1 open → R6 B5 = 0

2.2 Load R7 B[7:0] and R6 B[7:6] with the values corresponding to the left channel frequency. This 10 bits value is calculated as follows:

Subcarrier frequency = coded value x 10 kHz

(10 kHz is the minimum step of the frequency synthesis function). Since the tuning range is between 5 and 10 MHz, the coded value is a number between 500 and 1000 (210 = 1024). This value is coded on 10 bits.

Example:
7.02 MHz = 702 x 10 kHz
702 → 1010 1111 10 → AF + 10
R7 is loaded with AF and R6 B6: 0, R6 B7: 1.

Table 5 gives the settings for the most common subcarrier frequencies.

6.1.2 2nd Step (Left): VCO Frequency Checking (VCO)

This second step is actually a waiting loop in which the actual running frequency of the VCO is measured.

This loop can be exited when:

Subcarrier Frequency - 10 kHz ≤ Measured Frequency ≤ Subcarrier Frequency +10 kHz

Where, ±10 kHz is the maximum dispersion of the frequency synthesis function).

In practice, R8 B[3:2] and R9 B[7:0] are read and compared to the value loaded in R6 B[7:6] and R7 B[7:0] ±1 bit.

The duration of this step depends on the difference between the start frequency and the targeted frequency. Typically:

- The rate of change of the VCO frequency is about 3.75 MHz/s (pin CPUMP = 10 µF)
- In addition to this settling time, 100 ms must be added to take into account the sampling period of the watchdog.

6.1.3 3rd Step (Left)

The FM demodulation can be started by connecting the VCO to the phase locked loop (PLL).

In practice:

- Switch K3 closed → R6 B4 = 1
- Switch K4 open → R6 B2 = 0

After this sequence of 3 steps for left channel, a similar sequence is required for the right channel.

Note: 1 The FM deviation does not have to be selected again for the right channel (once is enough for the pair).

2 Before sending the demodulated signal to the audio output, it is recommended to keep the muting and to check whether a subcarrier is present at the desired frequency. Such information can be read in R8 B0 and R8 B4.

Two different strategies can be adopted when enabling the output:

- Either both left and right demodulated signals are simultaneously authorized when both channels are ready.
- Or while the right channel sequence is running, the already ready left signal is sent to the left and right outputs and the real stereo sound L/R is output when both channels are ready. This second option outputs the sound a few hundred milliseconds before the first one.

Table 5: Frequency Synthesis Register Setting for the Most Common Subcarrier Frequencies

Subcarrier Frequency (MHz)	Register 7 (hex)	Register 6	
		Bit 7	Bit 6
5.58	8B	1	0
5.76	90	0	0
5.8	91	0	0
5.94	94	1	0
6.2	9B	0	0
6.3	9D	1	0
6.4	A0	0	0
6.48	A2	0	0
6.5	A2	1	0
6.6	A5	0	0
6.65	A6	0	1
6.8	AA	0	0
6.85	AB	0	1
7.02	AF	1	0
7.20	B4	0	0
7.25	B5	0	1
7.38	B8	1	0
7.56	BD	0	0
7.74	C1	1	0
7.85	C4	0	1
7.92	C6	0	0
8.2	CD	0	0
8.65	D8	0	1

7 Application Diagrams

Figure 32: Typical STV0042A/Z Application Diagram with 2 Video De-emphasis Networks

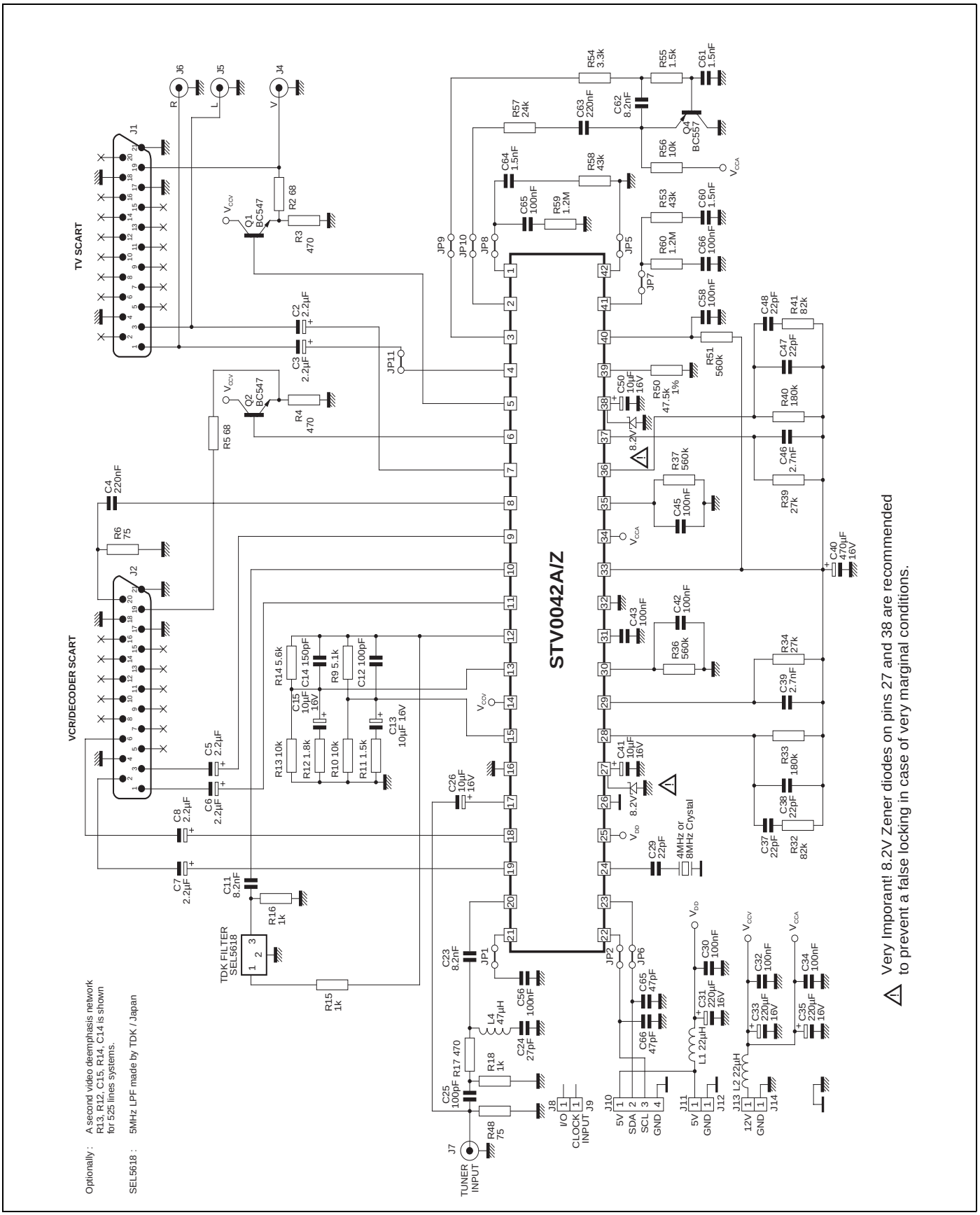
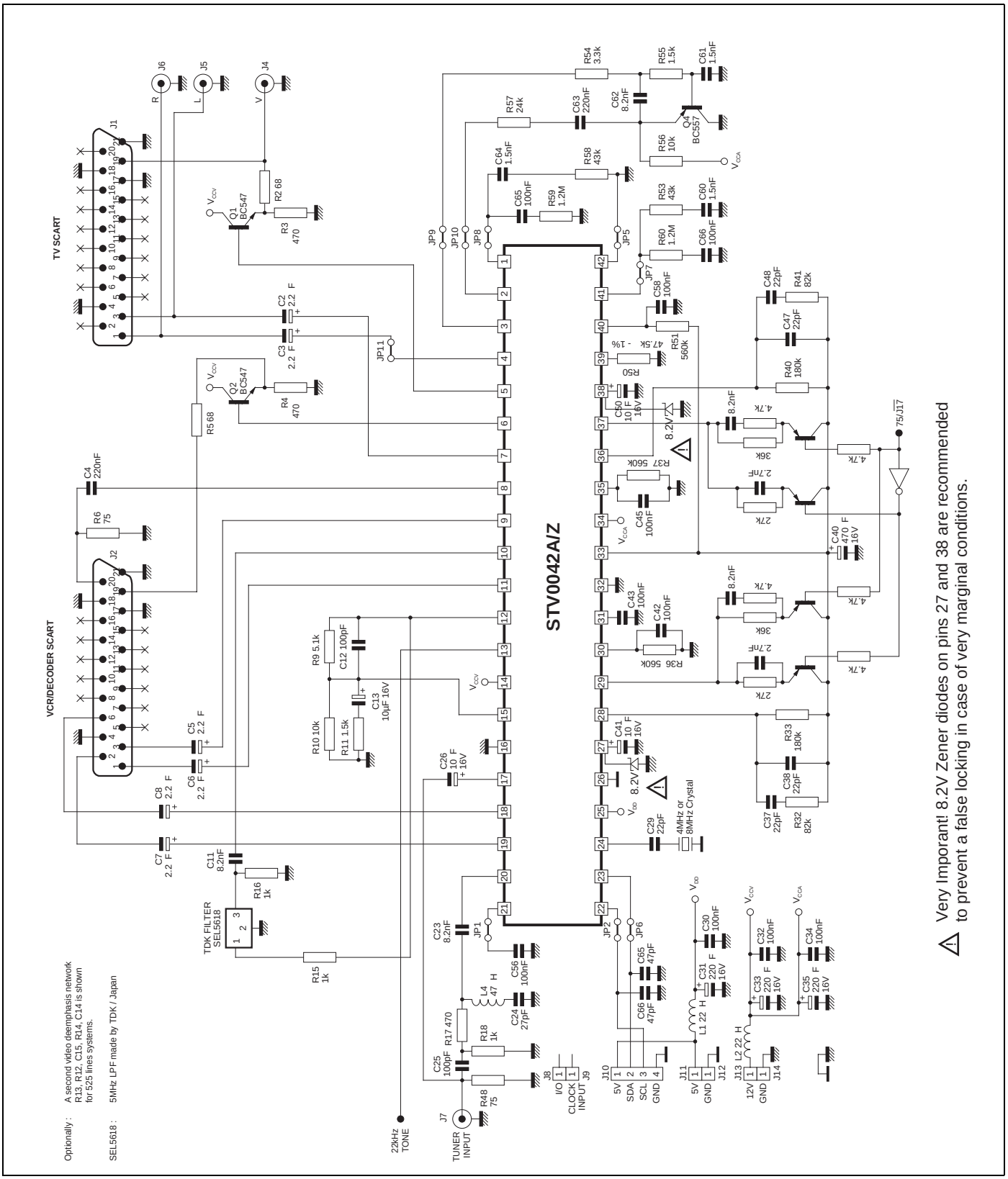


Figure 33: Typical STV0042A/Z Application Diagram with 22 kHz and 3 Audio De-emphasis Networks



8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC} V_{DD}	Supply Voltage	15.0 7.0	V
P_{TOT}	Total Power Dissipation	900	mW

8.2 Thermal Data

Symbol	Parameter	Value	Unit
R_{thJA}	Junction-to-Ambient Thermal Resistance	60	°C/W
T_{OPER}	Operating Ambient Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–55 to +150	°C

8.3 Electrical Characteristics

Test conditions: T_{AMB} = 25°C, V_{CC} = 12 V and V_{DD} = 5 V; unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} V_{DD}	Supply Voltage		11.4 4.75	12.0 5.0	12.6 5.25	V
IQ_{CC} IQ_{DD}	Supply Current	All audio and video outputs active.		55 8	70 15	mA
$IQLP_{CC}$ $IQLP_{DD}$	Supply Current at Low Power mode	All audio and video outputs in High Impedance mode.		27 6	35 9	mA

8.3.1 Clamp Stages (Pins CLAMPIN and S2VIDRTN)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ISKC	Clamp Input Sink Current	V_{IN} = 3 V	0.5	1.0	1.5	µA
ISCC	Clamp Input Source Current	V_{IN} = 2 V	40	50	60	µA

8.3.2 Audio Demodulator

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FMIN	FM Subcarrier Input Level (FMIN pin for AGC action)	VCO locked on carrier at 6 MHz 560 kΩ load on AMPLK pins 180 kΩ load on DET pins	5		500	mV_{PP}
DETH	Detector 1 and 2 (AMPLK pins) (Threshold for activating Level Detector 2)	8 mV_{PP} ≤ FMIN ≤ 500 mV_{PP} Carrier without modulation	2.90	3.10	3.30	V
VCO_{MIN}	VCO Minimum Frequency	V_{CC} = 11.4 to 12.6 V T_{AMB} = 0 to +70 °C			5	MHz
VCO_{MAX}	VCO Maximum Frequency	V_{CC} = 11.4 to 12.6 V T_{AMB} = 0 to +70 °C	10			MHz
AP50	1 kHz Audio Level at PLL Output (DET pins)	50 kHz dev. FM input at 0.5 V_{PP} Coarse deviation set to 50 kHz. (Reg. 05 = 36h)	0.6	1.0	1.35	V_{PP}
APA50	1 kHz Audio Level at PLL Output (DET pins)	50 kHz dev. FM input at 0.5 V_{PP} Coarse and fine settings used.	0.92	1.0	1.08	V_{PP}
FMBW	FM Demodulator Bandwidth	Gain at 12 kHz versus 1 kHz 180 kΩ, 82 kΩ and 22 pF on DET pins.	0.0	0.3	1.0	dB
DPCO	Digital Phase Comparator Output Current (CPUMP pins)	Average sink and source current to external capacitor.		60		µA

8.3.3 Automatic Noise Reduction System

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LRS	Output Level (SUMOUT pin)	1 V_{PP} on left and right channels.	0.9	1.0	1.1	V_{PP}
LDOR	Level Detector Output Resistance (PKOUT pins)		4.0	5.4	6.8	kΩ
NDFT	Level Detector Fall Time Constant (PKOUT pins)	External 22 nF to GND and 1.2 MΩ to VREF.		26.4		ms
NDLL	Bias Level (PKOUT pins)	No audio inputs.		2.4		V
LLCF	Noise Reduction Cut-off Frequency at Low Level Audio	100 mV_{PP} on DET pins, external 330 pF capacitor on FC pins.		0.85		kHz
HLCF	Noise Reduction Cut-off Frequency at High Level Audio	1 V_{PP} on DET pins, external 330 pF capacitor on FC pins.		7.00		kHz

8.3.4 Audio Outputs (Pins VOLOUTR and VOLOUTL)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DCOL	DC Output Level			4.8		V
AOLN	Audio Output Level (Reg 00 = 1Ah)	FM input same as APA50, No de-emphasis, no pre-emphasis and no noise reduction.	1.50	1.90	2.34	V_{PP}
AOL50	Audio Output Level (Reg 00 = 1Ah)	FM input same as APA50, 50 µs de-emphasis, 27 kΩ and 2.7 nF load, no pre-emphasis and no noise reduction.	2.0	3.3	4.0	V_{PP}
AOL75	Audio Output Level (Reg 00 = 1Ah)	FM input same as APA50, 75 µs de-emphasis, 27 kΩ and 2.7 nF load, no pre-emphasis and no noise reduction.	2.0	3.3	4.0	V_{PP}
AMA1	Audio Output Attenuation with Mute ON (Reg 00 = 00h)	1 kHz at 1 V_{PP} from S2RTN pins.	60	65		dB
MXAT	Maximum Attenuation before Mute (Reg 00 = 01h)	1 kHz from S2RTN pins.		32.75		dB
MXAG	Audio Gain (Reg 00 = 1Fh)	1 kHz from S2RTN pins.	5	6	7	dB
ASTP	Attenuation of each of the 31 Steps	1 kHz		1.25		dB
THDA1	THD with Reg00 = 1Ah	1 kHz at 1 V_{PP} from S2RTN pins.		0.15		%
THDA2	THD with Reg00 = 1Ah	1 kHz at 2 V_{PP} from S2RTN pins.		0.3	1.0	%
THDAFM	THD with Reg00 = 1Ah	FM input same as APA50, 75 µs de-emphasis, ANRS ON.		0.3	1.0	%
ACS	Audio Channel Separation	1 kHz at 1 V_{PP} from S2RTN pins.	60	74		dB
ACSFM	Audio Channel Separation at 1 kHz	0.5 V_{PP} and 50 kHz deviation FM input on one channel, 0.5V_{PP} no deviation FM input on the other channel, Reg 05 = 36h, 75 ms de-emphasis, no ANRS		60		dB
SNFM	Signal-to-Noise Ratio	FM input same as APA50, 75 µs de-emphasis, ANRS OFF, Unweighted.		56		dB
SNFMNR	Signal-to-Noise Ratio	FM input same as APA50, 75 µs de-emphasis, ANRS ON, Unweighted.		69		dB
Z_{OUTL} Z_{OUTH}	Audio Output Impedance	Low Impedance mode High Impedance mode	 30	18 44	 55	Ω kΩ

8.3.5 Auxiliary Audio Outputs (Pins S2OUTR and S2OUTL)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DCOLAO	DC Output Level	Auxiliary input pins in open circuit		4.8		V
AOLNS	Audio Output Level on S2	FM input same as APA50, No de-emphasis, no pre-emphasis and no noise reduction.	1.55	2.00	2.42	V_{PP}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AOL50S	Audio Output Level on S2	FM input same as APA50, 50 µs de-emphasis, 27 kΩ and 2.7 nF load, no pre-emphasis and no noise reduction.	2.0	3.4	4.0	V_{PP}
AOL75S	Audio Output Level on S2	FM input same as APA50, 75 µs de-emphasis, 27 kΩ and 2.7 nF load, no pre-emphasis and no noise reduction.	2.0	3.4	4.0	V_{PP}
THDAOFM	THD on S2	FM input same as APA50, 75 µs de-emphasis, ANRS ON.		0.3	1.0	%
Z_{OUTL} Z_{OUTH}	Audio Output Impedance	Low Impedance mode High Impedance mode	 30	60 44	100 55	Ω kΩ

8.3.6 Reset Threshold

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RTCCU	End of Reset Threshold for V_{CC}	V_{DD} = 5 V, V_{CC} rising		8.7		V
RTCCD	Start of Reset Threshold for V_{CC}	V_{DD} = 5 V, V_{CC} falling		7.9		V
RTDDU	End of Reset Threshold for V_{DD}	V_{CC} = 12 V, V_{DD} rising		3.8		V
RTDDD	Start of Reset Threshold for V_{DD}	V_{CC} = 12 V, V_{DD} falling		3.5		V

8.3.7 Video Matrix (Pins S1VIDOUT and S2VIDOUT)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
XTK	Output Level on any output when 1 VPP CVBS input is selected for any other output	5 MHz		-60		dB
BFG	Output Buffer Gain	100 kHz	1.87	2.0	2.13	
DCOLVH	DC Output Level	High Impedance mode		0.0	0.2	V
Z_{OUTHV}	Video Output Impedance	High Impedance mode	16	23	30	kΩ
VCL	Sync Tip Level on selected outputs	1 V_{PP} CVBS via 10 nF on input	1.05	1.30	1.55	V

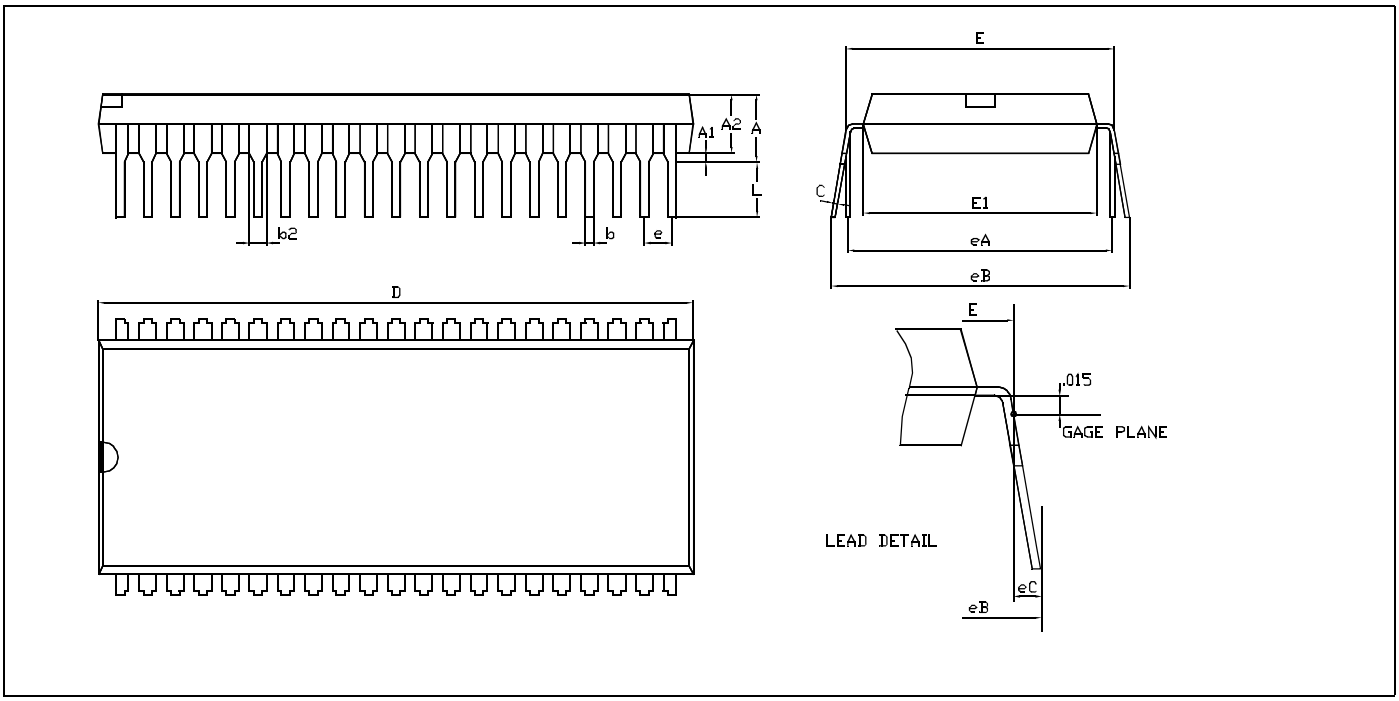
8.3.8 Composite Signal Processing

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIDC	VIDIN Voltage	External load current < 1 µA	2.25	2.45	2.65	V
ZVI	VIDIN Input Impedance		7	11	14	kΩ
DEODC	DC Output Level (VIDEEM pins)		2.25	2.45	2.65	V
DEOMX	Maximum AC Level before Clipping (VIDEEM pins)	GV = 0 dB, Reg 01 = 00h	2			V_{PP}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DGV	Gain Error versus GV at 100 kHz	GV = 0 to 12.7 dB, Reg 01 = 00h to 3Fh	-0.5	0	0.5	dB
INVG	Inverter Gain		-0.9	-1.0	-1.1	
VISOG	Video Input to SCART Output Gain	De-emphasis amplifier mounted in unity gain, normal video selected.	-1	0	1	dB
DEBW	Bandwidth for 1 V_{PP} input measured on VIDEEM pins	-3 dB with GV = 0 dB, Reg 01 = 00h	10			MHz
DFG	Differential Gain on Sync Pulses measured on VIDEEM pins	GV = 0 dB, 1 V_{PP} CVBS +0.5 V_{PP} 25 Hz sawtooth (VIDIN input)			1	%
ITMOD	Intermodulation of FM Subcarriers with Chroma Subcarrier	7.02 and 7.2 MHz subcarriers, 12.2 dB lower than Chroma		-60		dB

9 Package Mechanical Data

Figure 34: 42-Pin Shrink Plastic Dual In-Line Package, 600-mil Width



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
b		0.46	0.56		0.018	0.022
b2		1.02	1.14		0.040	0.045
C	0.23	0.25	0.38	0.009	0.010	0.015
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.600		0.630
E1	12.70	13.72	14.48	0.500	0.540	0.570
e		1.78			0.070	
eA		15.24			0.600	
eB			18.54			0.730
eC	0.00		1.52	0.000		0.060
L	2.54	3.30	3.56	0.100	0.130	0.140

10 Revision History

Revision	Main Changes	Date
0.1	First Issue.	June 2001
1.0	Revised Issue. Pin names ICATH and VOUT are confirmed. Document format updated.	January 2002
1.1	Addition of STV0042Z sales type and included information in Section 1.1.1.5: FM PLL Charge Pump Capacitors on page 6	July 2002
1.2	Modification of Figure 3: FM Demodulation, Figure 32: Typical STV0042A/Z Application Diagram with 2 Video De-emphasis Networks, Figure 33: Typical STV0042A/Z Application Diagram with 22 kHz and 3 Audio De-emphasis Networks, Section 1.1.1.5: FM PLL Charge Pump Capacitors and information in Section 5: Control Registers.	30 July 2002