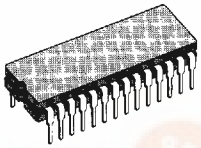
SGS-THOMSON MICROELECTRONICS

STU2071

4B3T U INTERFACE CIRCUIT

PRELIMINARY DATA

- 4B3T TWO-WIRE U INTERFACE CIRCUIT FOR LT AND NT APPLICATION
- 120 kbaud LINE SYMBOL RATE (120 SYMBOLS PER FRAME)
- SCRAMBLER AND DESCRAMBLER ACCORDING TO CCITT REC V.29
- BARKER CODE (11 SYMBOLS) SYNCHRONIZATION WORD
- UNSCRAMBLED 1 KBIT/S HOUSEKEEPING CHANNEL
- ADAPTIVE ECHO CANCELLATION WITH TRANSVERSAL FILTERING
- ADAPTIVE DECISION FEEDBACK EQUALIZATION
- AUTOMATIC GAIN CONTROL
- PDM AD CONVERTER
- AUTOMATIC ACTIVATION AND DEACTIVATION WITH POLARITY ADAPTION
- AUTOMATIC CODE VIOLATION DETECTION
- POWER FEED UNIT CONTROL
- ADVANCED CL3 1.5µm CMOS PROCESS
- 28 PIN DUAL-IN-LINE CERAMIC PACKAGE
- V* DIGITAL INTERFACE



Ceramic DIP28

ORDERING NUMBER:
STU2071F1

SYSTEM OVERVIEW

STU2071 (UIC) provides two transparent 64 kbit/s B channels, a transparent 16 kbit/s D channel, a transparent 1 kbit/s service channel and a 1 kbit/s maintenance channel for loop and error messages on subscriber lines.

UIC enables full duplex continuous data transmission via the standard twisted pair telephone cable. Adaptive Echo cancellation is used to restore the received data. An equalizer, done with an adaptive filter, restores the data which are distorted by the transmission line.

The coefficient of the equalizer and echo canceller are conserved during a power down. An all digital PLL performs both bit and frame synchronization.

The analog front end consists of receive path RX and transmit path TX, providing a full duplex analog interfacing to the twisted pair telephone cable. Before data are converted to analog signals, they pass through a digital filter (TX-filter) to reduce the high frequency components. After D/A conversion the signal is amplified and sent to the hybrid.

The received signal is converted back to digital data and passed through the RX matching filter to restore the line signal. The A/D convertor is a second order sigma/delta modulator which operates with a clock of 15.36 MHz. After timing recovery, achieved by a digital PLL, the received signal is equalized, in an adaptive digital filter, to correct for the frequency and group delay distortion of the line.

Power supply status can be read via PFOFF. The UIC can disable its power supply (DISS), and two relay drivers outputs are provided (accessible via B2*) to control the power feed unit (RD1,RD2).

PIN CONNECTION (Top view)

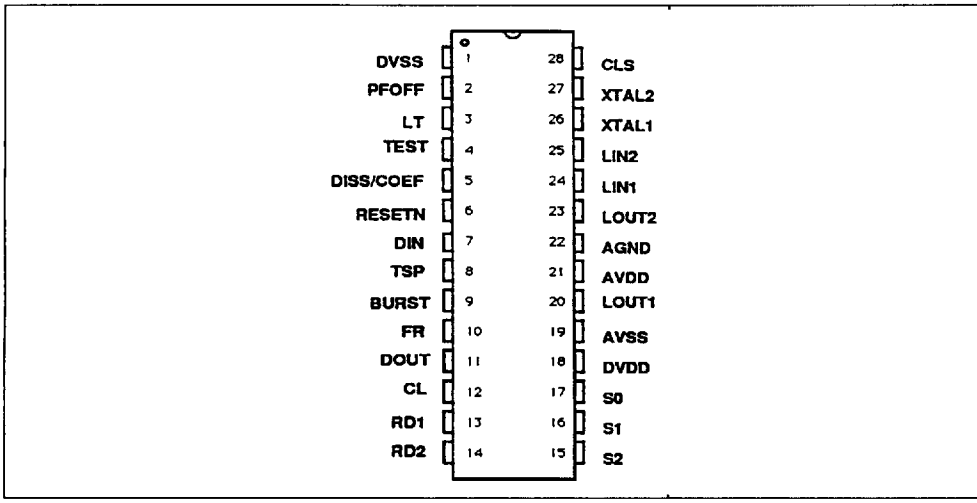
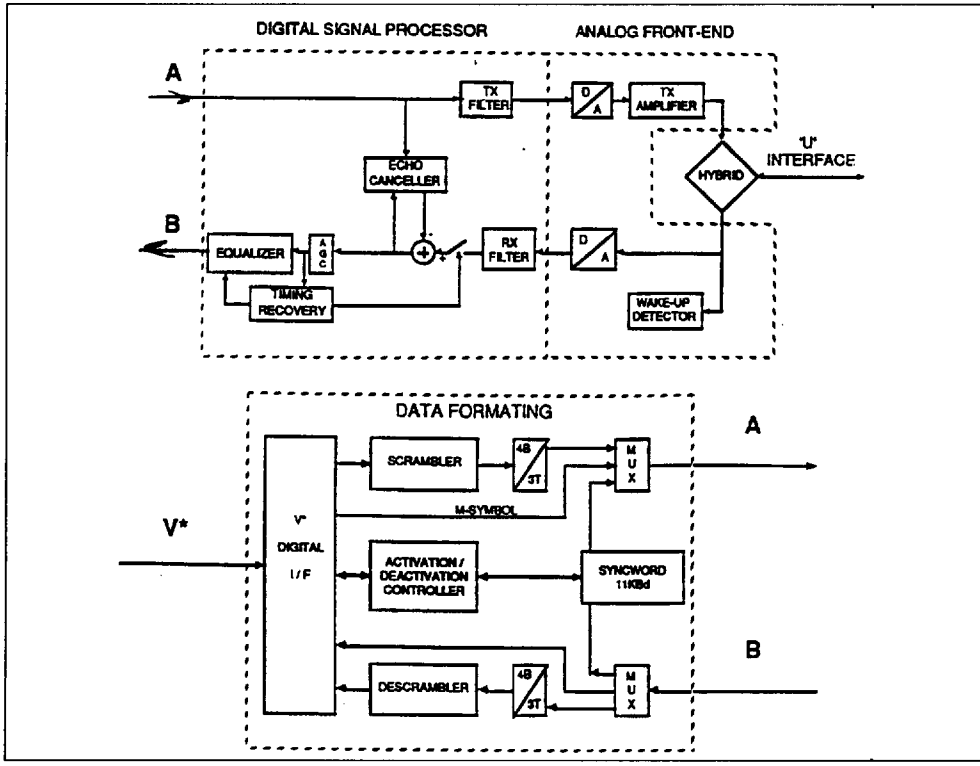


Figure 1: UIC Schematic Block Diagram



PIN DESCRIPTION

Pin	Name	Function
1	DVSS(input)	Digital Ground.
2	PFOFF(input)	Power feed off. PFOFF=HIGH is coded by the A-bit indication HI accessible on DOUT. Active in LT mode only.
3	LT(input)	LT/NT mode selection.
4	TEST(input)	Test Mode.
5	DISS(output)	A bit channel driven pin. Active in LT mode only.
6	RESETN(input)	Hardware Reset.
7	DIN(input)	Digital interface input.
8	TSP(input)	Transmit single pulse. 1 KHz single pulse alternating positive and negative polarity is transmitted.
9	BURST(input)	Burst mode selection. Active in LT mode only.
10	FR(in/out)	8KHz Digital interface frame clock; input in LT and output in NT mode.
11	DOUT(output)	Digital interface output.
12	CL(in/out)	Digital interface bit clock; input in LT and output in NT mode.
13	RD1(output)	Power feeder relay driver.
14	RD2(output)	Power feeder relay driver.
15, 16, 17	S2,S1,S0	Time slot pin strap (. Active in LT mode only.
18	DVDD(input)	5V +/-5% positive digital power supply.
19	AVSS(input)	Analog Ground.
20	LOUT1(output)	Output to the line.
21	AVDD(input)	5V +/-5% positive analog power supply.
22	AGND(input)	Analog Ground.
23	LOUT2(output)	Output to the line.
24,25	LIN1,LIN2(input)	Inputs from the line (UK0).
26, 27	XTAL1,XTAL2(inputs)	System clock input;nominal frequency is 15.36MHz.
28	CLS(output)	Clock output synchronous to the line receive clock at 7.68MHz.

APPLICATION AND MODES

The UIC can be used in LT, LT-burst and in NT mode.

Hereafter a list of the pin bias to set up the desired mode is given.

In LT mode:

Pins	Value
LT	1
BURST	0
S0	0
S1	0
S2	0

In LT burst:

Pins	Value
LT	1
BURST	1
S0	time slot
S1	time slot
S2	time slot

In NT:

Pins	Value
LT	0
BURST	0
S0	0
S1	0
S2	1

Test pins should always be tied to GND

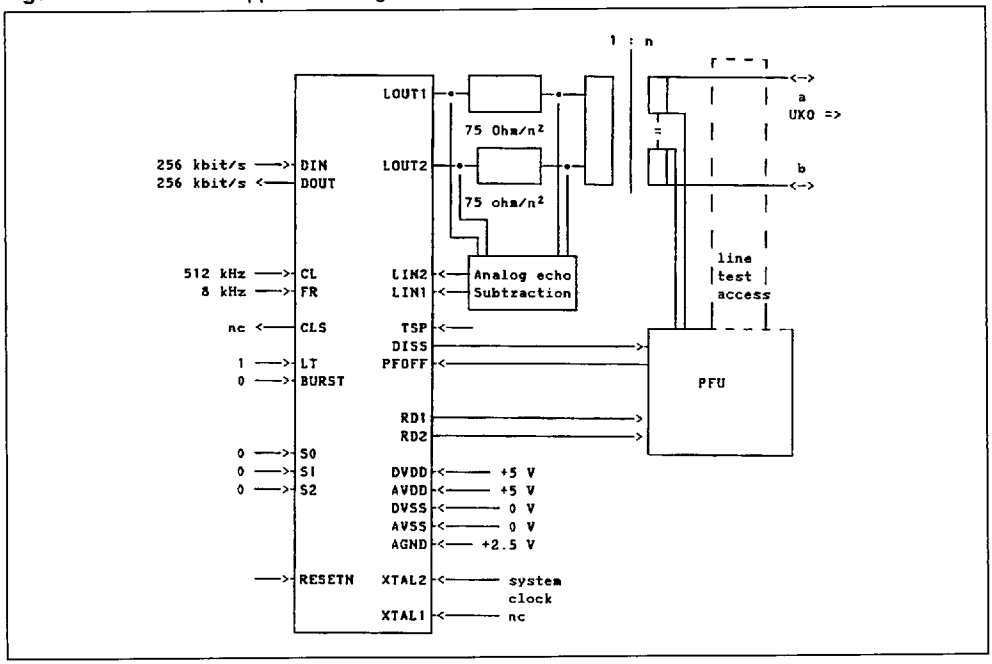
MODE DEPENDENT FUNCTIONS

PIN		MODE		
		LT burst	NT	LT
LT	input	1	0	1
BURST	input	1	0	0
S2, S1, S0	input	static	1 0 0	0 0 0
DIN DOUT	input output	2048 kbit/s	256 kbit/s	256 kbit/s
CLS (MHz)	output	7.68	7.68	7.68
CL (KHz)	input output	4096 –	– 512	512 –
FR (KHz)	input output	8 –	– 8	8 –

RECOMMENDED APPLICATIONS

LT mode

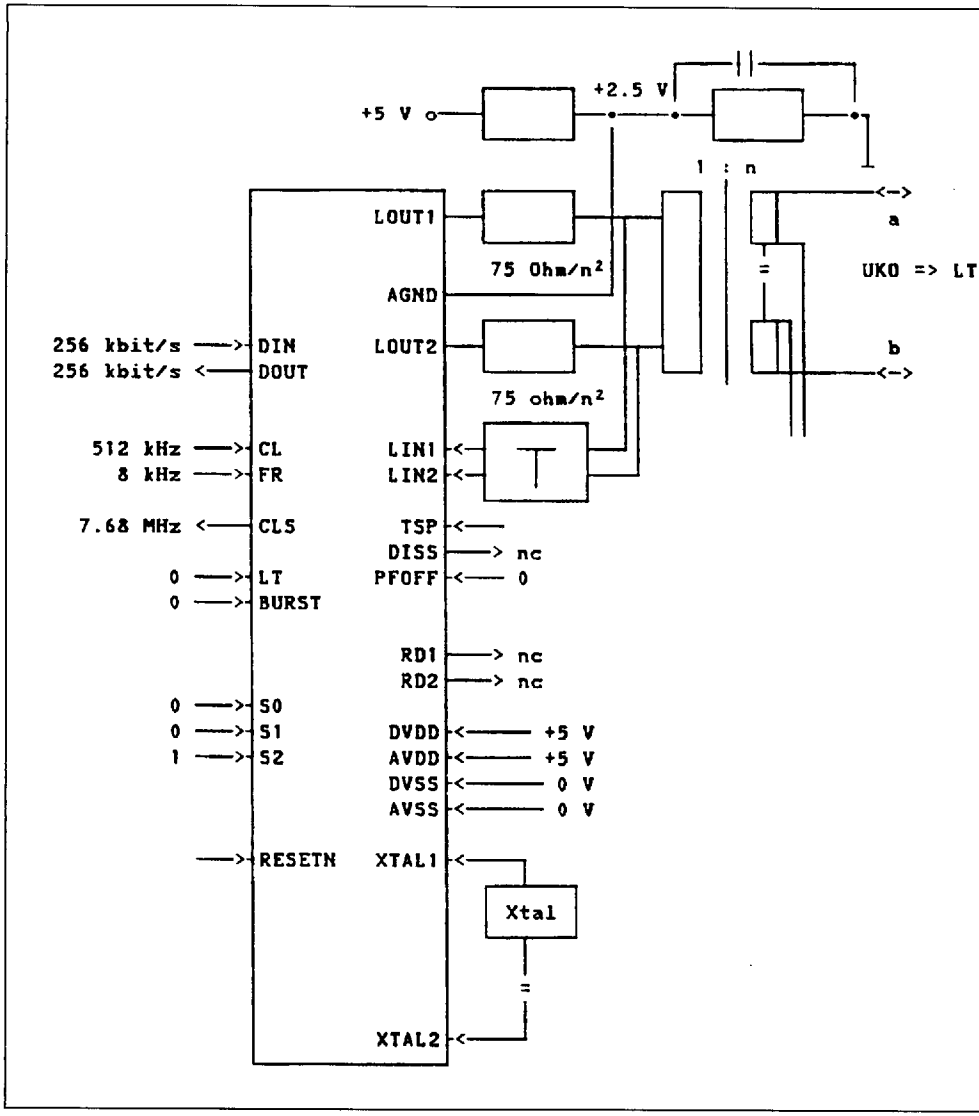
Figure 2: LT Schematic Application Diagram



DIN: Data input, datarate = 256 kbit/s, continuous
DOUT: Data output, datarate = 256 kbit/s, continuous
CL: Data clock input, f = 512 KHz
FR: Frame clock input, f = 8 KHz (1:1)
XTAL2: System clock input, f = 15.36 MHz (Tx clock synchronous to system clock)
CLS: Clock output, 7.68 MHz

NT mode

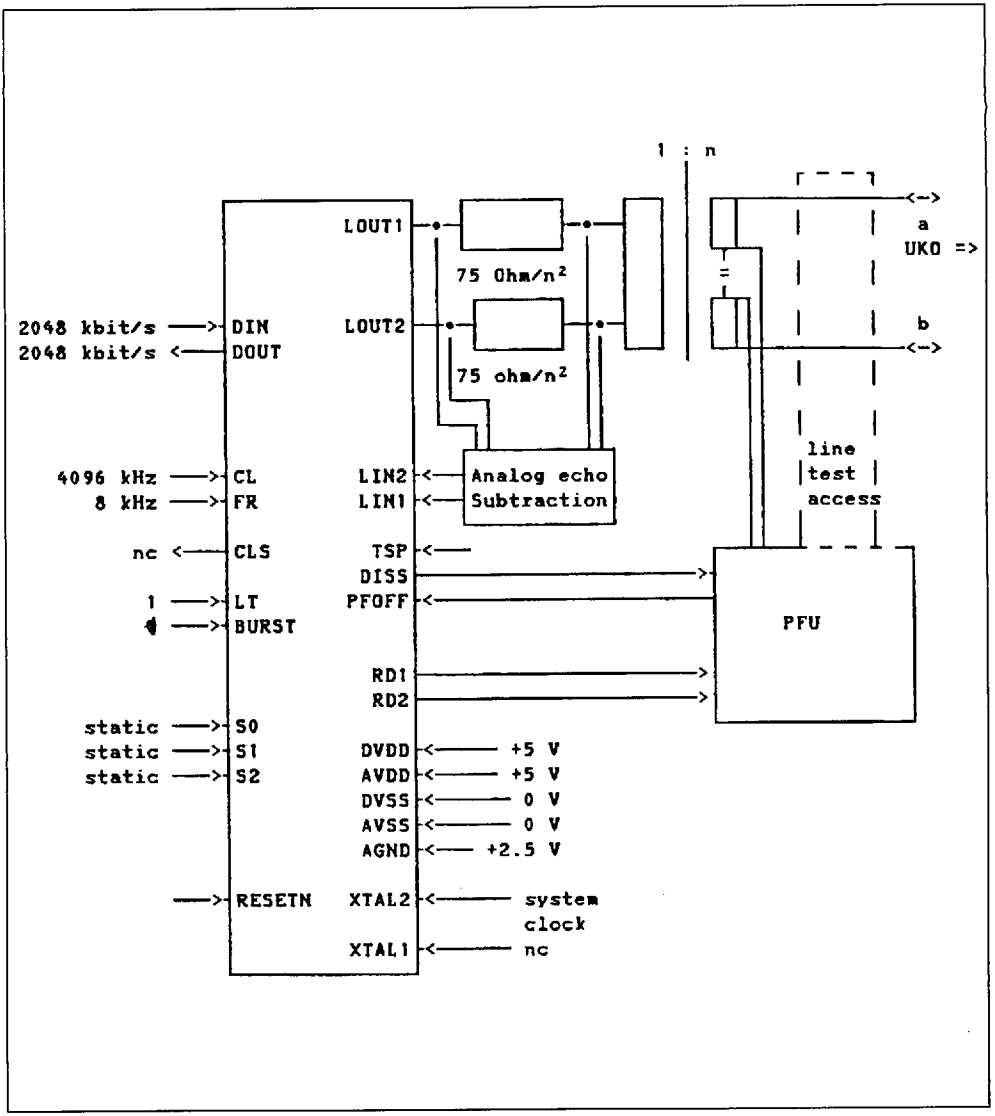
Figure 3: LT Schematic Application Diagram



DIN:	Data input, datarate = 256 kbit/s, continuous
DOUT:	Data output, datarate = 256 kbit/s, continuous
CL:	Data clock input, f = 512 KHz
FR:	Frame clock input, f = 8 KHz (1:1)
XTAL1/2:	15.36 MHz Xtal connection (Clock not synchronous to system clock)
CLS:	Clock output, 7.68 MHz (used to synch S interface)

LT burst mode

Figure 4: LT Burst Mode Schematic Application Diagram.



DIN:	Data input, datarate = 2048 kbit/s, continuous
DOUT:	Data output, datarate = 2048 kbit/s, continuous
CL:	Data clock input, f = 4096 KHz
FR:	Frame clock input, f = 8 KHz (1:1)
XTAL2:	System clock input, f = 15.36 MHz (Tx clock synchronous to system clock)
CLS:	Clock output, 7.68 MHz

DIGITAL INTERFACE

UIC is provided with a digital serial interface, named V*, which operates in two modes.

In Fig. 5 the frame format for both modes is shown.

The base frame consists of:

B1 : 64 kbit/s transparent data channel
B2 : 64 kbit/s transparent data channel
B2* : Monitor channel
B1* : 8 bits so set
D1/D2 : 16 kbit/s D channel
A1..A4 : Command/Indicate channel
T : Transparent service channel
E : Extension bit

In Fig. 6 and 7 the timings in Continuous and in Burst mode are given.

Figure 5: V* Frame Format.

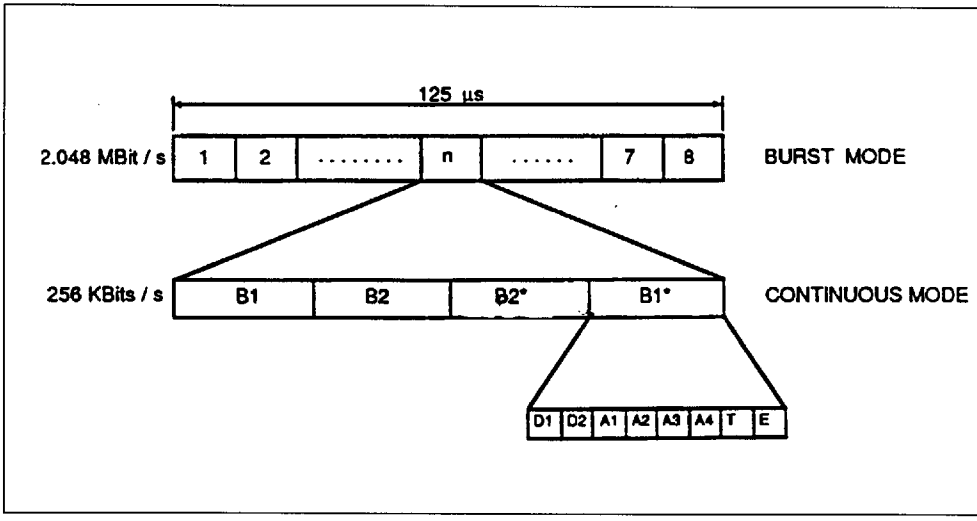


Figure 6: Continuous Mode.

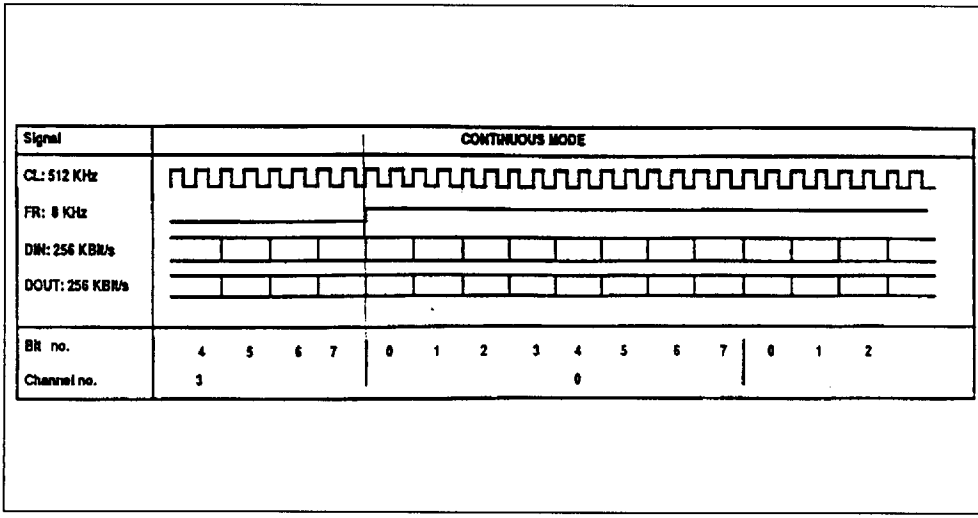
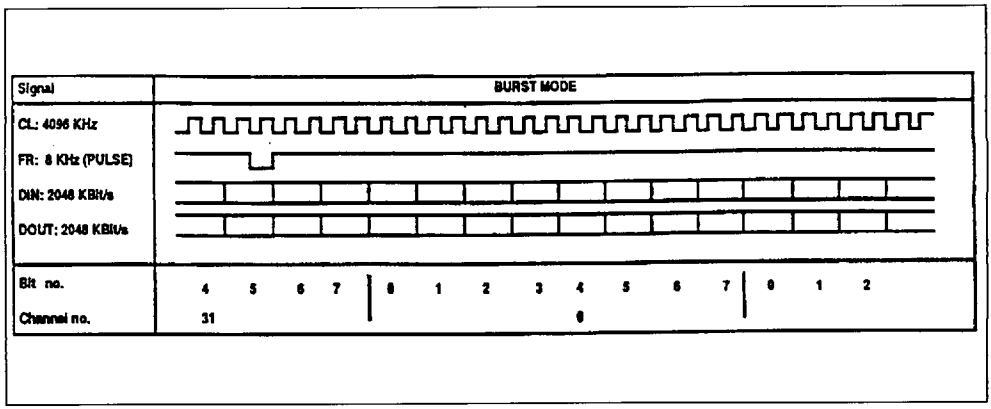


Figure 7: Burst Mode.



LINE FRAME STRUCTURE.

The information flow across the subscriber line uses the frame structure here below. The length of one frame corresponds to 120 ternary symbols being transmitted within 1 ms.

1	2	3	4	5	6	7	8	9	10	11	12		
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1		
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	24	
T1	T1	T1	T2	T2	T2	T2	T2	T2	T2	T2	T2	36	
T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	48	
T2	T2	T2	T2	T2	T2	T3	T3	T3	T3	T3	T3	60	LT ⇒ NT
T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	72	
T3	T3	T3	T3	T3	T3	T3	T3	T3	T4	T4	T4	84	
T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	96	
T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	108	
T4	SW1											120	

1	2	3	4	5	6	7	8	9	19	11	12		
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5		
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	24	
M2	T5	T5	T5	T6	T6	T6	T6	T6	T6	T6	T6	36	
T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	48	
T6	SW2											60	NT ⇒ LT
T6	T6	T6	T6	T6	T6	T7	T7	T7	T7	T7	T7	72	
T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	84	
T7	T7	T7	T7	T7	T7	T7	T7	T7	T8	T8	T8	96	
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	108	
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	120	

Agenda:

T1.....T8 B + B + D - Data (ternary)
M1, M2 Service Data (ternary)
SW1, SW2 Synchronizing Word

Maintenance and service channel.

The ternary symbols M1 and M2 represent non-scrambled data that can be transmitted at a rate of 1 kBaud. Those symbols are used for various purposes:

- Maintenance Channel (control test loops (LT → NT) and frame errors (LT → NT)
- Service channel (transparent user data and transmit messages from NT to LT)

Encoding.

The encoding of a binary bit stream is made such that 4 binary bits correspond to 3 symbols of ternary symbol stream. The encoding follows the rules of modified monitoring state 43 (MMS43).

COMMAND / INDICATE CHANNEL (A bits)

Command/Indicate codes are define depending on the mode selected (LT or NT).

NT mode COMMANDS (DIN)

ACT	1 0 0 0	Activate. Layer 1 is activated at the UK0 interface starting with a 'wake-up' signal INFO U1W, followed by INFO U1A during synchronization and closed by INFO U1 when synch is gained.
AW	0 0 0 0	Awake. Set the module interface from the power-down to the power-up state. No signal is emitted at UK0 interface. Even DIN pin pulled LOW can have the same effect.
DC	1 1 1 1	Deactivation confirmation. The module interface is deactivated. The transmitter is disabled but the receiver is still enabled to recognize an awake signal. THe UIC is set in power down state.
RES	1 1 0 1	Reset. Reset the UIC to the initial state.
SY	1 1 0 0	Synchronize. Drive the UIC in connect through from module interface to line interface.

Remark: Executing the command RES (1101) is functionally equivalent to pulling the RESETN pin (6) LOW, with one exception:

a) RES command set pin DISS to HIGH (+5V)
b) pulling RESETN LOW set pin DISS to LOW (0V).

NT mode INDICATION (DOUT)

ACT	1 0 0 0	Activate. The synchronous state of the receiver is reached.
DC	1 1 1 1	Deactivation confirmation. The transmitter is disabled but the receiver remains enabled to detect awake signals at UK0 UIC is set in power down state.
DEAC	0 0 0 0	Deactivate. A request to deactivate INFO U0 has been detected.
CT	1 1 0 0	Connection Through. The UIC is fully activated.
CTL2	1 1 1 0	Connection through with loop 2. A loop 2 command has been detected at UK0.
L2	1 0 1 0	Loop 2. Synchronization has been reached during a Loop 2 activation procedure.
RSYN	0 1 0 0	Resynchronization. The receiver has lost framing and is attempting to resynchronize.

LT mode COMMANDS (DIN)

ACT	1000	Activate. UIC is set in power-up state, executing the complete activation of Layer 1. The transparent channel transmission is enabled.
AL	1001	Analog Loop. The analog transmitter output is looped back to the receiver input which is disconnected from UK0 interface. A pseudo wake-up procedure is executed.
L2	1010	Loop 2. Command to close Loop 2 in NT.
LTD	0011	Line Transmission Disabled. UIC stops transmitting signals on the line and is powered down.
DEAC	0000	Deactivate. Request to deactivate UK0.
RES	1101	Reset. Reset the UIC to the initial state.
SSP	0101	Send Single Pulse. The UIC transmits single pulse at 1 ms time intervals with alternate polarity.

LT mode INDICATION (DOUT)

ACT	1000	Activation running. UIC is powered-up and the activation procedure is running.
RDS	0111	Running Digital Sum. Given during activation procedure. The receiver has reached synchronization.
CT	1100	Connection Through. Layer 1 activation procedure has been completed. B and D channels are transparently connected.
DEAC	0001	Deactivation running. UIC is deactivating in response of a DEAC, RES or LTD command.
DC	1111	Deactivation confirmation. UIC has completed the deactivation procedure.
RSYN	0100	Resynchronization. The receiver has lost framing and is attempting to resynchronize.
HI	0011	High Impedance. When pin PFOFF is HIGH indication HI is output and UIC starts transmitting INFO U0. Normally used to indicate that remote feeding has been switched off.

POWER DOWN STATE

Power consumption of most functions is reduced; module interface is not active; C/I messages cannot be exchanged.

ACTIVATION DEACTIVATION

The ACTIVATION procedure consists of three steps: AWAKE, SYNCHRONIZE and CONNECT THROUGH.

Activation times are (max):

COLDSTART 1 sec

WARMSTART 170 msec

The DEACTIVATION procedure consists of two steps: line DEACTIVATION and POWER DOWN.

Deactivation time is (typ) 4 ms.

OSCILLATOR

Oscillators of 15.36 MHz are required. When in NT a tollerances of +/-30 ppm is allowed, it is advisable to use in LT a tollerances of +/-20 ppm.

LINE RANGE

The LINE RANGE depends on the cable section. Typically:

up to 4.2Km with 0.4mm cable

- 5.5Km - 0.5mm -
- 8.0Km - 0.6mm -

Assumed noise level for such performances is 10uV/SQRT(Hz) on a 200KHz bandwidth.

LT CLOCK JITTER

The phase jitter between Master Clock (15.36MHz) and interface clock (4.096MHz) should not exceed 50ns.

ELECTRICAL CHARACTERISTICS

Supply Voltages:

DVDD = 5V +/- 5%

AVDD = 5V +/- 5%

AGND = 2.5V +/- 5% (max curr 0.25mA)

Power consumption

Active = max 280mW (line loaded at 150Ohm)

Power down = max 30mW

DIGITAL INTERFACE STATIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		3.5			V
V_{IL}	Low Level Input Voltage				1.0	V
V_{OH1}	High Level Output Voltage all outputs except DOUT	I_{OH1} = 0.4mA	V_{DD}-0.66			V
V_{OH2}	High Level Output Voltage DOUT, (Open Drain)	R to DV_{DD} R = 1KΩ	4			V
V_{OL1}	Low Level Output Voltage all outputs except DOUT	I_{OL1} = 0.4mA			0.33	V
V_{OL2}	Low Level Output Voltage DOUT, (Open Drain)	I_{OL1} = 0.7mA			0.4	V
C_{IN}	Inputs Capacitance, all inputs at DOUT if output is off				10 10	pF pF
C_{OUT}	Load Capacitance at all outputs except at DOUT				25	pF
C_{OUT}	Load Capacitance at DOUT				150	pF
I_{IN}	Input Leakage Current				1	µA

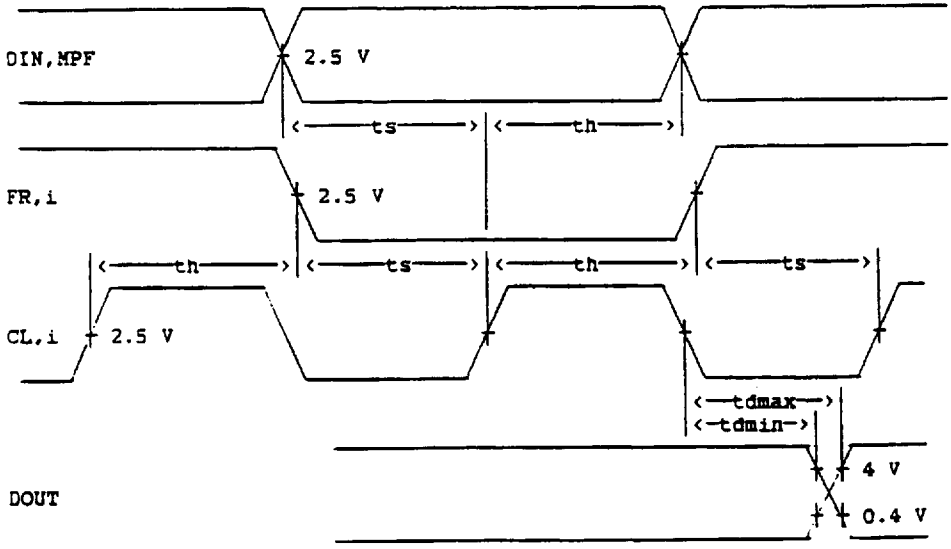
DIGITAL INTERFACE DYNAMIC CHARACTERISTICS

Burst mode.

Parameter	Port	from	to	Conditions		Min.	Max.
				C	R to DVDD		
				pF	KΩ	ns	ns
Rise Time tr	FR, CL	1.0V	3.5V	10			30
Fall Time tf	FR, CL	3.5V	1.0V	10			30
Setup Time ts	FR	FR, i –	CL, i +			30	
Setup Time ts	FR	FR, i +	CL, i +			30	
Setup Time ts	DIN	DIN +/–	CL, i +			50	
Setup Time ts	MPF	MPF +/–	CL, i +			50	
Hold Time th	FR	CL, i +	FR, i –			50	
Hold Time th	FR	CL, i +	FR, i +			50	
Hold Time th	DIN	CL, i +	DIN +/–			60	
Hold Time th	MPF	CL, i +	MPF +/–			60	
Delay Time td	DOUT	CL, i –	DOUT +/–	50	1	0	150
Delay Time td	DOUT	CL, i –	DOUT +/–	150	1	0	200
Clock Width tc	CL, i	CL +/–	CL +/–			239	249
Clock Width tc	CL, i	CL +/–	CL –/+			100	144

+ = rising edge

– = falling edge



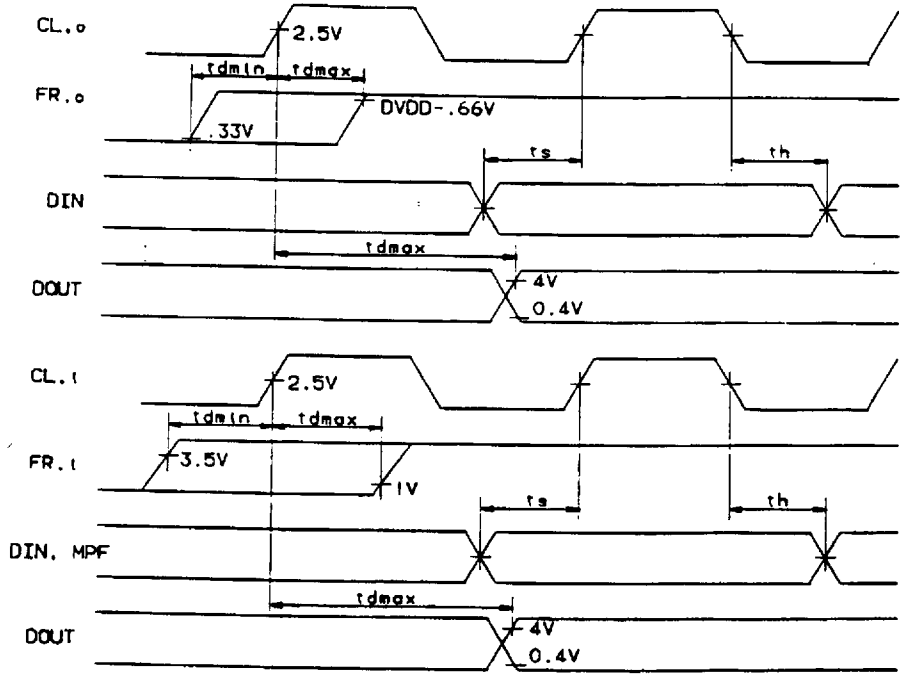
DIGITAL INTERFACE DYNAMIC CHARACTERISTICS (continued)

Continuous mode.

Parameter	Port	from	to	Conditions		Min.	Max.
				C	R to DVDD		
				pF	KΩ	ns	ns
Rise Time tr	FR, CL, i	1.0V	3.5V	10			30
Fall Time tf	FR, CL, i	3.5V	1.0V	10			30
Rise Time tr	FR, CL, o	10%	90%	25			30
Fall Time tf	FR, CL, o	90%	10%	25			30
Setup Time ts	DIN	DIN +/–	CL, i +			50	
Setup Time ts	MPF	MPF +/–	CL, i +			50	
Delay Time td	FR	CL, i +	FR, i +			-200	200
Hold Time th	DIN	CL, i –	DIN +/–			100	
Hold Time th	MPF	CL, i –	DIN +/–			100	
Delay Time td	DOUT	CL, i +	DOUT +/–	25	10		500
Setup Time ts	DIN	DIN +/–1	CL, o +			50	
Setup Time th	DIN	CL, o –	DIN +/–			100	
Delay Time td	DOUT	CL. o +	DOUT +/–	25	10		500
Delay Time td	FR	CL, o +	FR,o +	25		-150	150
Clock Width tc	CL, i	CL +/–	CL +/–			1830	2080
Clock Width tp	CL, i	CL +/–	CL +/–	25		1830	2080
Pulse Width tp	CL, i	CL +/–	CL –/+			850	1100
Pulse Width tp	CL, i	CL +/–	CL –/+	25		850	1100

+ = rising edge

– = falling edge



DIGITAL INTERFACE DYNAMIC CHARACTERISTICS (continued)

Master clock.

Parameter	Port	from	to	Conditions C pF		Min. ns	Max. ns
Rise Time tr Fall Time tf	XTAL2 XTAL2	1.0V 3.5V	3.5V 1.0V	10 10			15 15
Rise Time tr Fall Time tf	CLS CLS	10% 90%	90% 10%	25 25			15 15
Pulse Width	CLS	CLS +/–	CLS –/+	25		20	

+ = rising edge

– = falling edge

Setup Time ts Hold Time th Delay min. td Delay max. td	DIN, FR, i +/– CL, i + CL, i + CL, i – CL, i + CL, i –	2.5V 2.5V 2.5V 2.5V	CL, i + DIN, FR, i +/– DOUT +/– DOUT +/–	2.5V 2.5V 0.4 / 4V 4 / 0.4V
Delay min. td (negative) Delay max. td	CL, i + CL, i +	2.5V 2.5V	FR, i + FR, i +	3.5V 1V
Setup Time ts Hold Time ts Delay max. td Delay min. td (negative) Delay max. td	DIN, +/– CL, o + CL, o + CL, o + CL, o +	2.5V 2.5V 2.5V 2.5V 2.5V	CL, o + DIN +/– DOUT +/– FR, o + FR, o +	2.5V 2.5V 4 / 0.4V 0.33V VDD - 0.66V
Pulse Width tp Clock Width tc	CL, o +/– CL, o +/–	2.5V 2.5V	CL, o –/+ CL, o +/–	2.5V 2.5V
Pulse Width tp Clock Width tc	CLS, MXCL +/– CLS, MXCL +/–	2.5V 2.5V	CL, o –/+ CL, o +/–	2.5V 2.5V