



STQ1NC60

N-CHANNEL 600V - 12Ω - 0.3A TO-92

PowerMesh™ II MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STQ1NC60	600 V	< 15 Ω	0.38 A

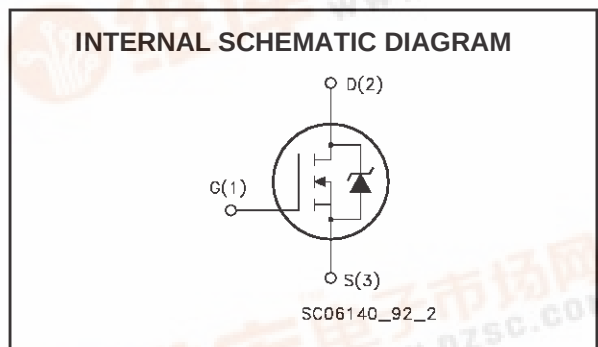
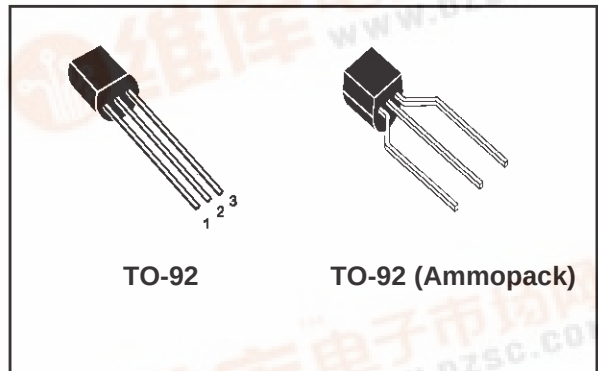
- n TYPICAL R_{DS(on)} = 12 Ω
- n EXTREMELY HIGH dv/dt CAPABILITY
- n 100% AVALANCHE TESTED
- n NEW HIGH VOLTAGE BENCHMARK
- n GATE CHARGE MINIMIZED
- n ADD SUFFIX "-AP" FOR ORDERING IN AMMOPAK

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ II process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- n SWITCH MODE LOW POWER SUPPLIES (SMPS)
- n BATTERY CHARGER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C	0.38	A
I _D	Drain Current (continuous) at T _C = 100°C	0.24	A
I _{DM} (t)	Drain Current (pulsed)	1.52	A
P _{TOT}	Total Dissipation at T _C = 25°C	3.1	W
	Derating Factor	0.028	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤ 0.3 A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

STQ1NC60

THERMAL DATA

		TO-92	
Rthj-amb	Thermal Resistance Junction-ambient Max	120	°C/W
Rthj-lead	Thermal Resistance Junction-lead Max	40	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	260	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	0.3	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	60	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 µA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 0.3 A		12	15	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs}	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 0.3 A		0.87		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		108		pF
C _{oss}	Output Capacitance			18		pF
C _{rss}	Reverse Transfer Capacitance			2.5		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300V, I_D = 0.5 A$		7.2		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		8		ns
Q_g	Total Gate Charge	$V_{DD} = 480V, I_D = 1 A,$		7.3	10	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10V, R_G = 4.7\Omega$		3.4		nC
Q_{gd}	Gate-Drain Charge			2.5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(voff)}$	Off-voltage Rise Time	$V_{DD} = 480 V, I_D = 1 A,$		33		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		11		ns
t_c	Cross-over Time			43		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				0.3	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				1.2	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 0.3 A, V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 1 A, di/dt = 100A/\mu s,$		450		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 25V, T_j = 150^\circ C$ (see test circuit, Figure 5)		720		μC
I_{RRM}	Reverse Recovery Current			3.2		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

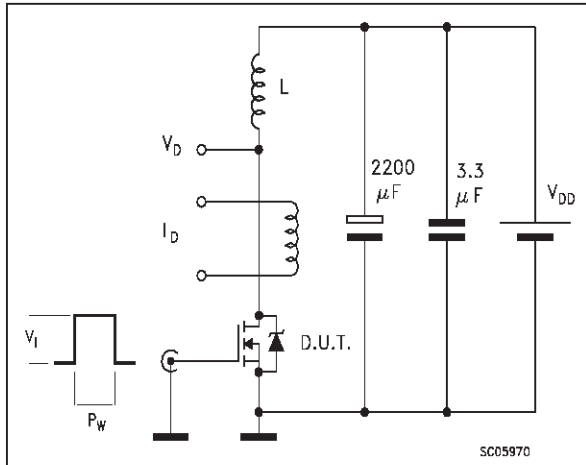


Fig. 2: Unclamped Inductive Waveform

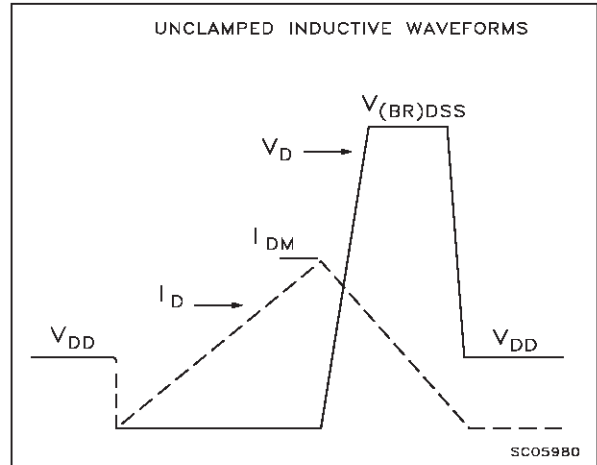


Fig. 3: Switching Times Test Circuit For Resistive Load

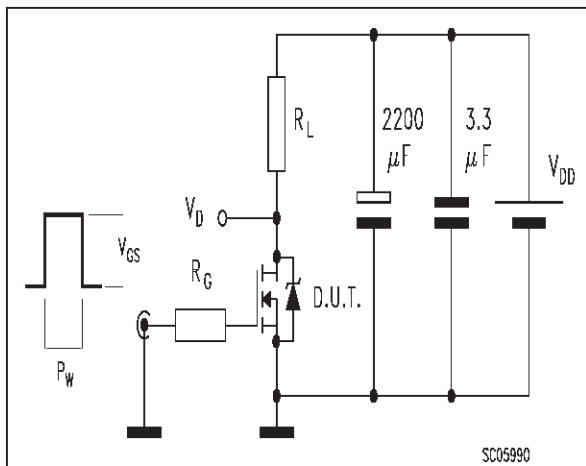


Fig. 4: Gate Charge test Circuit

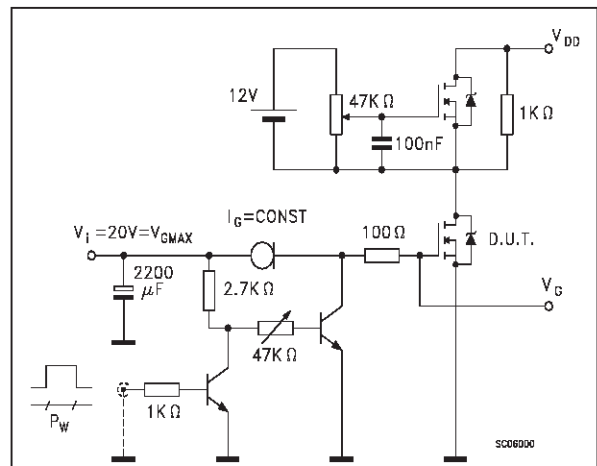
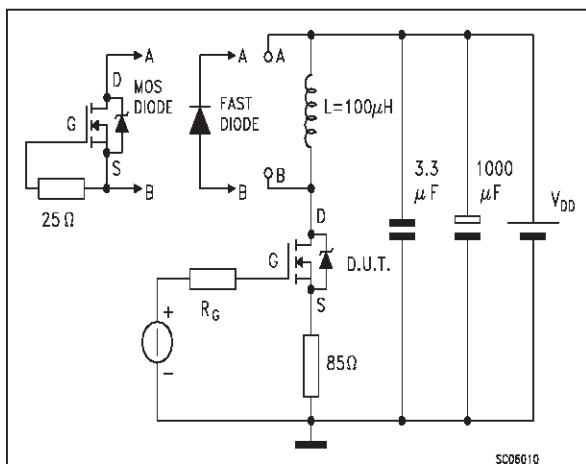
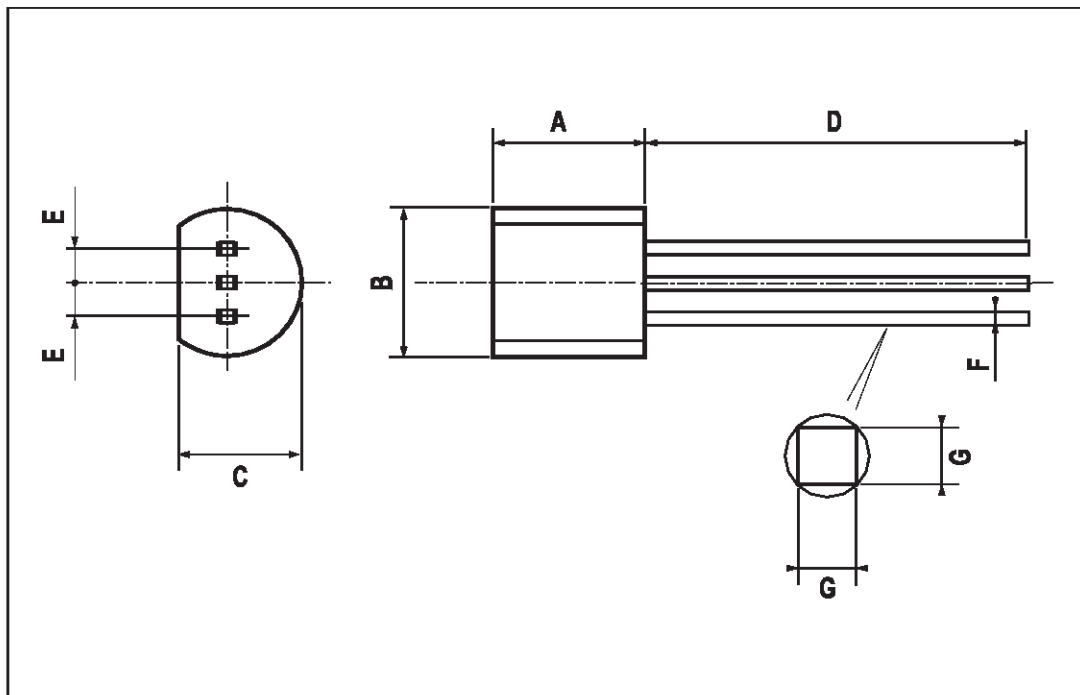


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-92 MECHANICAL DATA

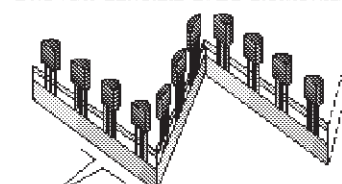
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.58		5.33	0.180		0.210
B	4.45		5.2	0.175		0.204
C	3.2		4.2	0.126		0.165
D	12.7			0.500		
E		1.27			0.050	
F	0.4		0.51	0.016		0.020
G	0.35			0.14		



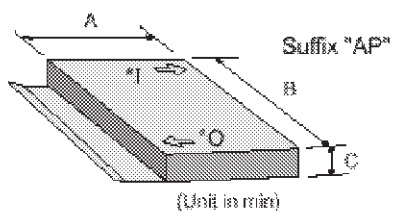
SHIPPING METHODS

TO-92 AMMOPACK (suffix "-AP")

One row consists of 25 elements

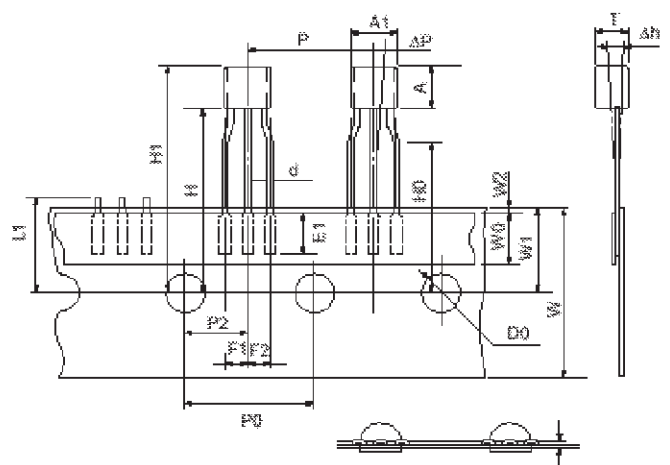


Remove more than 4 elements



* shows a first-out electrode of a lead.
O : Output first-out
I : Input first-out

DIM	mm	
	Min.	Max.
A	3	250
B	3	330
C	3	45



TAPING IN FORWARD DIRECTION

BOTTOM VIEW

DIM	mm	
	Min.	Max.
A1	-	5
A	-	5
T	-	4
d	-	0.45
E1	2.5	-
P	11.7	13.7
P0	12.4	13
Hole Center to Device Center	5.95	6.75
F1/F2	2.4	2.8
Δh	-1	1
ΔP	-1	1
W	17.5	19
W0	5.7	6.3
W1	8.5	9.75
W2	-	0.5
H	-	20
H0	15.5	16.5
H1	-	25
D0	3.8	4.2
t	0.4	0.8
L1	-	11

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