Advanced Power MOSFET

SSW/I3N80A

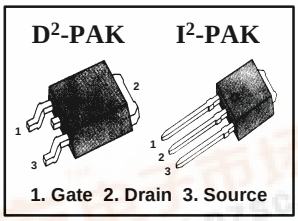
FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 μA (Max.) @ V_{DS} = 800V
- Low $R_{DS(ON)}$: 3.800 Ω (Typ.)

BV_{DSS} = 800 V

$R_{DS(on)}$ = 4.8 Ω

I_D = 3 A



Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	800	V
I_D	Continuous Drain Current (T_C=25 ℃)	3	A
	Continuous Drain Current (T_C=100 ℃)	1.9	
I_{DM}	Drain Current-Pulsed ①	12	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	240	mJ
I_{AR}	Avalanche Current ①	3	A
E_{AR}	Repetitive Avalanche Energy ①	10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
P_D	Total Power Dissipation (T_A=25 ℃) *	3.1	W
	Total Power Dissipation (T_C=25 ℃)	100	W
	Linear Derating Factor	0.8	W/℃
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	℃
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.25	℃/W
$R_{\theta CS}$	Case-to-Sink	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

* When mounted on the minimum pad size recommended (PCB Mount).

FAIRCHILD SEMICONDUCTOR™

SSW/I3N80A

N-CHANNEL
POWER MOSFET

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	800	--	--	V	V_{GS}=0V,I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	1.01	--	V/℃	I_D=250μA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	3.5	V	V_{DS}=5V,I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=30V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V_{DS}=800V
		--	--	250		V_{DS}=640V,T_C=125℃
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	4.8	Ω	V_{GS}=10V,I_D=0.85A ④*
g_{fs}	Forward Transconductance	--	2.17	--	Ω	V_{DS}=50V,I_D=0.85A ④
C_{iss}	Input Capacitance	--	580	750	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	60	75		
C_{rss}	Reverse Transfer Capacitance	--	23	30		
$t_{d(on)}$	Turn-On Delay Time	--	16	40	ns	V_{DD}=400V,I_D=2A, R_G=16 Ω ***See Fig 13*** ④⑤
t_r	Rise Time	--	26	60		
$t_{d(off)}$	Turn-Off Delay Time	--	46	100		
t_f	Fall Time	--	24	60		
Q_g	Total Gate Charge	--	27	35	nC	V_{DS}=640V,V_{GS}=10V, I_D=2A ***See Fig 6 & Fig 12*** ④⑤
Q_{gs}	Gate-Source Charge	--	5.3	--		
Q_{gd}	Gate-Drain(“Miller”) Charge	--	12.2	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	3	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	12		
V_{SD}	Diode Forward Voltage ④	--	--	1.4	V	T_J=25 ℃,I_S=3A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	330	--	ns	T_J=25 ℃,I_F=3A
Q_{rr}	Reverse Recovery Charge	--	1.52	--	μC	di_F/dt=100A/μs ④

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
② L=50mH, I_{AS}=3A, V_{DD}=50V, R_G=27Ω, Starting T_J=25 ℃
③ I_{SD}≤3A, di/dt ≤100A/μs, V_{DD} ≤BV_{DSS}, Starting T_J=25 ℃
④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤2%
⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

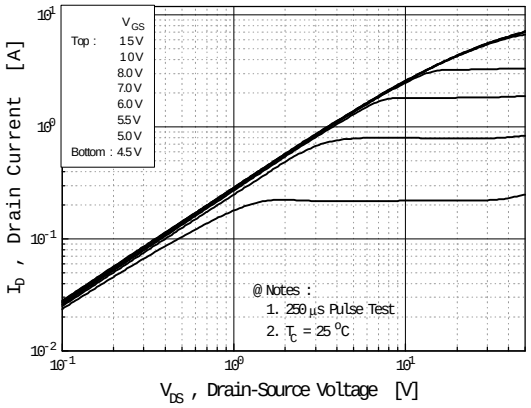


Fig 2. Transfer Characteristics

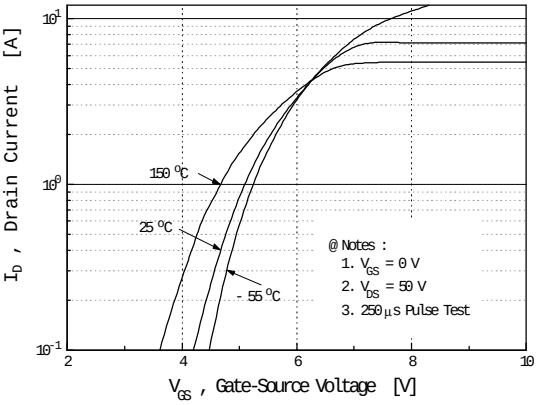


Fig 3. On-Resistance vs. Drain Current

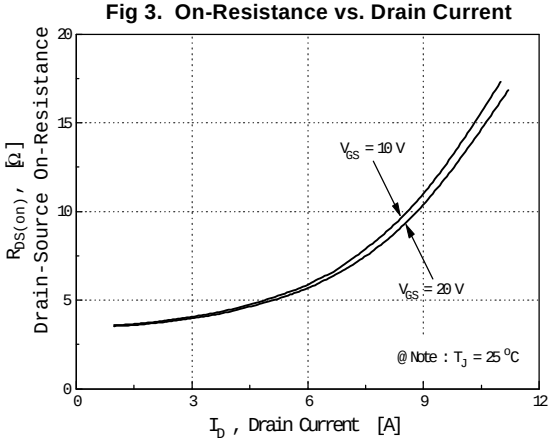


Fig 4. Source-Drain Diode Forward Voltage

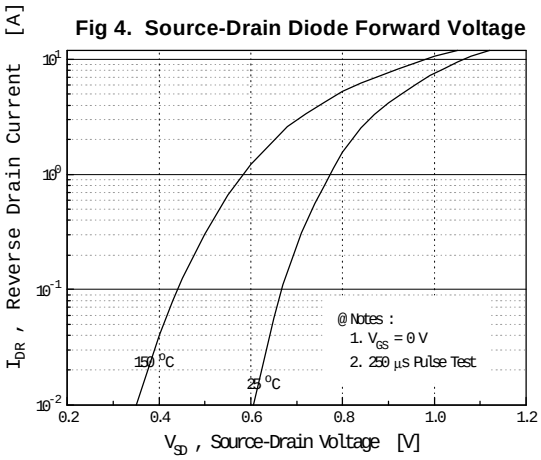


Fig 5. Capacitance vs. Drain-Source Voltage

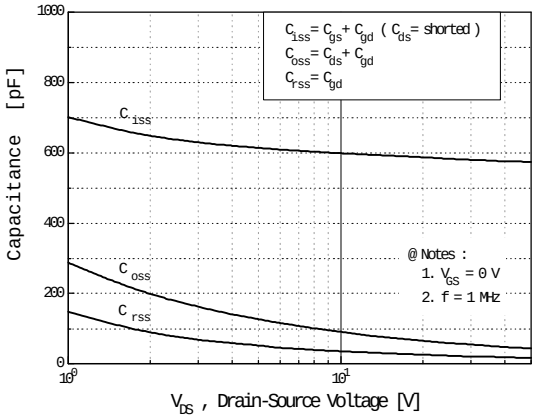


Fig 6. Gate Charge vs. Gate-Source Voltage

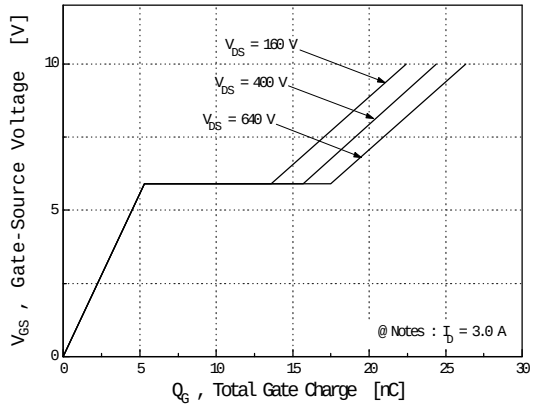


Fig 7. Breakdown Voltage vs. Temperature

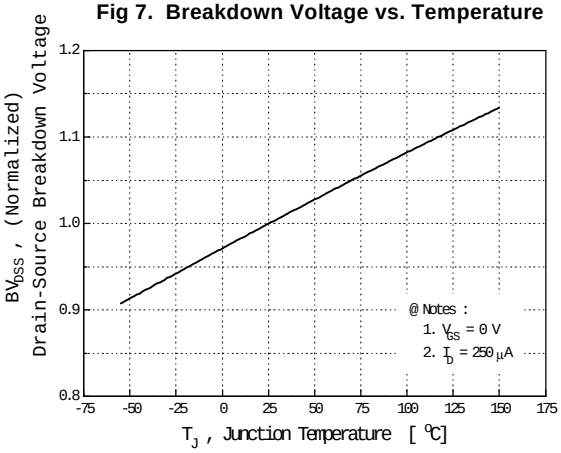


Fig 8. On-Resistance vs. Temperature

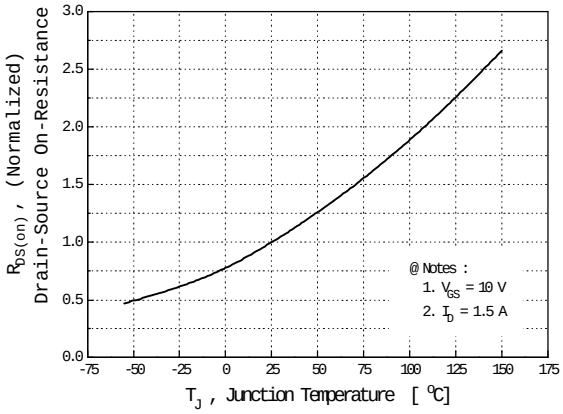


Fig 9. Max. Safe Operating Area

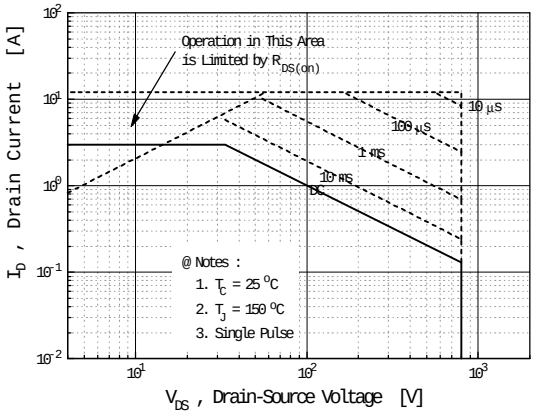


Fig 10. Max. Drain Current vs. Case Temperature

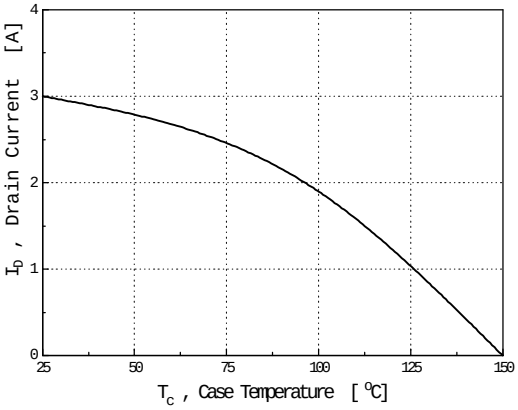


Fig 11. Thermal Response

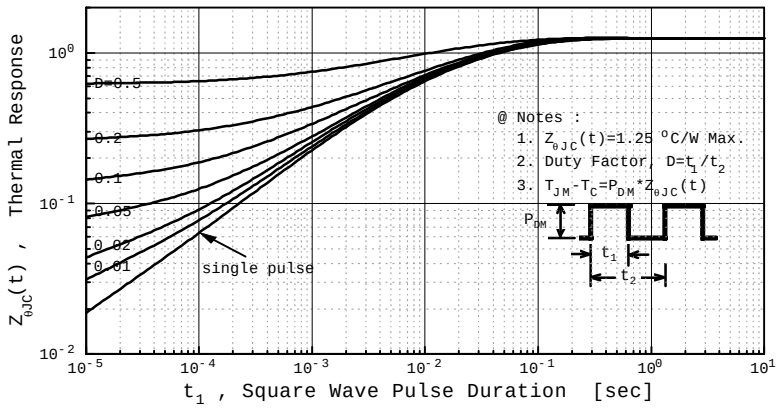


Fig 12. Gate Charge Test Circuit & Waveform

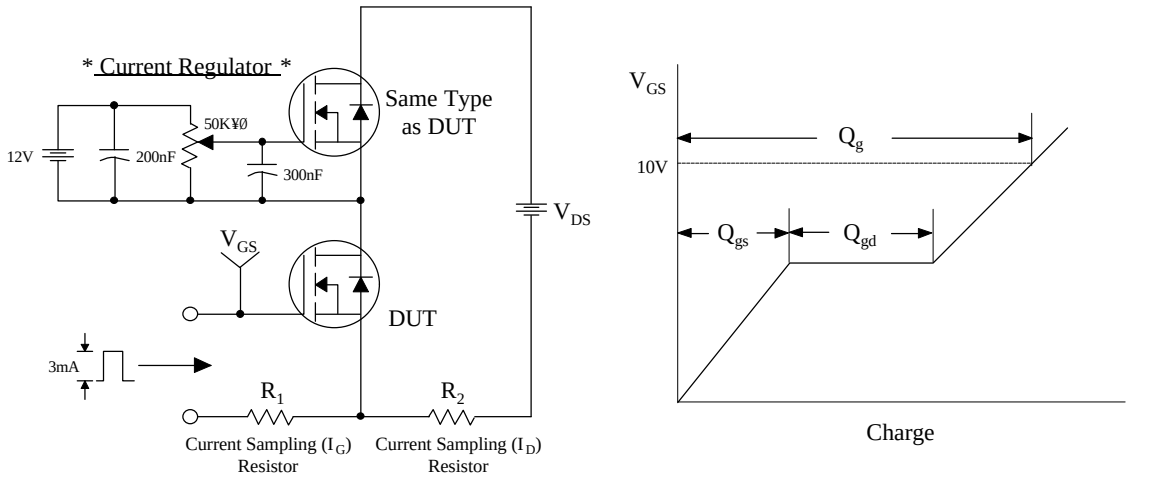


Fig 13. Resistive Switching Test Circuit & Waveforms

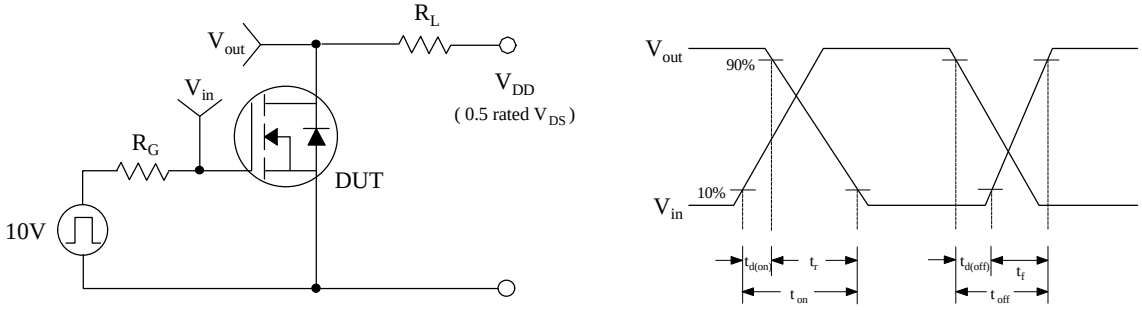


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

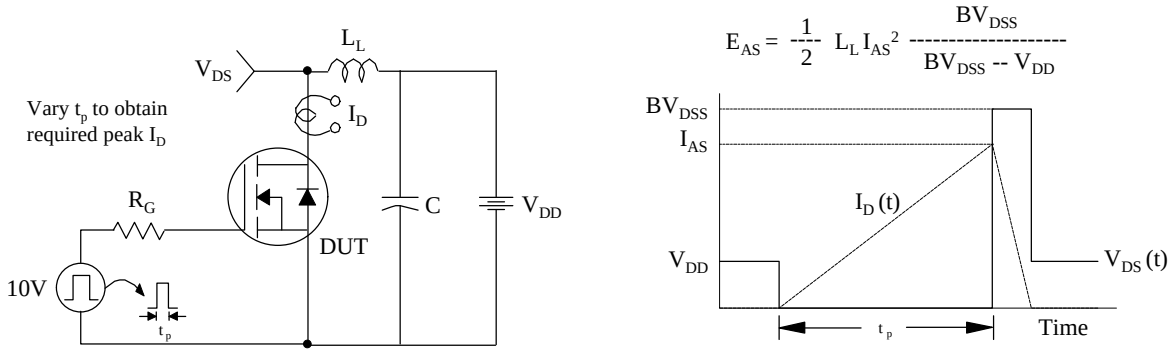
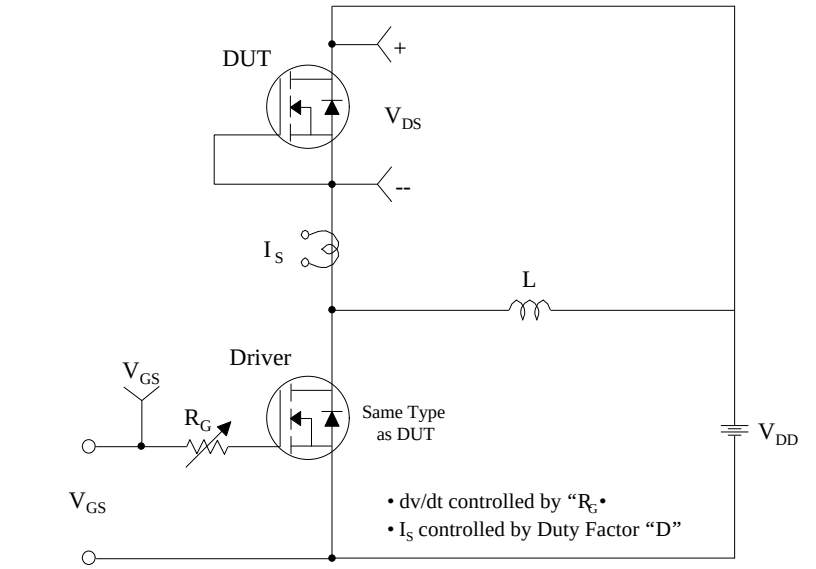
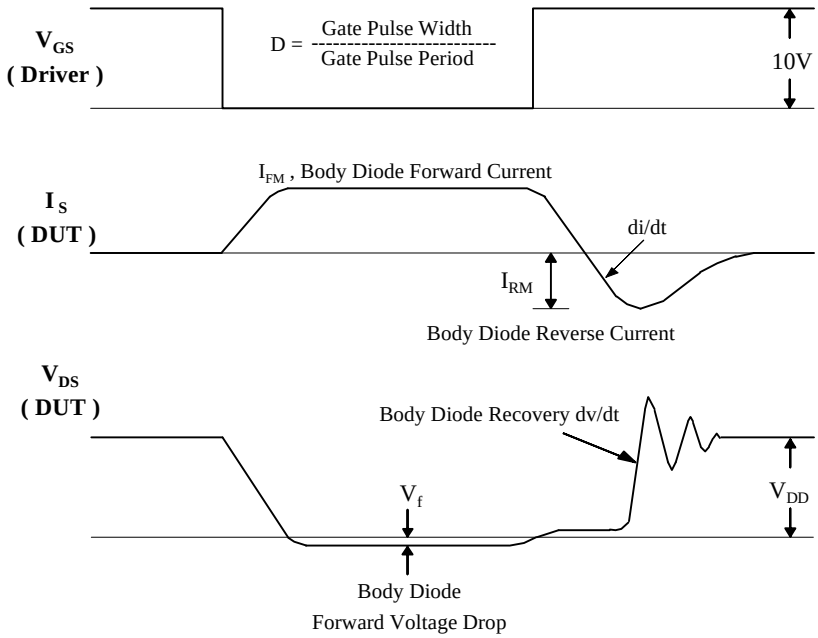


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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