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SSI 32D4666
Time Base Generator

May 1994

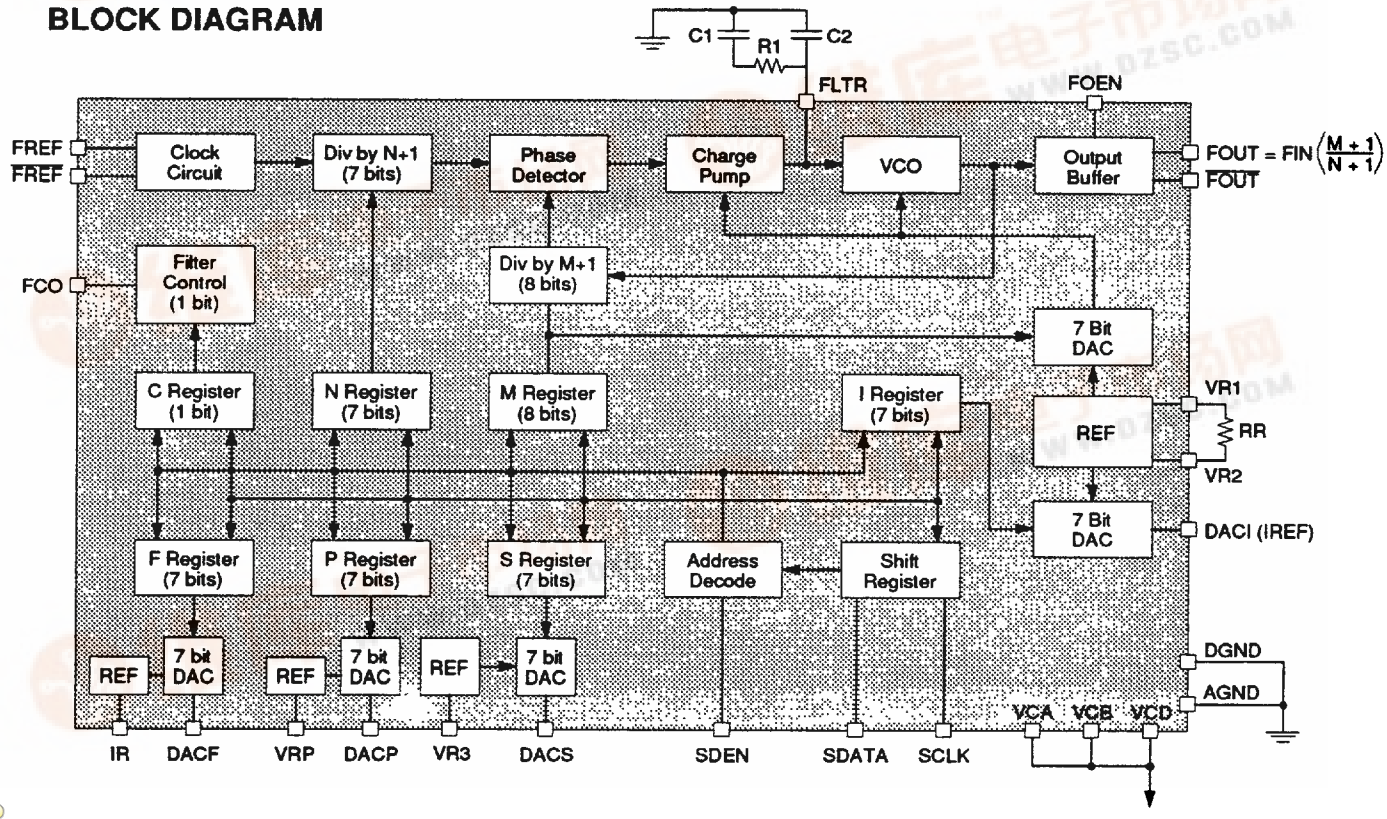
DESCRIPTION

The SSI 32D4666 is a high performance bipolar device that provides a programmable frequency reference and four internal control DACs to support hard disk drive applications that use zoned recording techniques. It is optimized for use with the 32P3000 family of pulse detector/filter devices and the 32D53X family of data separators. The frequency reference can be programmed up to 108 MHz with better than 1% resolution. The 7-bit DACs provide control of the 3 dB cutoff frequency and pulse slimming of the electronic filter, the hysteresis level of the pulse qualifier, and the center frequency of the data separator. A single latched TTL output is also provided to control switching of external loop filter components on the data separator. A serial microprocessor interface reduces the pin count and provides convenient access to the internal program storage registers. The 32D4666 requires a +5 VDC supply and is available in a 24-lead SOL and VSOP package.

FEATURES

- **Programmable frequency output up to 108 MHz**
- **1% frequency resolution**
- **Differential PECL reference clock input (FREF)**
- **Differential PECL frequency reference output (FOUT)**
- **7-bit DAC for data separator center frequency control (DACI)**
- **7-bit DAC for filter Fc control (DACF)**
- **7-bit DAC for filter boost/equalization control (DACS)**
- **7-bit DAC for hysteresis level control (DACP)**
- **+5 VDC operation**
- **Available in small footprint 24-lead SOL and VSOP packages**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

FREQUENCY REFERENCE OPERATION

The 32D4666 programmable frequency reference accepts a differential PECL compatible clock source and generates a differential PECL compatible reference output (FOUT/$\overline{\text{FOUT}}$). The output frequency of FOUT is controlled by programming internal M and N counters to set up internal divide-by ratios. The 7-bit N register sets the divide-by factor for the input clock source. This will determine the update frequency for the phase detector. The value of this register is set based upon the frequency of the input clock according to the following equation:

$$N = [(FIN \times 256)/108] - 1$$

where FIN is in MHz

The 8-bit M register sets the divide-by term for the VCO reference clock feeding back into the phase detector and determines the center frequency of the VCO. The value set in the M register is independent of the input clock frequency. The value of the M register is determined by the following equation:

$$FOUT = [(M+1)/(N+1)] \times FIN$$

DAC OPERATION

The output of each of the four 7-bit DACs is controlled by programming the associated register. In addition, each DAC has a reference input that determines the maximum DAC output. The following equations are used to calculate the DAC outputs:

$$I_{DACF} = IR \times FREG \times 4/128 \text{ mA}$$

$$I_{DACI} = (7.41E - 2 \times IREG)/RR \text{ mA, where RR is in k}\Omega$$

$$V_{DACP} = [2 \times PREG \times (VRP - (VCA - VR3))]/128V$$

$$V_{DACS} = (SREG \times VR3)/128V$$

SERIAL PORT OPERATION

The 32D4666 provides a simple serial port interface that allows programming of the device's internal registers. The write-only serial port is a three-line interface that requires an enable signal (SDEN) along with clock (SCLK) and data (SDATA) signals to program the internal registers of the 32D4666. Data is shifted into the registers in 8-bit bytes that are divided into four bits of address and four bits of data. To load data into the device, the enable pin (SDEN) is asserted for eight clock cycles during which data can be presented on the SDATA input pin. Data on the SDATA pin is clocked into the device on the falling edges of the clock signal provided on the SCLK pin. The falling edge of SDEN latches the data internally and initiates the function selected. To save power the serial port circuitry is powered down when the SDEN line is low. Because of this, there is a minimum set-up and hold time for the SDEN signal (refer to specifications.) Table 1 provides the address-to-function mapping for the internal registers.

TABLE 1: Data Packet Fields (X = Don't care bit)

ADDRESS BITS				REGISTER	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
0	1	0	0	P Register	X	P6	P5	P4
0	1	0	1	P Register	P3	P2	P1	P0
0	1	1	0	I Register	X	I6	I5	I4
0	1	1	1	I Register	I3	I2	I1	I0
1	0	0	0	S Register	X	S6	S5	S4
1	0	0	1	S Register	S3	S2	S1	S0
1	0	1	0	F,C Register	C0	F6	F5	F4
1	0	1	1	F Register	F3	F2	F1	F0
1	1	0	0	M Register	M7	M6	M5	M4
1	1	0	1	M Register	M3	M2	M1	M0
1	1	1	0	N Register	X	N6	N5	N4
1	1	1	1	N Register	N3	N2	N1	N0

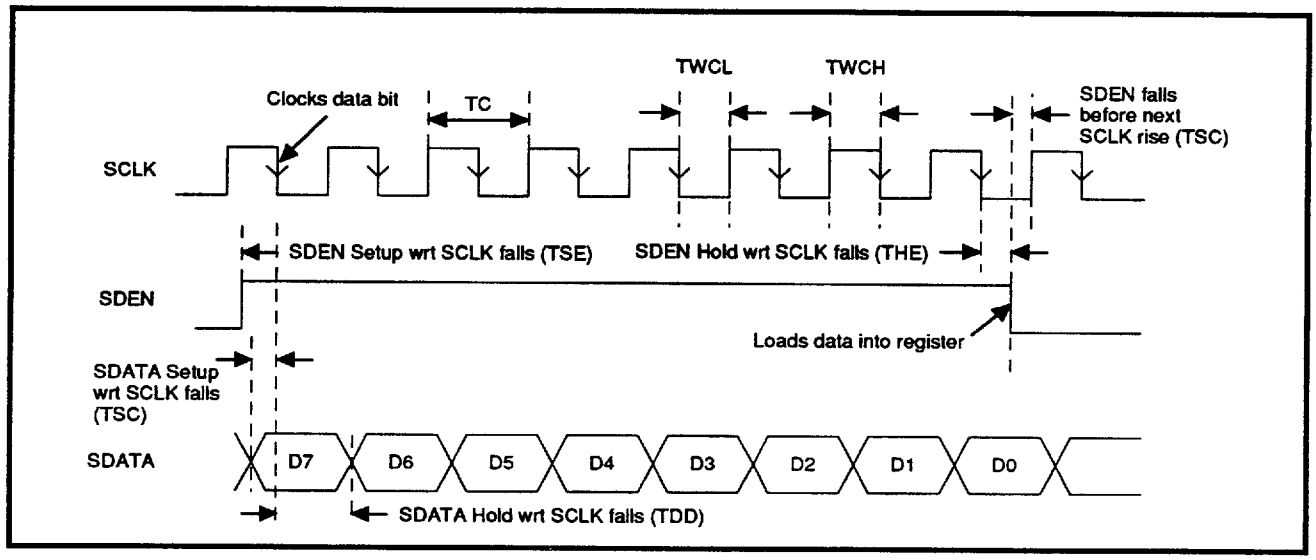


FIGURE 1: Serial Port Timing Relationship

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
FOEN	I	This is a TTL compatible input that disables the output buffer of the FOUT pin with a TTL low signal. This function is used to reduce jitter when the reference output is not required.
FREF/$\overline{\text{FREF}}$	I	Reference clock inputs. An 8 to 20 MHz differential PECL reference clock is applied to these input pins. This serves as the reference for the internal PLL.
SDATA	I	Serial port input data. Data input for an 8-bit internal shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four bits are the data value. For loading data into both registers of a DAC or the M and N counters, it is suggested that the registers be loaded with a minimum delay between packets to reduce the output transients.
SCLK	I	Serial Data Clock. Serial data is clocked into the internal shift register on the falling edge of this input.
SDEN	I	Serial Data Enable. A high level TTL input on this pin will enable the clocking of the internal shift register. The data in the shift register is latched on the falling edge of SDEN.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
DACF	O	Current DAC output. The output of this 7-bit current DAC is determined by the contents of the F register and the current applied to the IR pin.
DACI	O	Current DAC output. The output of this 7-bit current DAC is determined by the contents of the I register and the resistor across the VR1/VR2 pins.
DACP	O	Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the P register, and voltage at VR3 and VRP.
DACS	O	Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the S register, and voltage at VR3.
FCO	O	Filter Control Output. This is a latched TTL output that can be used to switch an external FET for changing the components of the data separator loop filter. When C0 is set to TTL high ("1") in the F register, the FCO output will be high.
FOUT/$\overline{\text{FOUT}}$	O	Frequency Output. A differential PECL frequency reference output that is determined by the M and N registers and the FREF/$\overline{\text{FREF}}$ input frequency where FOUT = [(μ + 1) / (N + 1)] FIN. This output should be AC coupled into the reference input of the data separator device.

ANALOG PINS

FLTR	–	PLL loop filter. An RC filter is connected to this pin to control the VCO voltage.
VR1/VR2	–	Current setting resistor. A resistor is connected between these pins to set the current reference for DACI.
AGND	–	Analog ground pin.
DGND	–	Digital ground pin.
VCA, B	–	+5V analog power supply pins.
VCD	–	+5V digital power supply pin.
IR	–	Reference Current Input. The current applied to this pin provides the reference for DACF.
VR3	–	Reference Input Voltage. The voltage applied to this pin establishes the reference for DACS.
VRP	–	Reference Input Voltage. The voltage applied to this pin establishes the reference for DACP.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.65V < POSITIVE SUPPLY VOLTAGE < 5.25V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature, Tj	+150°C
Positive Supply Voltage (VCA, VCB, VCD)	-0.5V to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp+0.5V

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage (VCA, VCB, VCD)	4.65V to 5.25V
Junction Operating Temperature, Tj	0 ≤ Tj ≤ 130°C
Ambient Temperature, Ta	0 ≤ Ta ≤ 70°C

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC (VCA, B, D)	Outputs and test point pins open		77	110	mA
Pd Power Dissipation	Outputs and test point pins open		385	578	mW

TTL COMPATIBLE INPUTS

Input low voltage	VIL				0.8	V
Input high voltage	VIH		2.0			V
Input low current	IIL	VIL= 0.4V			-1.5	mA
Input high current	IIH	VIH = 2.7V			20	µA

TTL COMPATIBLE OUTPUTS

Output low voltage	VOL	IOL = 2.0 mA			0.5	V
Output high voltage	VOH	IOH = -400 µA	2.4			V

PECL OUTPUT LEVELS (FOUT/$\overline{\text{FOUT}}$)

Output high level		VCA = 5.0V	VCA-1.02			V
Output low level		VCA = 5.0V			VCA-1.45	V
Single-ended output voltage swing		VCA = 5.0V	0.75		0.95	V
Output current	IFOUT		-4.0		+4.0	mA

PECL INPUT LEVELS (FREF/$\overline{FREF}$)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input high level	VFIH	VCA = 5.0 V	VFIL - 0.5		VCA - 0.5	V
Input high current	IFIH				100	µA
Input low level	VFIL	VCA = 5.0 V	VCA - 2.2		VFIH - 0.5	V
Input low current	IFIL		-100			µA
Differential input		VCA = 5.0 V	0.5			V

FREQUENCY REFERENCE OUTPUT

Unless otherwise specified, FOUT = 30 MHz; loop filter components are C1 = 3300 pF, C2 = 270 pF, R1 = 4.12 kΩ; 4.65V ≤ VCn ≤ 5.25V; 0 ≤ Ta ≤ 70°C.

Reference frequency	FIN		8		20	MHz
Output frequency	FOUT				108	MHz
Output jitter	JFO				1% x TVCO	ps(RMS)
Output duty cycle	DFO	50% amplitude, FOUT = 108 MHz	42		58	%
M counter value			80		255	
N counter value			18		127	
RR resistor value			4.5		5.25	kΩ
VCO center frequency	TVCO	TVCO = (4.01 E-10) (RR/M) + 2.4 E-9; VCA = 5.0V, RR = 4.75 kΩ, FLTR = 2.7V, M = 100, FIN = 20 MHz	0.77 TVCO		1.23 TVCO	ns
VCO dynamic range		1V < FLTR < VCA - 0.5 FOUT = 108 MHz, VCA = 5.0V	±25		±45	%
VCO control gain	KVCO	ωi = 2π/TVCO	0.14 ωi		0.26 ωi	rad/s V
Phase detector gain	KD	K_D = (4.39E - 3) x M/RR		K_D		A/rad

CONTROL DACS

Differential linearity (monotonicity)		DACF, I, P, S 0 ≤ Ta ≤ 70°C 4.75V ≤ VCA ≤ 5.25V	-1LSB			
DACF output current	IOF	VCA = 5.0V IOF = (F x 4 x IR)/128 Rx = 2.74 kΩ IR = VR3/(4 x Rx)	0.97 IOF -3/4 LSB		1.04 IOF +3/4 LSB	A

CONTROL DACS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Rx resistor value		2.5		3.0	kΩ
DACI output accuracy	VCA = 5.0V IOI = (7.421E - 2) x I/RR RR = 4.75 kΩ	0.95 x IOI -3/4 LSB		1.05 x IOI +3/4 LSB	A
DACI/F voltage compliance				2	V
DACP output voltage VOP	VCA = 5.0V VOP = 2 x P x [VRP - (VCA - VR3)]/128 RR = 4.75 kΩ VR3 = 2.2V VRP = 3.6V	0.97V -3/4 LSB -25 mV		1.04V +3/4 LSB +25 mV	V
DACP output range		VCA- VR3		VCA- 0.9	V
DACP output resistance		50		200	Ω
VRP input voltage		(VCA -VR3) + 0.2		VCA -1.0	V
VRP input current	2.0V ≤ VRP ≤ VCA			20	µA
DACS output voltage VOS	VCA = 5.0V VOS = (5REG x VR3)/128	0.97 x VOS -3/4 LSB -15 mV		1.03 x VOS +3/4 LSB +60 mV	V
DACS output range		0.1		2.4	V
DACS output resistance				3.7	kΩ
VR3 input voltage		2.0		2.4	V
VR3 input current	VR3 = 2.2V			1.0	mA

SERIAL PORT TIMING

SCLK period TC		100			ns
SDEN Setup wrt first SCLK falls TSE		10		TC/2 - 10	ns
SDEN Hold wrt last SCLK falls THE		10		TC/4	ns
SDEN Falls wrt next SCLK rise TSC		25			ns
SDATA Setup/Hold wrt SCLK falls TDD		25			ns
SCLK Negative pulse width TWCL		25		TC - 25	ns
SCL Positive pulse width TWCH		25		TC - 25	ns

APPLICATIONS INFORMATION

The serial port allows the user to program the internal registers of the 32D4666 device. This port has been designed to operate with the serial port on most microcontrollers such as the 8051. Silicon Systems also provides a serial port board that can be used to operate the serial interface. The serial port consists of three lines: enable (SDEN or SERMODE), data (SDATA), and clock (SCLK). During a serial data transfer, eight bits of data should be transferred to the selected device. The first four bits of data contain register address information while the last four bits contain the programming data. The timing considerations for the serial port are fairly straight forward (see Figure 2). The enable line is driven high to initiate the data transfer. While the enable line is high, the transmitting device should output eight clock pulses along with eight bits of synchronous programming data, four address bits followed by four data bits. The data is shifted internally on the falling edge of the clock pulses. To prevent false data from being latched in, only eight (8) clock pulses should be provided while the enable line is active. The falling edge of the enable input will latch the data into the internal registers and initiate the selected function.

Note: it takes two transfers to load a single register.

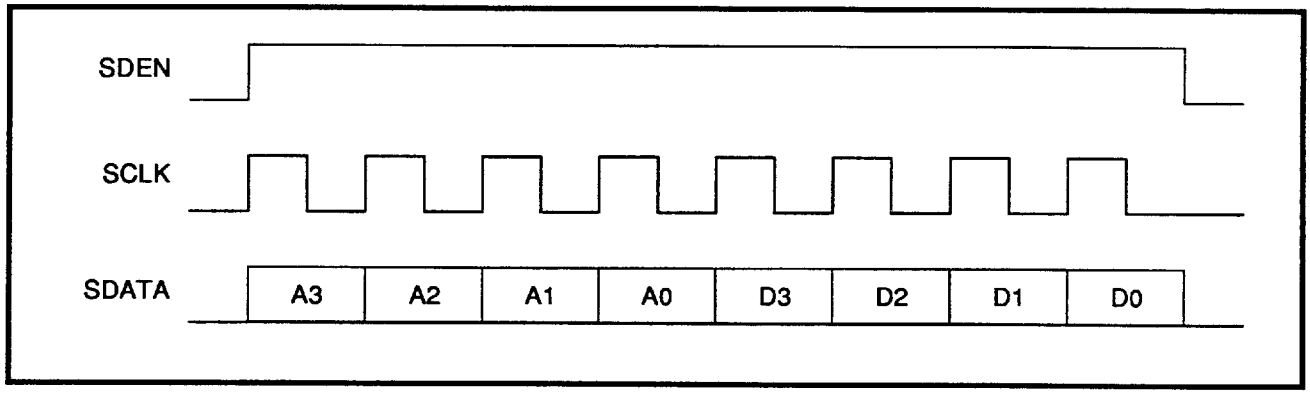


FIGURE 2: Serial Port Timing

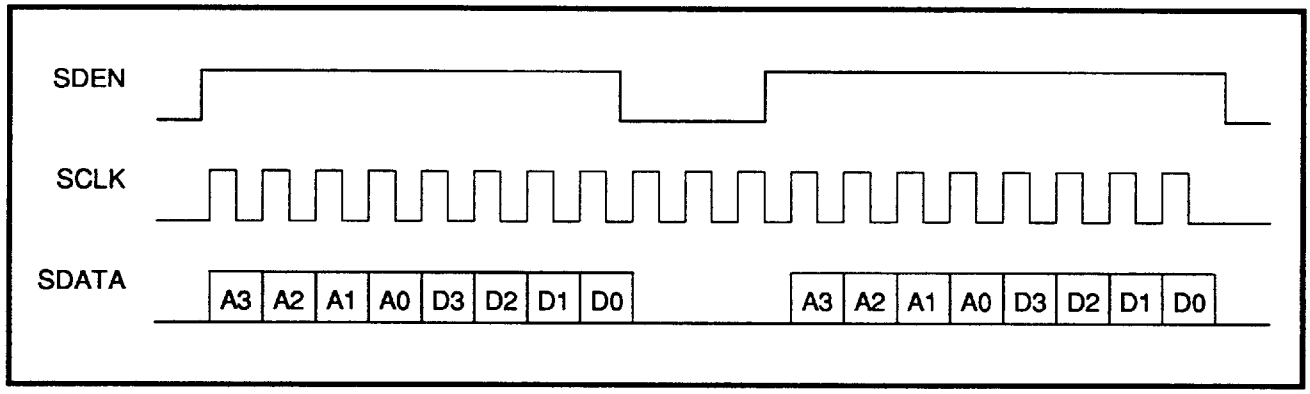


FIGURE 3: Serial Port Timing, Multiple Transfers

APPLICATIONS INFORMATION (continued)

REFERENCE FREQUENCY OUTPUT:

The 32D4666 provides the reference frequency for the phase-locked loop (PLL) of a data separator. The required frequency is programmed using the **M** and **N** registers of the 32D4666.

The value of the **N** register is determined by the oscillator that drives the 32D4666 according to the following equation:

$$N=\frac{(Fin \bullet 256)}{(108\ MHz)}-1$$

For this application, using a 20 MHz oscillator (Fin) would yield an **N** integer value of 46. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 45 to 47. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \bullet Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 3x reference clock), at 26 Mbit/s the required reference frequency is 78 MHz and using a value of **N** = 47, yields an **M** value of 186. At 28 Mbit/s using the **N** value of 49 would require an **M** value of 209 to produce an output frequency of 84 MHz. **M** and **N** values for some sample data rates are provided in the table that follows. Note: the values for Fout are approximate.

TABLE 2: M and N Register Programming Example

DR (Mbit/s)	Fout	M	N
26 Mb/s	78 MHz	186	47
28 Mb/s	84 MHz	192	45
30 Mb/s	90 MHz	206	45
32 Mb/s	96 MHz	220	45

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

TABLE 3: Frequency Programming Information, N Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	0	X	0	1	0	N Register MSBs for N = 47
1	1	1	1	1	1	1	1	N Register LSBs for N = 47
1	1	1	0	X	0	1	0	N Register MSBs for N = 45
1	1	1	1	1	1	0	1	N Register LSBs for N = 45

The **M** register is at address "1100" for the MSBs and at address "1101" for the LSBs. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

TABLE 4: Frequency Programming Information, M Register

ADDRESS BITS				DATA BITS				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	0	1	0	1	1	M Register = 186,
1	1	0	1	1	0	1	0	Fout = 78 MHz
1	1	0	0	1	1	0	0	M Register = 192,
1	1	0	1	0	0	0	0	Fout = 84 MHz
1	1	0	0	1	1	0	0	M Register = 206,
1	1	0	1	1	1	1	0	Fout = 90 MHz
1	1	0	0	1	1	0	1	M Register = 220,
1	1	0	1	1	1	0	0	Fout = 96 MHz

LOOP FILTER FOR THE 32D4666:

The 32D4666 requires a loop filter to control the PLL locking characteristics. While there are several types of filters that can be used to perform this function, a simple integrating filter has proven to be very effective (see Figure 4). To select the components for the loop filter, two considerations should be made. First, the acquisition time of the loop must be less than the minimum track-to-track seek time and second, the capacitor C1 should be low leakage (C1 < 1.0 μF). The acquisition time of the loop is set-up to accommodate a zero phase restart and allow for 1% maximum phase error after phase acquisition. This yields a settling time of: $t_s = 5/\omega_n$.

Suppose FREF = 12 MHz, FOUT = 100 MHz, M = 232, N = 27

KVCO = (0.21)(2π)(FOUT) rad/s V (typ.), at 100 MHz, $\underline{KVCO = 1.33 \times 10^8}$ rad/s V

KD = (4.39 E-3)M/RR A/rad @ RR = 4750Ω, $\underline{KD = 2.14 \times 10^{-4}}$ A/rad

For a second order system,

$R1 = (2 \times \zeta \times \omega_n)/\left(\frac{KVCO \times KD}{M+1}\right)$ where ζ is the damping factor.

$C1 = \left(\frac{KVCO \times KD}{M+1}\right)/(\omega_n^2)$ and C1/10 > C2 > C1/20

A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

If we start with $\omega_n = 2 \times 10^4$, C1 can be calculated as 0.3 µF and C2 can be calculated as 0.015 to 0.03 µF. As mentioned above, the damping factor at the maximum frequency of 100 MHz should be 1.0, so R1 is calculated as:

$$R1 = (2 \times 1.0 \times 2E4)/\left(\frac{1.33E8 \times 2.14E\text{-}4}{233}\right) = 328\Omega$$

These values will produce a loop settling time t_s of $5/2 \times 10^4 = 250$ µs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.

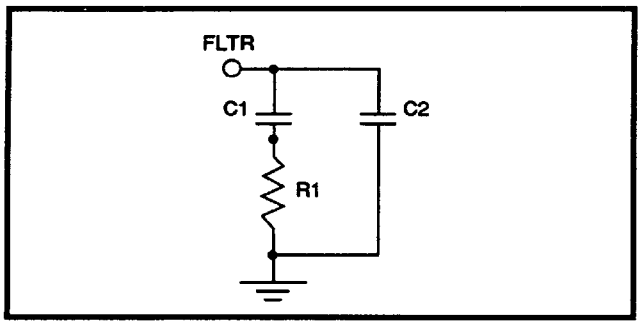


FIGURE 4: Integrating Filter for the Phase Locked Loop

NOTE: For further information on the loop filter, consult the Data Synchronizer Family Application Notes.

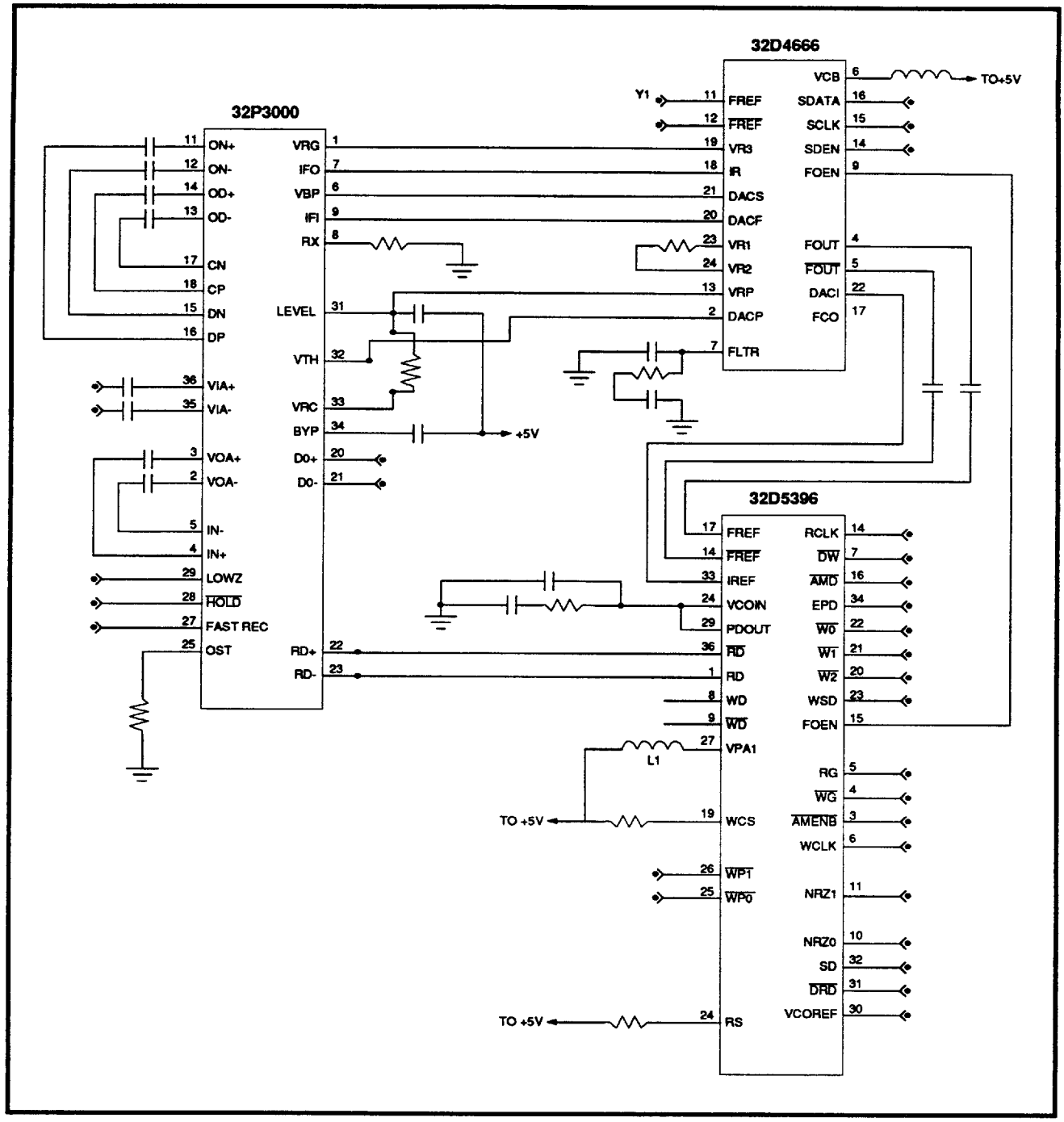


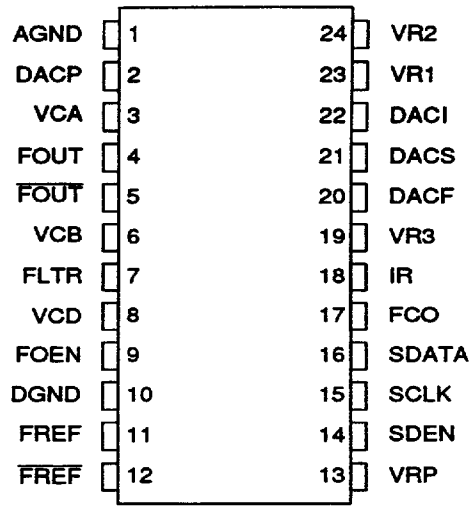
FIGURE 5: Typical 32D4666 Application

SSI 32D4666
Time Base Generator

PACKAGE PIN DESIGNATIONS
(Top View)

Thermal Characteristics: θjA

24-Lead SOL	80°C/W
24-Lead VSOP	110°C/W



24-Lead SOL/VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32D4666	24-Lead SOL	32D4666-CL	32D4666-CL
	24-Lead VSOP	32D4666-CV	32D4666-CV

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