

## Advanced Power MOSFET

## SSF4N80AS

### FEATURES

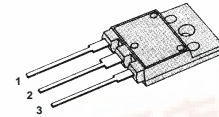
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25  $\mu$ A (Max.) @  $V_{DS} = 800V$
- Low  $R_{DS(ON)}$  : 2.450  $\Omega$  (Typ.)c

$$BV_{DSS} = 800 V$$

$$R_{DS(on)} = 3.0 \Omega$$

$$I_D = 3.5 A$$

#### TO-3PF



1.Gate 2. Drain 3. Source

### Absolute Maximum Ratings

| Symbol         | Characteristic  | Value        | Units      |
|----------------|---|--------------|------------|
| $V_{DSS}$      | Drain-to-Source Voltage   | 800          | V          |
| $I_D$          | Continuous Drain Current ( $T_C=25^\circ C$ )                           | 3.5          | A          |
|                | Continuous Drain Current ( $T_C=100^\circ C$ )                          | 2.2          |            |
| $I_{DM}$       | Drain Current-Pulsed ①  | 18           | A          |
| $V_{GS}$       | Gate-to-Source Voltage  | $\pm 30$     | V          |
| $E_{AS}$       | Single Pulsed Avalanche Energy ②  | 327          | mJ         |
| $I_{AR}$       | Avalanche Current ①   | 3.5          | A          |
| $E_{AR}$       | Repetitive Avalanche Energy ①   | 8.5          | mJ         |
| dv/dt          | Peak Diode Recovery dv/dt ③   | 2.0          | V/ns       |
| $P_D$          | Total Power Dissipation ( $T_C=25^\circ C$ )                            | 85           | W          |
|                | Linear Derating Factor  | 0.68         |            |
| $T_J, T_{STG}$ | Operating Junction and Storage Temperature Range                        | - 55 to +150 | $^\circ C$ |
| $T_L$          | Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds | 300          |            |

### Thermal Resistance

| Symbol          | Characteristic      | Typ. | Max. | Units        |
|-----------------|---------------------|------|------|--------------|
| $R_{\theta JC}$ | Junction-to-Case    | --   | 1.47 | $^\circ C/W$ |
| $R_{\theta JA}$ | Junction-to-Ambient | --   | 40   |              |

Rev. B

# SSF4N80AS

## N-CHANNEL POWER MOSFET

### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise specified)

| Symbol              | Characteristic                          | Min. | Typ. | Max. | Units | Test Condition  |
|---------------------|---|------|------|------|-------|---|
| BV <sub>DSS</sub>   | Drain-Source Breakdown Voltage          | 800  | --   | --   | V     | V <sub>GS</sub> =0V, I <sub>D</sub> =250μA  |
| ΔBV/ΔT <sub>J</sub> | Breakdown Voltage Temp. Coeff.          | --   | 0.96 | --   | V/°C  | I <sub>D</sub> =250μA <b>See Fig 7</b>  |
| V <sub>GS(th)</sub> | Gate Threshold Voltage                  | 2.0  | --   | 3.5  | V     | V <sub>DS</sub> =5V, I <sub>D</sub> =250μA  |
| I <sub>GSS</sub>    | Gate-Source Leakage, Forward            | --   | --   | 100  | nA    | V <sub>GS</sub> =30V  |
|                     | Gate-Source Leakage, Reverse            | --   | --   | -100 |       | V <sub>GS</sub> =-30V   |
| I <sub>DSS</sub>    | Drain-to-Source Leakage Current         | --   | --   | 25   | μA    | V <sub>DS</sub> =800V   |
|                     |   | --   | --   | 250  |       | V <sub>DS</sub> =640V, T <sub>C</sub> =125°C  |
| R <sub>DS(on)</sub> | Static Drain-Source On-State Resistance | --   | --   | 3.0  | Ω     | V <sub>GS</sub> =10V, I <sub>D</sub> =0.85A ④*  |
| g <sub>fs</sub>     | Forward Transconductance                | --   | 3.1  | --   | Ω     | V <sub>DS</sub> =50V, I <sub>D</sub> =0.85A ④   |
| C <sub>iss</sub>    | Input Capacitance                       | --   | 880  | 1140 | pF    | V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz<br><b>See Fig 5</b>                                   |
| C <sub>oss</sub>    | Output Capacitance                      | --   | 90   | 105  |       |   |
| C <sub>rss</sub>    | Reverse Transfer Capacitance            | --   | 35   | 42   |       |   |
| t <sub>d(on)</sub>  | Turn-On Delay Time                      | --   | 19   | 50   | ns    | V <sub>DD</sub> =400V, I <sub>D</sub> =2A,<br>R <sub>G</sub> =16 Ω<br><b>See Fig 13</b> ④ ⑤             |
| t <sub>r</sub>      | Rise Time                               | --   | 32   | 75   |       |   |
| t <sub>d(off)</sub> | Turn-Off Delay Time                     | --   | 67   | 145  |       |   |
| t <sub>f</sub>      | Fall Time                               | --   | 32   | 75   |       |   |
| Q <sub>g</sub>      | Total Gate Charge                       | --   | 40   | 52   | nC    | V <sub>DS</sub> =640V, V <sub>GS</sub> =10V,<br>I <sub>D</sub> =2A<br><b>See Fig 6 &amp; Fig 12</b> ④ ⑤ |
| Q <sub>gs</sub>     | Gate-Source Charge                      | --   | 7.3  | --   |       |   |
| Q <sub>gd</sub>     | Gate-Drain("Miller") Charge             | --   | 18.1 | --   |       |   |

### Source-Drain Diode Ratings and Characteristics

| Symbol          | Characteristic            | Min. | Typ. | Max. | Units | Test Condition   |
|-----------------|---------------------------|------|------|------|-------|--|
| I <sub>S</sub>  | Continuous Source Current | --   | --   | 3.5  | A     | Integral reverse pn-diode in the MOSFET                          |
| I <sub>SM</sub> | Pulsed-Source Current ①   | --   | --   | 18   |       |  |
| V <sub>SD</sub> | Diode Forward Voltage ④   | --   | --   | 1.4  | V     | T <sub>J</sub> =25 °C, I <sub>S</sub> =3.5A, V <sub>GS</sub> =0V |
| t <sub>rr</sub> | Reverse Recovery Time     | --   | 430  | --   | ns    | T <sub>J</sub> =25 °C, I <sub>F</sub> =4.5A                      |
| Q <sub>rr</sub> | Reverse Recovery Charge   | --   | 4.06 | --   | μC    | di <sub>F</sub> /dt=100A/μs ④                                    |

#### Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=50mH, I<sub>AS</sub>=3.5A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω, Starting T<sub>J</sub>=25 °C
- ③ I<sub>SD</sub>≤4.5A, di/dt ≤120A/μs, V<sub>DD</sub>≤BV<sub>DSS</sub>, Starting T<sub>J</sub>=25 °C
- ④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

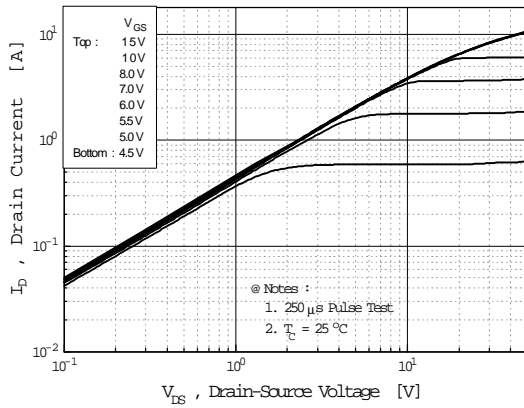


Fig 2. Transfer Characteristics

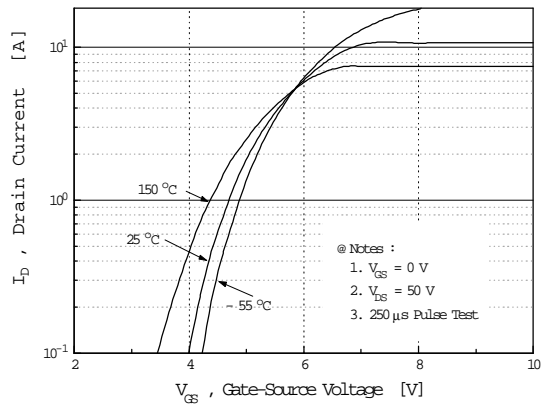


Fig 3. On-Resistance vs. Drain Current

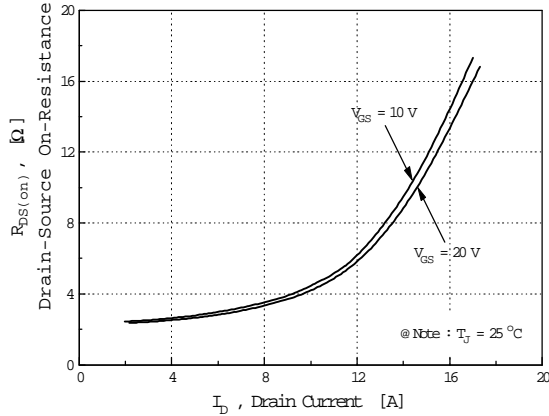


Fig 4. Source-Drain Diode Forward Voltage

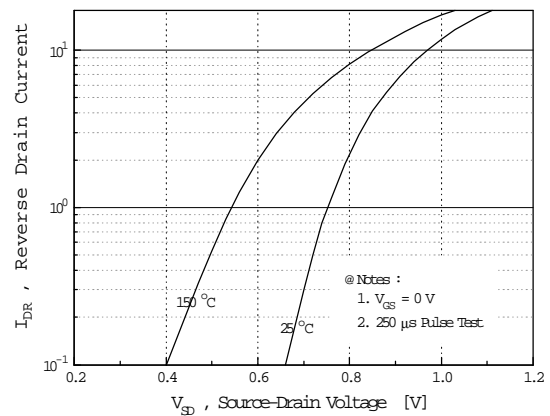


Fig 5. Capacitance vs. Drain-Source Voltage

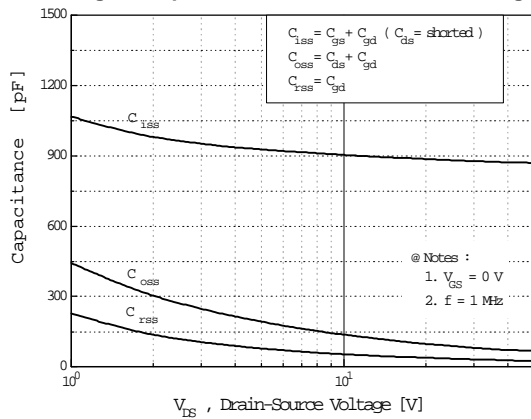
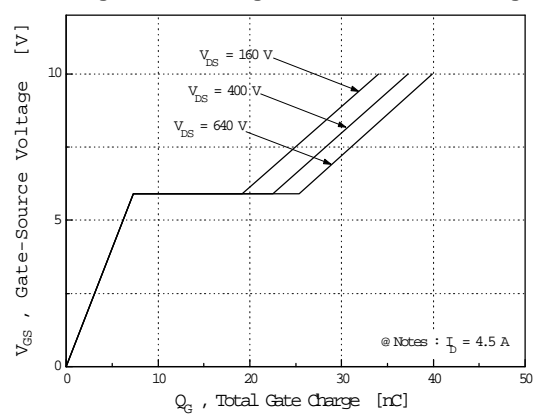
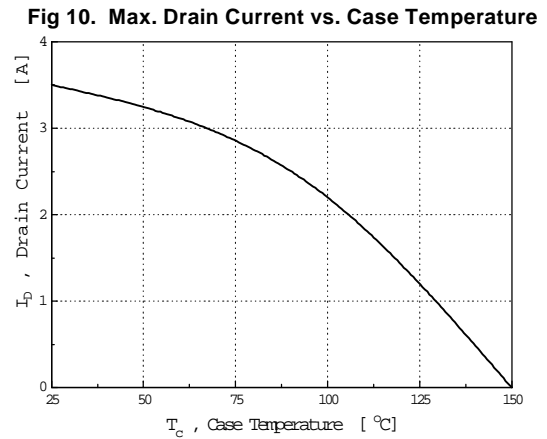
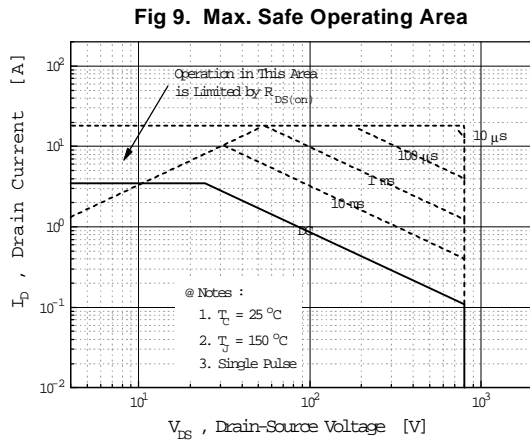
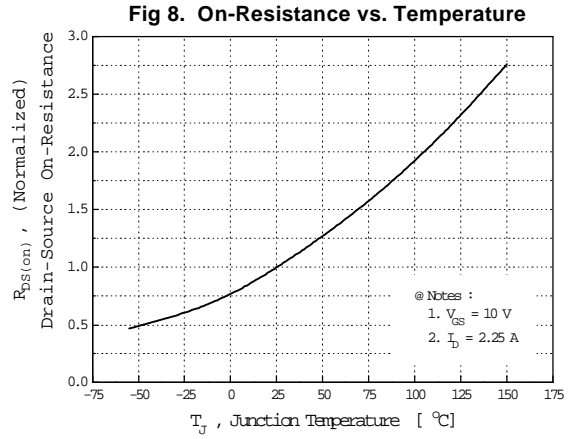
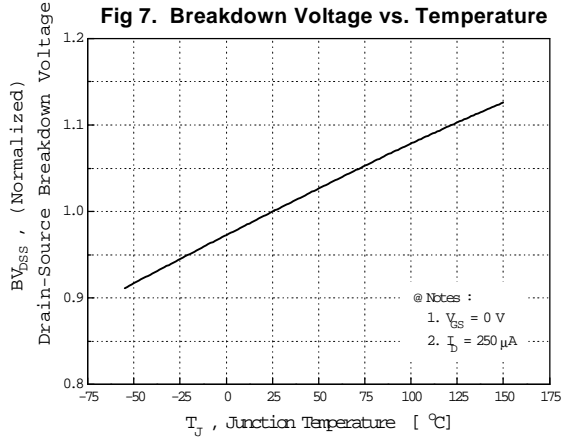


Fig 6. Gate Charge vs. Gate-Source Voltage



# SSF4N80AS

## N-CHANNEL POWER MOSFET



**Fig 11. Thermal Response**

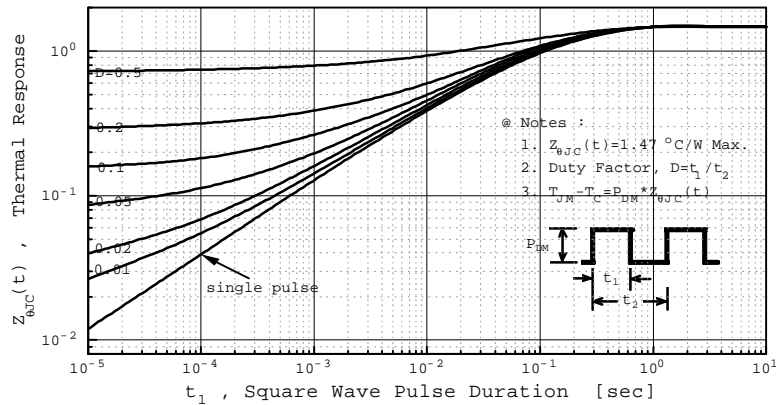


Fig 12. Gate Charge Test Circuit & Waveform

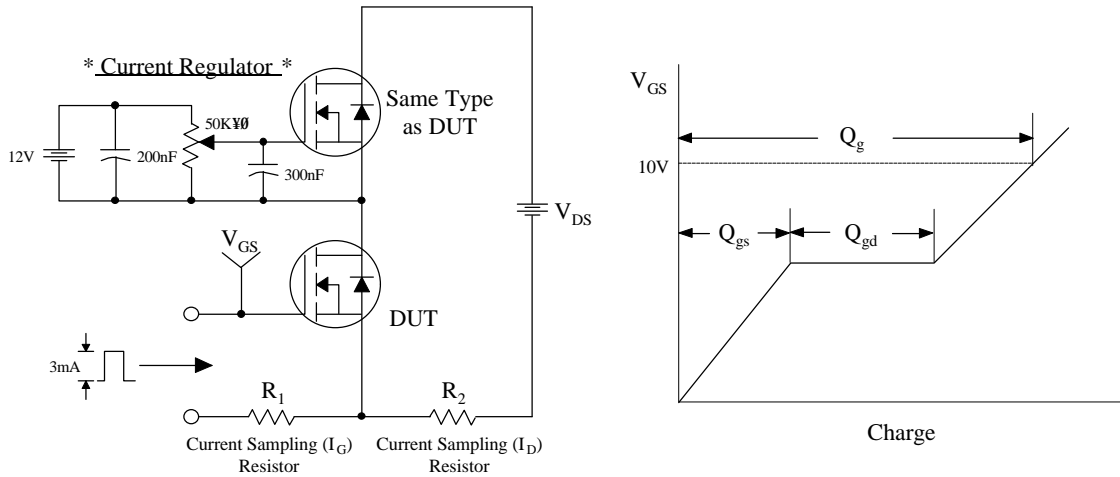


Fig 13. Resistive Switching Test Circuit & Waveforms

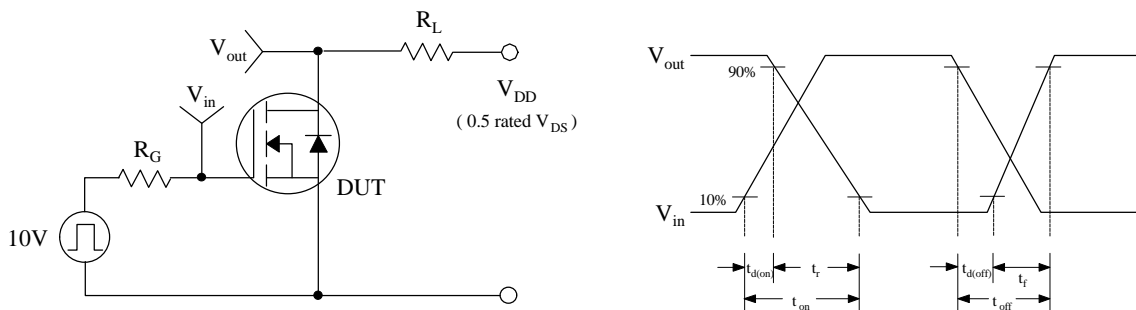


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

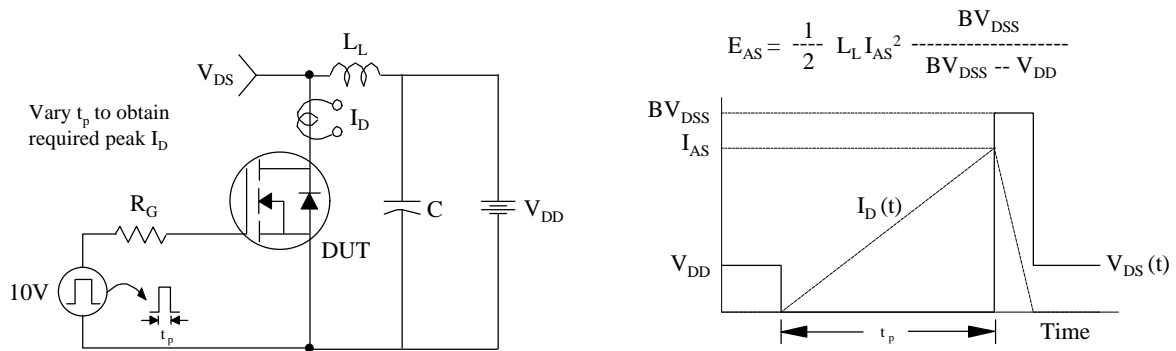
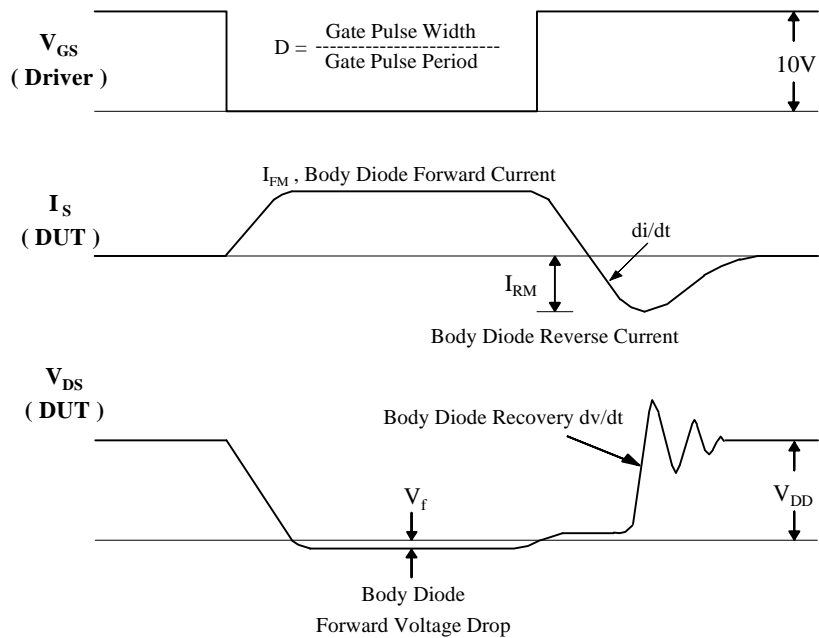
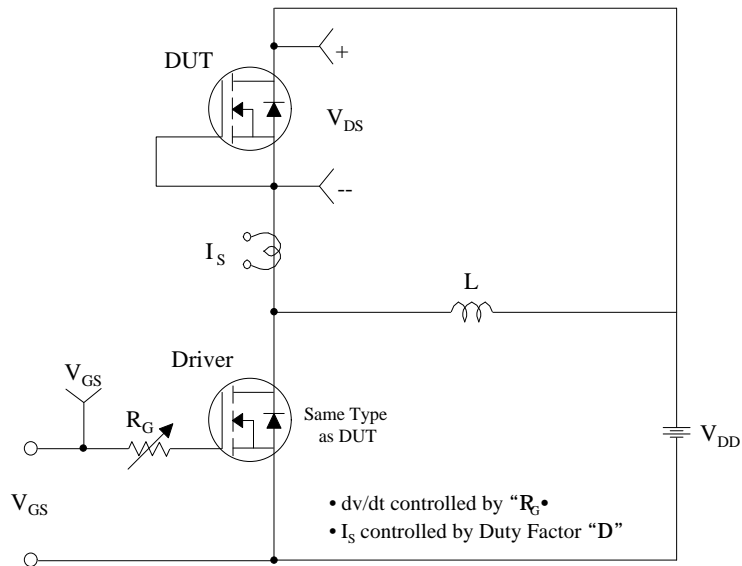


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

|                      |               |      |
|----------------------|---------------|------|
| ACE <sup>x</sup> ™   | ISOPLANAR™    | UHC™ |
| CoolFET™             | MICROWIRE™    | VCX™ |
| CROSSVOLT™           | POP™          |      |
| E <sup>2</sup> CMOS™ | PowerTrench™  |      |
| FACT™                | QS™           |      |
| FACT Quiet Series™   | Quiet Series™ |      |
| FAST®                | SuperSOT™-3   |      |
| FAST <sub>r</sub> ™  | SuperSOT™-6   |      |
| GTO™                 | SuperSOT™-8   |      |
| HiSeC™               | TinyLogic™    |      |

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status         | Definition  |
|--------------------------|------------------------|---|
| Advance Information      | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.  |
| Preliminary              | First Production       | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production        | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.   |
| Obsolete                 | Not In Production      | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.   |