查询SSC2060供应商 捷多邦，专业PCB打样工厂，24小时加急出货

SSC2000 Series

T-42-11-09

CMOS LOW VOLTAGE STANDARD CELL

- **Low Voltage Operation at 0.9 V min.**
- **Built–in Level Shift Circuit**
- **Up to 11,000 gates**

■ DESCRIPTION

The SSC2000 Series CMOS standard cell, to which low-threshold manufacturing process is applied, enables low voltage operation. The built-in level shift circuit is very convenient for use in equipment operated by multiple power voltages and portable battery-driven (1.5 or 3V) equipment.

The cell library is functionally compatible with the SLA gate array series and consists of functions and names equivalent to the TTL74 series. It provides 20 models different in scales from 250 gates to 11,000 gates for easy designing of desired systems.

■ FEATURES

- 2.0 CMOS, 2 layer metalization
- Low 0.9V (min) operating voltage
- Output drive
  – 24mA for a single output at 5.0 volts
  – 48 mA for parallel outputs at 5.0 volts
- Built-in level shifter: from 1.5V to 3.0V
  from 3.0V to 5.0V
- Built-in oscillator: 0.9V ~ 6.0V, 32KHz ~ 4MHz
- I/O level = CMOS, TTL
- Ideal for portable equipment
- High speed: tpd (2-input NAND)

Voltage(V)	1.5	3.0
Internal gates (ns) (2 NAND, FO=2, AL=2mm)	8.5	3.0
Input buffer $T_{PLH} = T_{PHL}$ (ns)	12.0	4.0
Output buffers* $T_{PLH} = T_{PHL}$ (ns) C_L = 15pF	40.0	14.0

* Delay times are different with level shifter.

■ PRODUCT CONFIGURATION

Array Member	Usable Gates			Total # of Pads
SSC2000	Min	Avg	Max	
SSC2010	250	300	450	40
SSC2020	350	350	550	44
SSC2030	450	450	650	48
SSC2040	800	800	1100	60
SSC2050	900	900	1300	64
SSC2060	1100	1300	1600	72
SSC2070	1400	1600	2200	80
SSC2080	1700	1900	2300	84
SSC2090	2000	2100	2900	92
SSC2100	2400	2700	3500	100
SSC2110	3200	3600	4400	112
SSC2120	3600	4100	5000	120
SSC2130	4000	4500	5500	124
SSC2140	4600	5000	6200	132
SSC2150	6200	6600	8000	148
SSC2160	7600	7900	9400	160
SSC2170	8600	9200	10900	172
SSC2180	9500	10000	11900	180
SSC2190	10500	10900	12900	188
SSC2200	11000	11400	13400	192

Note: The device fit is only guaranteed for minimum number of usable gates, and to fit the maximum number of usable gates into the

■ ABSOLUTE MAXIMUM RATINGS

(Vss = 0V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	$V_{DD1, 2}$	-0.3 to 7.0	V
Input voltage	V_I	-0.3 to $V_{DD1, 2}$ + 0.3	V
Output voltage	V_O	-0.3 to $V_{DD1, 2}$ + 0.3	V
Storage temperature	T_{stg}	-65 to +150	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage	V_{DD1}	1.5V only	1.35	1.50	1.65	V
	V_{DD2}	3V only (V_{DD1} = 1.5V only)	2.70	3.00	3.30	V
	V_{DD1}	3V only	2.70	3.00	3.30	V
	V_{DD2}	5V only (V_{DD1} = 3.0V only)	4.50	5.00	5.50	V
Allowable operating voltage	$V_{DD1, 2}$		0.90	—	6.00	V
Operating temperature	T_{opr}		0	—	70	°C

■ ELECTRICAL CHARACTERISTICS

(Ta = 0 – 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply current	I_{DD1}	Stationary state, V_{DD1} = 1.5V	—	—	500	nA
	I_{DD1}	Stationary state, V_{DD1} = 3.0V	—	—	1.0	µA
	I_{DD2}	Stationary state, V_{DD2} = 3.0V Per level shift	—	—	90	nA
	I_{DD2}	Stationary state, V_{DD2} = 5.0V Per level shift	—	—	100	nA
High level output voltage	V_{OH}	V_{DD1} = 1.5V, I_{OH} = -0.23mA	1.3	—	—	V
	V_{OH}	$V_{DD1,2}$ = 3.0V, I_{OH} = -0.6mA	2.7	—	—	V
	V_{OH}	V_{DD2} = 5.0V, I_{OH} = -1.2mA	4.6	—	—	V
Low level output voltage	V_{OL}	V_{DD1} = 1.5V, I_{OL} = 0.7mA	—	—	0.2	V
	V_{OL}	$V_{DD1, 2}$ = 3.0V, I_{OL} = 1.7mA	—	—	0.3	V
	V_{OL}	V_{DD2} = 5.0V, I_{OL} = 4.0mA	—	—	0.4	V
High level input voltage	$V_{IH\,1}$	(TTL) V_{DD2} = 5.0V	1.8	—	—	V
	$V_{IH\,2}$	(CMOS) V_{DD1} = 1.5V	1.1	—	—	V
		(CMOS) $V_{DD1, 2}$ = 3.0V	2.0	—	—	V
		(CMOS) V_{DD2} = 5.0V	3.5	—	—	V
Low level input voltage	$V_{IL\,1}$	(TTL) V_{DD2} = 5.0V	—	—	0.6	V
	$V_{IL\,2}$	(CMOS) V_{DD1} = 1.5V	—	—	0.4	V
		(CMOS) $V_{DD1, 2}$ = 3.0V	—	—	1.0	V
		(CMOS) V_{DD2} = 5.0V	—	—	1.5	V
Input leakage current	I_{LI}		–200	—	200	nA

NOTE: I_{DD2} flows from V_{DD2} to the I/O cell using level shift.
V_{DD1} : Voltage applied to MSI inside the chip.
V_{DD2} : External voltage.
$V_{DD2} \geq V_{DD1}$ shall be satisfied

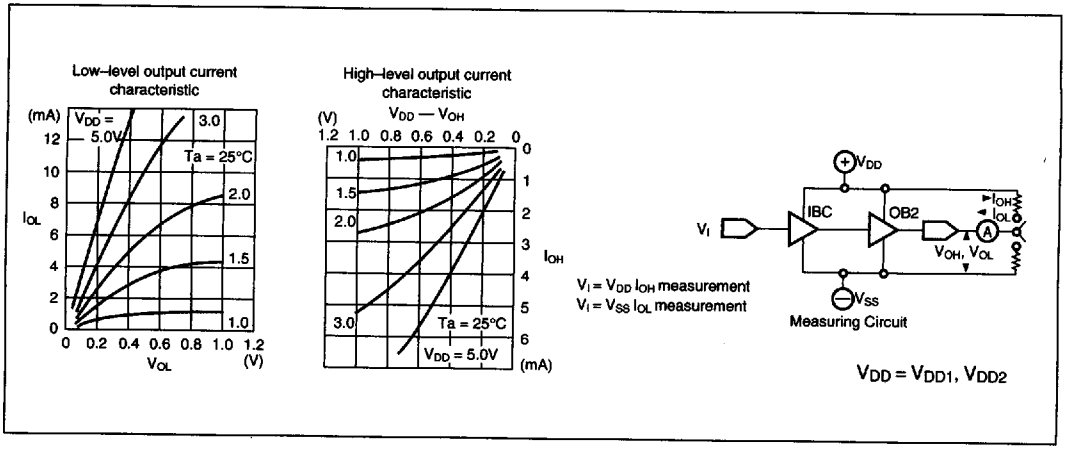
■ PACKAGE MATRIX

Package Type	No. of Pins	Device code	2010	2020	2030	2040	2050	2060	2070	2080	2090	2100	2110	2120	2130	2140	2150	2160	2170	2180	2190	2200
		No. of Pads	40	44	48	60	64	72	80	84	92	100	112	120	124	132	148	160	172	180	188	192
		Gross Gates	400	500	700	1100	1300	1700	2100	2400	2900	3600	4400	5300	5500	6400	8200	9600	11000	12000	13000	14000
Plastic DIP	16	C16	A*		A*	LQ																
	18	C18	A*	A*		Q																
	24	C24	A*	A*	A*	A*	A*	A*	A*	A*	A*	Q										
	28	C28	A*	A*	A*	A*	A*	A*	A*	A*	A*											
	40	C40			A*	A*	A*	A*	A*	A*	A*	A*	A*			Q						
	42	C42			A*	A*	A*	A*	A*	A*	Q	A*	A*			A						
Plastic Shrink DIP	64	S64						A*	A*	A*	L	L										
Plastic QFP	44	F44–4	L										Q									
	44	F44–6	A									A	A	A*		LQ						
	48	F48–12	A	A	A	A	A	A														
	52	F52–6														LQ	LQ					
	60	F60–6									A	A	A									
	60	F60–5				A*	A*	A	A	A	A	A	A	A	A	A	A					
	64	F64–5					A															
	64	F64–6					A	A				A		A		LQ	LQ					
	64	F64–13					A*	A	A			A										
	80	F80–5					A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	LQ				
	80	F80–14						A*	A*	A*	A*	A*	A*	A*	A*	A*	A*					
	100	F100–5								A*	A*	A*	A*	A*	A*	A*	A*				LQ	
	100	F100–15								A*	A*	A	A	A*	A*	A*	A*					
	120	F120–8											A	A*	A*	A*	A*	A			L	L
	128	F128–5											A	A*	A*	A*	A*	A*	A*			
	128	F128–8														A	A				LQ	
	144	F144–8													A*	A*	A*	A*	A*	A*	A*	A*
	160	F160–8														A*	A*	A	A*	A*	L	A*
	184	F184–16																				
	196	F196–9																	A	A*	A*	A*
	208	F208–8																				A
Plastic SOP	14	PSOP5	A																			
	16	PSOP1	A	A	A	A																
	24	PSOP1		A	A																	
	28	SOP2	A*	A*	A*	A*	A*	A*	A*	A												
Plastic TSOP	28	TSOP	L	L	A	A																
PLCC	44	J44		A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	A*								
	68	J68				A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	A*			
	84	J84							A*	A*	A*	A*	A*	A*	A*	A*	A*	A*	A*			Q
Plastic PGA	89	G89									L	L	L	L	L							
Ceramic PGA	64	P64										A	A	A*	A*	A*						
	72	P72																				

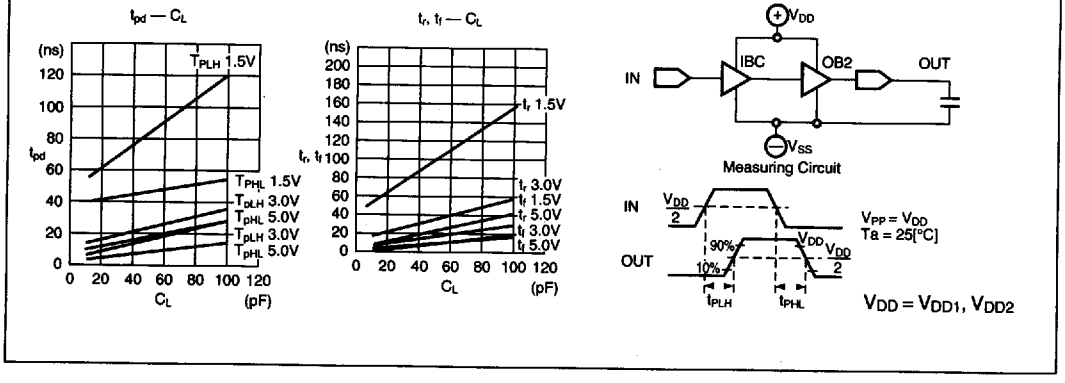
A: Available
*: Pin–Pad table exist
L: Need Lead frame development (2.5 months for new lead frame development)
Q: Need Qualification (reliability test) (2.5 months for reliability test)
LQ: Need Lead frame and Qualification (reliability test)(2.5 months for new lead frame development and/or 2.5 months for reliability test)

■ PERFORMANCE CURVES

● Output Current

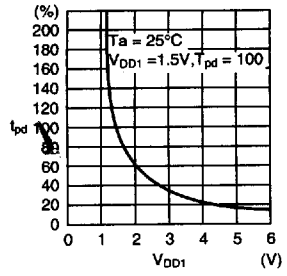


● tpd, tr, tf—C_L

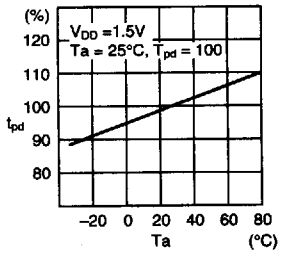


● Propagation time characteristic and power consumption

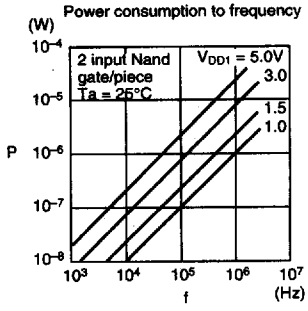
Propagation time to power supply voltage



Propagation time to ambient temperature

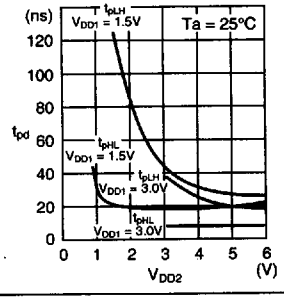


Power consumption to frequency

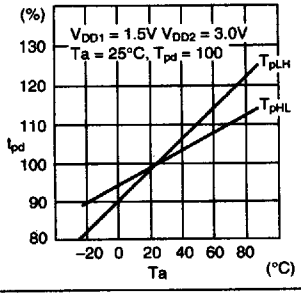


● Level shift circuit propagation time characteristic

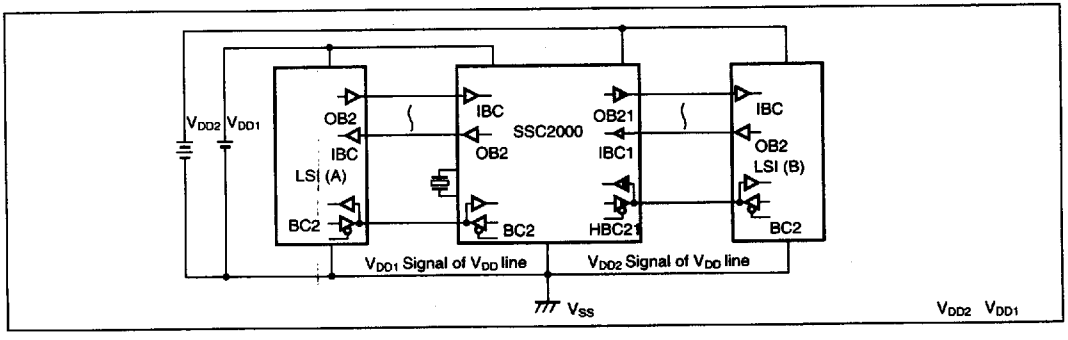
Propagation time to power supply voltage
Level shift circuit



Propagation time to ambient temperature
Level shift circuit



● Example of circuit application



NOTE: Values in the characteristic graphs are shown by value relation on lines.

NOTE: Specifications are subject to change for improvement. The circuits described in this pamphlet are only intended to aid in understanding the product.

We are not responsible for any circuit problems or patent infringements resulting from usage of them.

NOTE: This document contains technology relating to strategic products controlled under the Foreign Exchange and Foreign Trade Control Law of Japan.

This document or a portion thereof should not be exported without obtaining an export license from the ministry of International Trade and industry in accordance with the above law.