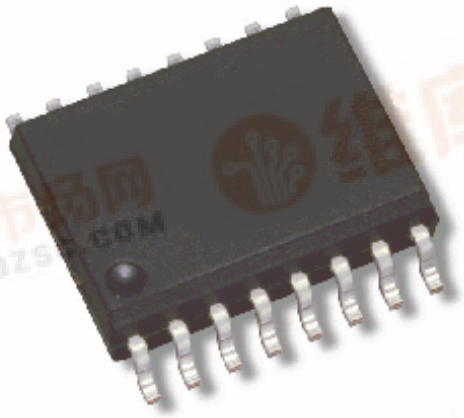
Reliability Qualification Report

STQ-2016Z - Matte Sn, RoHS compliant

Products Qualified by Similarity

STQ-1016Z	SRF-1016Z	SRQ-2116Z
STQ-3016Z	SRF-2016Z	



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I. Qualification Overview

The STQ-2016Z family of products has demonstrated reliable operation by passing all qualification testing in Sirenza Microdevices' product qualification test plan. The STQ-2016Z has been subject to stresses such as humidity (autoclave), extreme hot and cold environments (temperature cycling), moisture sensitivity (MSL-1 and solder reflow testing), and several others as part of the qualification process.

II. Introduction

The Sirenza Microdevices' STQ-2016Z is a direct quadrature modulator targeted for use in a wide range of communications systems, including cellular/PCS, CDMA2000, UMTS, and ISM data com. This device features a wide 700-2500 MHz operating frequency band, excellent carrier and sideband suppression, and a low broadband noise floor.

III. Fabrication Technology

These amplifiers are manufactured using a Silicon Germanium Heterojunction Bipolar Transistor (HBT) technology. This patented self-aligned emitter, double poly HBT process has been in production by our foundry since 1998. The process has been successfully used for a wide range of RFIC products including GSM PAs, DECT front end transceivers, LNAs & VCOs. This process offers comparable performance to GaAs HBTs with the added advantages of mature and highly reproducible Silicon wafer processing.

IV. Package Type

The STQ-2016Z is packaged in a plastic encapsulated TSSOP-16 package that is assembled using a highly reproducible automated assembly process. The die is mounted using an industry standard thermally and electrically conductive silver epoxy. The die is mounted directly to the exposed paddle to provide a low thermal resistance path for heat conduction out of the package.

Figure 1 : Image of TSSOP -16 Exposed Paddle Plastic Package

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V. Qualification Methodology

The Sirenza Microdevices qualification process consists of a series of tests designed to stress various potential failure mechanisms. This testing is performed to ensure that Sirenza Microdevices products are robust against potential failure modes that could arise from the various die and package failure mechanisms stressed. The qualification testing is based on JESD test methods common to the semiconductor industry. The manufacturing test specifications are used as the PASS/FAIL criteria for initial and final DC/RF tests.

VI. Qualification By Similarity

A device can be qualified by similarity to previously qualified products provided that no new potential failure modes/mechanisms are possible in the new design. The following products have been qualified by similarity to STQ-2016Z:

STQ-1016Z STQ-3016Z SRF-1016Z SRF-2016Z SRQ-2116Z

VII. Operational Life Testing

Sirenza Microdevices defines operational life testing as a DC biased elevated temperature test performed at the maximum operational junction temperature limit. For the STQ-2016Z the maximum operational temperature limit is 150°C. The purpose of the operational life test is to statistically show that the product operated at its maximum operational ratings will be reliable by operating several hundred devices for a total time of 1000 hours. The results for this test are expressed in device hours that are calculated by multiplying the total number of devices passing the test by the number of hours tested.

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VIII. Moisture Sensitivity Level - MSL Level 1 Device

STQ-2016Z has successfully completed 168 hours of moisture soak (85ºC/85%RH) followed by three convection reflow cycles with a peak temperature of 270ºC. The successful completion of this test classifies the part as JESD22-A113B Moisture Sensitivity Level 1 (MSL-1). MSL-1 indicates that no special dry pack requirements or time limits from opening of static bag to reflow exist for the STQ-2016Z. MSL-1 is highest level of moisture resistance that a device can be classified according to the above mentioned standard.

IX. Electrostatic Discharge Classification

Sirenza Microdevices classifies Human Body Model (HBM) electrostatic discharge (ESD) according to the JESD22-A114 convention. All pin pair combinations were tested. Each pin pair is stressed at one static voltage level using 1 positive and 1 negative pulse polarity to determine the weakest pin pair combination. The weakest pin pair is tested with 3 devices below and above the failure voltage to classify the part. The Pass/Fail status of a part is determined by the manufacturing test specification. The ESD class quoted indicates that the device passed exposure to a certain voltage, but does not pass the next higher level. The following table indicates the JESD ESD sensitivity classification levels.

Class	Passes	Fails
0	0 V	<250 V
1A	250 V	500 V
1B	500 V	1000 V
1C	1000 V	2000 V
2	2000 V	4000 V

Part Number	HBM ESD Rating
STQ-2016Z	Class 1A
SRQ-2116Z	Class 1A

X. Operational Life Test Results

HTOL Completion Date	Test Duration	Junction Temperature	Quantity	Device-Hours
July 2005	**1000 hours**	**150˚C**	**39**	**39,000**
Dec 2005	**1000 hours**	**150˚C**	**40**	**40,000**

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XI. Qualification Test Results

Group	Test Name	Test Condition/ Standard	Sample Size	Results
B	Preconditioning	MSL1 Reflow @ 270ºC Peak JESD22-A113C	359	Pass
B1a	Temperature Cycling	Air to Air, Soldered on PCB -65ºC to 150ºC 10 min dwell, 1 min transition 1000 cycles JESD22-A104B	6	Pass
B1b	High Temperature Operating Life	T_j = 150°C 1000 hours JESD22-A108B	79	Pass
B1c	HAST	Tamb=110°C, 85%RH Biased, 264 hours JESD22-A110B	15	Pass
B1d	Power Temperature Cycle	-40°C to +85°C Cycled bias (5' on/5'off) 1000 cycles JESD22-A109A	10	Pass
B2	Autoclave	T_{amb}=121°C, 100%RH Un-Biased, 96 hours JESD22-A102C	30	Pass
B3	Temperature Cycle	-65°C to +150°C 10 min dwell, 1 min transition 1000 cycles JESD22-A104B	60	Pass

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XI. Qualification Test Results

Group	Test Name	Test Condition/ Standard	Sample Size	Results
C	Low Temperature Storage	T_{amb}=-40°C 1000 hours	27	Pass
		T_{amb}=-65°C 1000 hours	20	Pass
D	High Temperature Storage	T_{amb}=150°C 1000 hours JESD22-A103B	27	Pass
G	Solderability	Dip & Look Steam Age Condition C Dip Condition A, 215°C JESD22-B102C	30	Pass
		Dip & Look Steam Age Condition C Dip Condition B, 245°C JESD22-B102C	15	
F	Tin Whisker	T_{amb}=60°C, 90%RH 1800 hours NEMI	10	Pass

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XII. Junction Temperature Determination

One key issue in performing qualification testing is to accurately determine the junction temperature of the device. Sirenza Microdevices uses a 3um spot size emissivity corrected infrared camera measurement to resolve the surface temperature of the device at the maximum operational power dissipation. The results are displayed below for the STQ-2016Z device running at operational current of Id= 80mA, a device voltage of 5V, and lead temperature of 85°C.

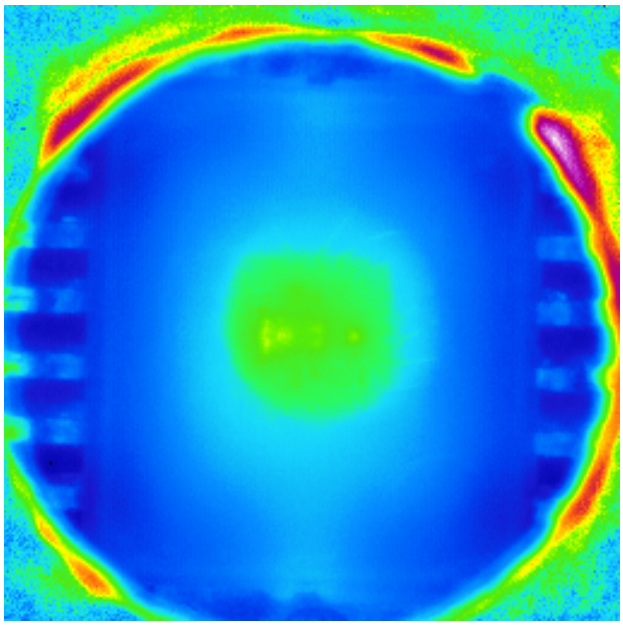

Figure 2: Infrared Thermal Image of STQ-2016Z, Vd = 5.0V, Id =80mA, Tj = 98°C

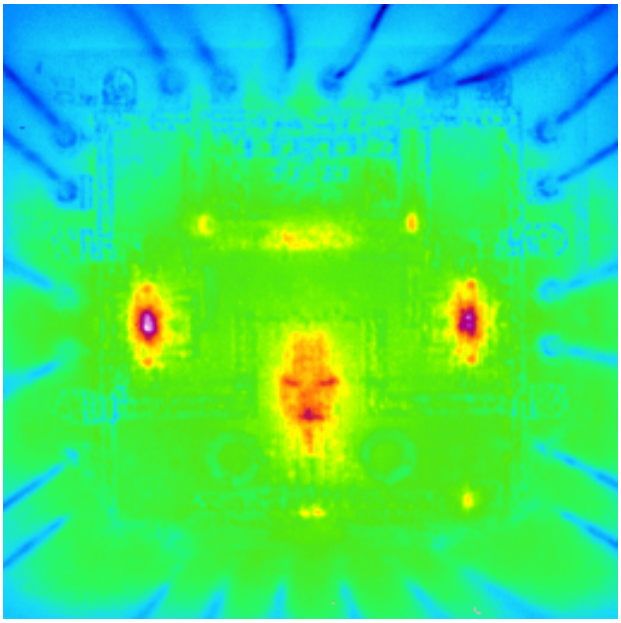

Figure 3: Infrared Thermal Image of SRQ-2116Z, Vd = 5.0V, Id =157mA, Tj = 103.8°C

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XIII. FIT Calculation from Accelerated Life Test Data

The following data demonstrates the results from accelerated life tests performed on the Sirenza 4A SiGe HBT Process. The test was performed on 791 units running at a peak junction temperature up to 195°C. The FIT rate calculation can be found below. The FIT rates were generated assuming 1 failure. In reality, there were no failures, making this a very conservative calculation.

Activation Energy (eV)	0.7
FIT (per 10^9 dev-hours) @ T_j=55°C, 60% CL	0.73

Table 3: Activation Energy and calculated FIT for STQ-2016Z.