

# SRM20100LC<sub>70/85/10</sub>

## CMOS 1M-BIT STATIC RAM

- Low Supply Current
- Access Time 70ns/85ns/100ns
- 131,072 Words × 8-Bit Asynchronous

### DESCRIPTION

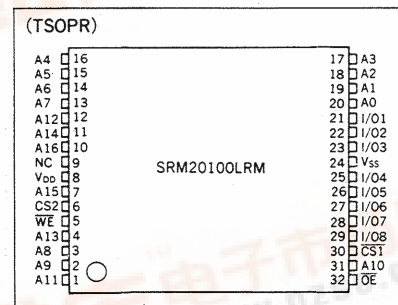
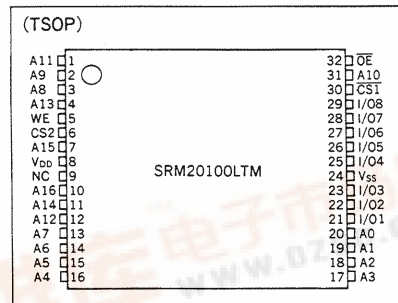
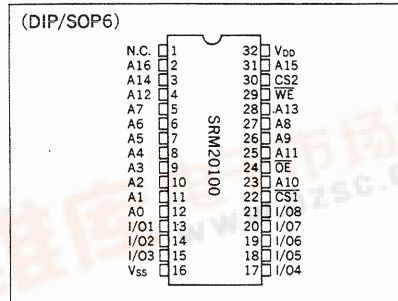
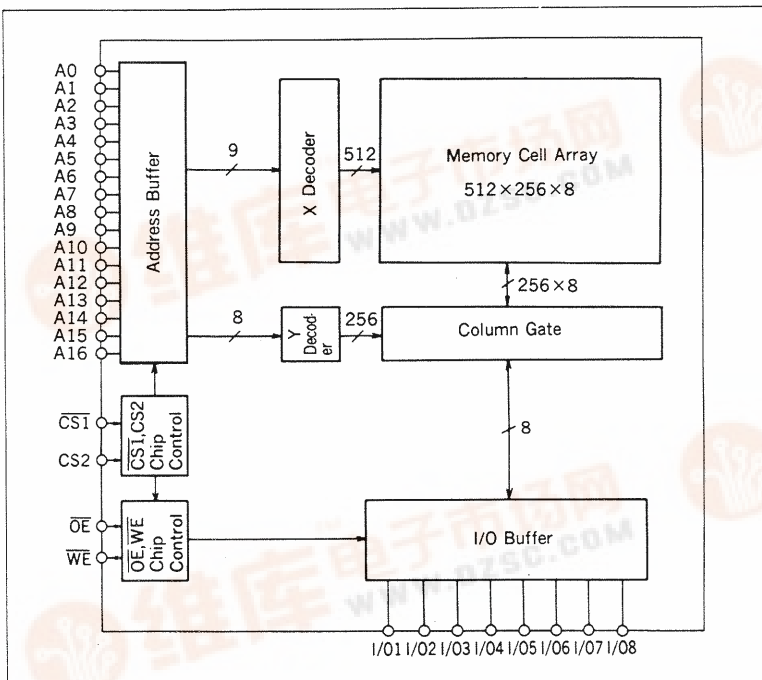
The SRM20100LC<sub>70/85/10</sub> is an 131,072 words × 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

### FEATURES

- Fast Access time..... SRM20100LC<sub>70</sub> 70ns (Max)\*  
SRM20100LC<sub>85</sub> 85ns (Max)  
SRM20100LC<sub>10</sub> 100ns (Max)
- Low supply current..... standby : 2μA (Typ)  
operation: 15mA/MHz (Typ)
- Completely static..... No clock required
- Single power supply..... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package..... SRM20100LC<sub>70/85/10</sub> DIP-32pin (plastic)  
SRM20100LM<sub>70/85/10</sub> SOP6-32pin (plastic)  
SRM20100LTM<sub>70/85/10</sub> TSOP-32pin (plastic)\*  
SRM20100LRM<sub>70/85/10</sub> TSOPR-32pin (plastic)\*

\* : Under development

### BLOCK DIAGRAM



### PIN DESCRIPTION

A0 to A16	Address Input
WE	Write Enable
OE	Output Enable
CS1, CS2	Chip Select
I/O1 to 8	Data I/O
VDD	Power Supply(+5V)
VSS	Power Supply( 0V)
NC	No connection



## ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 7.0	V
Input voltage*	V <sub>I</sub>	-0.5 to 7.0	V
Input/Output voltage*	V <sub>I/O</sub>	-0.5 to V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to 70	°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temperature and time	T <sub>sol</sub>	260°C, 10s (at lead)	—

\* V<sub>I</sub>, V<sub>I/O</sub> (Min) = -3.0V (Pulse width is 50ns)

## ■ DC RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>	—	4.5	5.0	5.5	V
	V <sub>SS</sub>	—	0	0	0	V
Input voltage	V <sub>IH</sub>	—	2.2	3.5	V <sub>DD</sub> + 0.3	V
	V <sub>IL</sub>	—	-0.3*	0	0.8	V

\* If pulse width is less than 50ns, it is -3.0V

## ■ ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

### ● DC Electrical Characteristics

Parameter	Symbol	Conditions	SRM20100LC70			SRM20100LC85			SRM20100LC10			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I <sub>LI</sub>	V <sub>I</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	-1	—	1	μA
Standby supply current	I <sub>DDs</sub>	CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub>	-	1.0	3.0	-	1.0	3.0	-	1.0	3.0	mA
	I <sub>DDs1</sub>	CS1 = CS2 ≥ V <sub>DD</sub> - 0.2V or CS2 ≤ 0.2V	-	2	100	-	2	100	-	2	100	μA
Average operating current	I <sub>DDA</sub>	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> = 0mA t <sub>cyc</sub> = Min	-	45	70	-	45	70	-	45	70	mA
Operating supply current	I <sub>DDO</sub>	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> = 0mA	-	15	35	-	15	35	-	15	35	mA
Output leakage	I <sub>LO</sub>	CS1 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or WE = V <sub>IL</sub> or OE = V <sub>IH</sub> V <sub>I/O</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	-1	—	1	μA
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	—	—	0.4	—	—	0.4	—	—	0.4	V

\* Typical values are measured at T<sub>a</sub> = 25°C and V<sub>DD</sub> = 5.0V

### ● Terminal Capacitance

(f = 1MHz, T<sub>a</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C <sub>ADD</sub>	V <sub>ADD</sub> = 0V	—	—	8	pF
Input Capacitance	C <sub>I</sub>	V <sub>I</sub> = 0V	—	—	10	pF
I/O Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	10	pF

### ● AC Electrical Characteristics

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

#### ○ Read Cycle

Parameter	Symbol	Conditions	SRM20100LC70		SRM20100LC85		SRM20100LC10		Unit
			Min	Max	Min	Max	Min	Max	
Read cycle time	t <sub>RC</sub>	* 1	70	—	85	—	100	—	ns
Address access time	t <sub>ACC</sub>		—	70	—	85	—	100	ns
Chip select 1 access time	t <sub>ACS1</sub>		—	70	—	85	—	100	ns
Chip select 2 access time	t <sub>ACS2</sub>		—	70	—	85	—	100	ns
Output enable access time	t <sub>OE</sub>		—	40	—	45	—	50	ns
Chip select 1 output set time	t <sub>CLZ1</sub>	* 2	10	—	10	—	10	—	ns
Chip select 1 output floating	t <sub>CHZ1</sub>		—	30	—	30	—	35	ns
Chip select 2 output set time	t <sub>CLZ2</sub>		10	—	10	—	10	—	ns
Chip select 2 output floating	t <sub>CHZ2</sub>		—	30	—	30	—	35	ns
Output enable output set time	t <sub>OLZ</sub>		5	—	5	—	5	—	ns
Output enable output floating	t <sub>OHZ</sub>		—	30	—	30	—	35	ns
Output hold time	t <sub>OH</sub>		* 1	10	—	10	—	10	—

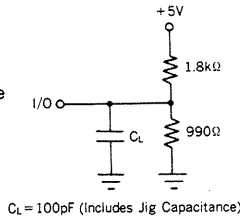
○ Write Cycle

( $V_{DD}=5V \pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=0$  to  $70^\circ C$ )

Parameter	Symbol	Conditions	SRM20100LC70		SRM20100LC85		SRM20100LC10		Unit
			Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{wc}$	* 1	70	—	85	—	100	—	ns
Chip select time 1	$t_{cw1}$		60	—	70	—	80	—	ns
Chip select time 2	$t_{cw2}$		60	—	70	—	80	—	ns
Address enable time	$t_{aw}$		60	—	70	—	80	—	ns
Address setup time	$t_{as}$		0	—	0	—	0	—	ns
Write pulse width	$t_{wp}$		55	—	65	—	75	—	ns
Address hold time	$t_{wr}$		0	—	0	—	0	—	ns
Input data setup time	$t_{dw}$		30	—	35	—	40	—	ns
Input data hold time	$t_{dh}$		0	—	0	—	0	—	ns
$\overline{WE}$ Output floating	$t_{whz}$	* 2	—	30	—	30	—	35	ns
$\overline{WE}$ Output setup time	$t_{ow}$		5	—	5	—	5	—	ns

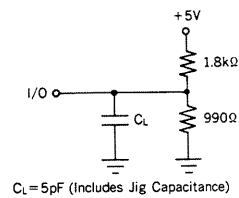
\* 1 Test Conditions

- Input pulse level : 0.6V to 2.4V
- $t_r=t_f=5ns$
- Input and output timing reference levels : 1.5V
- Output load  $C_L=100pF$

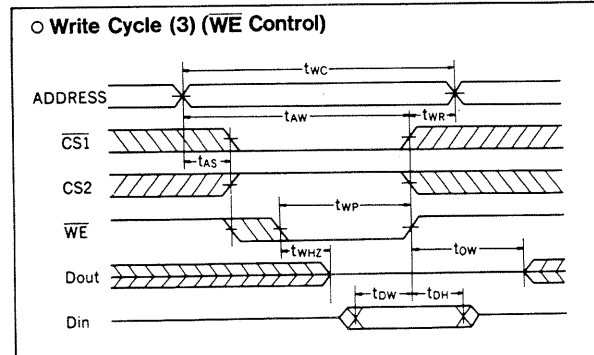
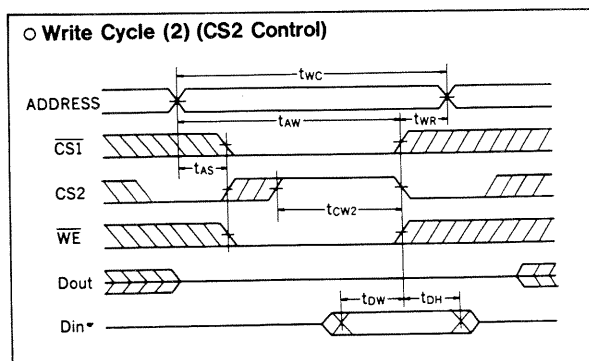
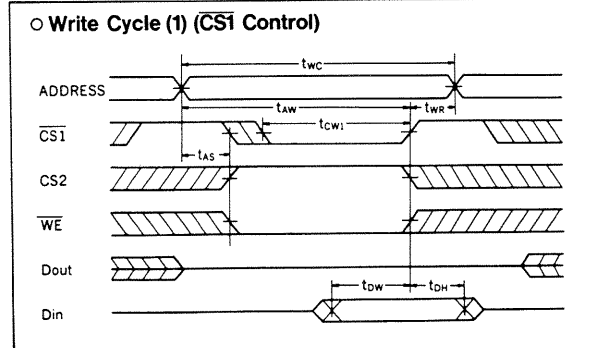
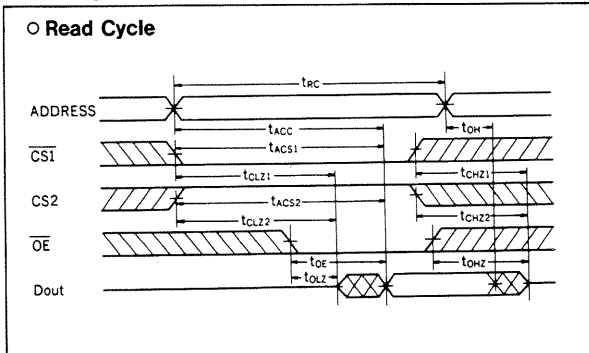


\* 2 Test Conditions

- Input pulse level : 0.6V to 2.4V
- $t_r=t_f=5ns$
- Input timing reference levels : 1.5V
- Output timing reference levels :  $\pm 200mV$  (the level displaced from stable output voltage level)
- Output load  $C_L=5pF$



● Timing Chart



- Note :
- During read cycle time,  $\overline{WE}$  is to be "H" level.
  - During write cycle time that is controlled by CS1 or CS2, Output Buffer is in high impedance state whether  $\overline{OE}$  level is "H" or "L".
  - During write cycle time that is controlled by  $\overline{WE}$ , Output Buffer is high impedance state if  $\overline{OE}$  is "H" level.
  - When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

## DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

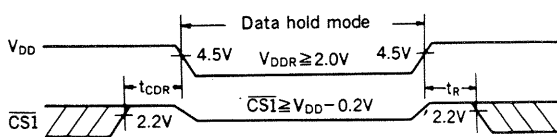
( $T_a = 0$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{DDR}$		2.0	—	5.5	V
Data retention current	$I_{DDR}$	$V_{DD} = 3\text{V}$ $\overline{\text{CS1}} = \text{CS2} \geq V_{DD} - 0.2\text{V}$ or $\text{CS2} \leq 0.2\text{V}$	—	1 *1	50	$\mu\text{A}$
Chip select·data hold time	$t_{CDR}$		0	—	—	ns
Operation recovery time	$t_R$		$t_{RC}$ *2	—	—	ns

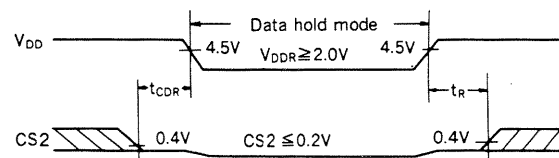
\*1  $T_a = 25^\circ\text{C}$

\*2  $t_{RC}$  = Read cycle time

### Data retention timing ( $\overline{\text{CS1}}$ Control)



### Data retention timing (CS2 Control)



## FUNCTIONS

### Truth Table

$\overline{\text{CS1}}$	CS2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	DATA I/O	Mode	$I_{DD}$
H	X	—	—	Hi-Z	Unselected	$I_{DDs}, I_{DDs1}$
—	L	—	—	Hi-Z	Unselected	$I_{DDs}, I_{DDs1}$
L	H	X	L	Input data	Write	$I_{DDO}$
L	H	L	H	Output data	Read	$I_{DDO}$
L	H	H	H	Hi-Z	Output disable	$I_{DDO}$

X: "H" or "L", —: "H", "L" or "Hi-Z"

### Reading data

Data is able to be read when the address is set while holding  $\overline{\text{CS1}} = \text{"L"}$ ,  $\text{CS2} = \text{"H"}$ ,  $\overline{\text{OE}} = \text{"L"}$  and  $\overline{\text{WE}} = \text{"H"}$ . Since Data I/O terminals are in high impedance state when  $\overline{\text{OE}} = \text{"H"}$ , the data bus line can be used for any other objective, then access time apparently is able to be cut down.

### Writing data

There are the following four ways of writing data into the memory.

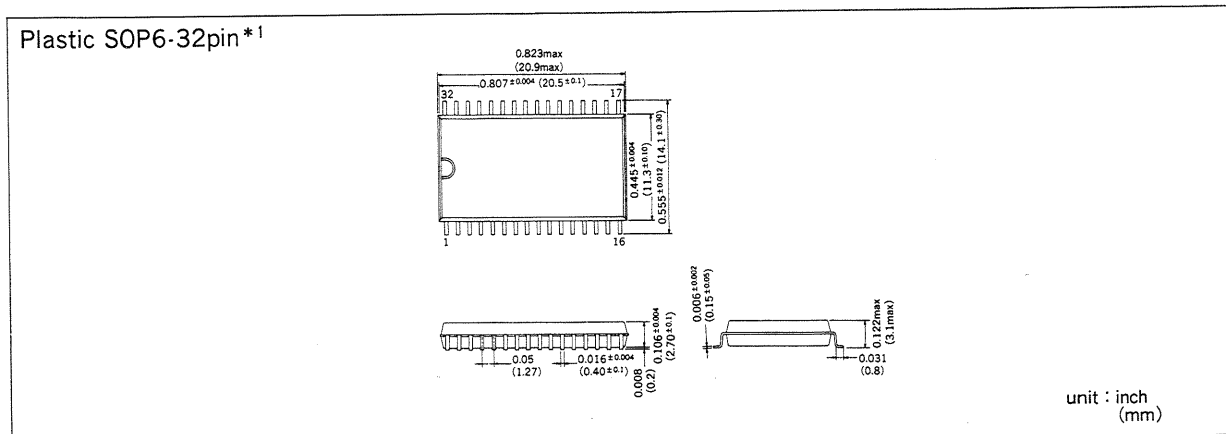
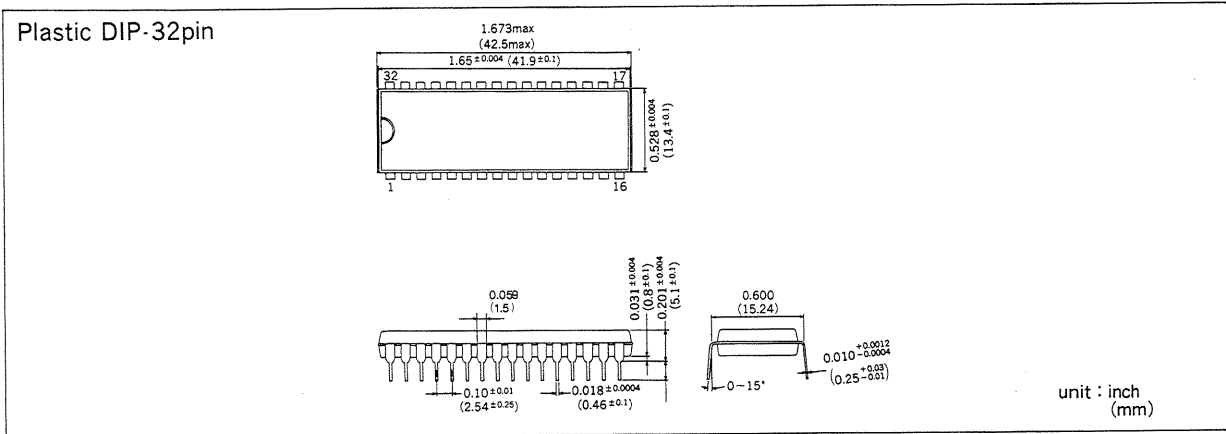
- (1) Hold  $\text{CS2} = \text{"H"}$ ,  $\overline{\text{WE}} = \text{"L"}$  set addresses and give "L" pulse to  $\overline{\text{CS1}}$ .
- (2) Hold  $\overline{\text{CS1}} = \text{"L"}$ ,  $\overline{\text{WE}} = \text{"L"}$ , set addresses and give "H" pulse to CS2.
- (3) Hold  $\overline{\text{CS1}} = \text{"L"}$ ,  $\text{CS2} = \text{"H"}$ , set addresses and give "L" pulse to  $\overline{\text{WE}}$ .
- (4) After setting addresses, give "L" pulse to  $\overline{\text{CS1}}$ ,  $\overline{\text{WE}}$  and give "H" pulse to CS2.

Anyway, data on the Data I/O terminals are latched up into the SRM20100LC70/B5/10 at the end of the period that  $\overline{\text{CS1}}$ ,  $\overline{\text{WE}}$  are "L" level, and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of  $\overline{\text{CS1}}$ ,  $\overline{\text{OE}} = \text{"H"}$ , or  $\text{CS2} = \text{"L"}$ , the contention on the data bus can be avoided.

● Standby mode

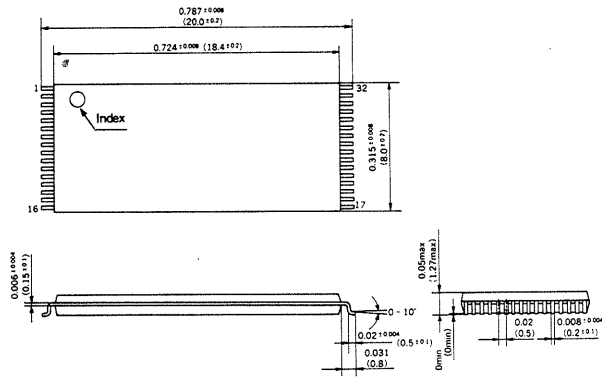
When  $\overline{CS1}$  is "H" or CS2 is "L" level, the SRM20100LC<sub>70/85/10</sub> is in the standby mode which has retaning date operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses,  $\overline{WE}$  and data can be any "H" or "L". When  $\overline{CS1}$  and CS2 level are in the range over  $V_{DD}-0.2V$ , or CS2 level is in the range under 0.2V, in the SRM20100LC<sub>70/85/10</sub> there is almost no current flow except through the high resistance parts of the memory.

■ PACKAGE DIMENSIONS



\*1 SRM20100LM<sub>70/85/10</sub> has the same characteristics as SRM20100LC<sub>70/85/10</sub>.

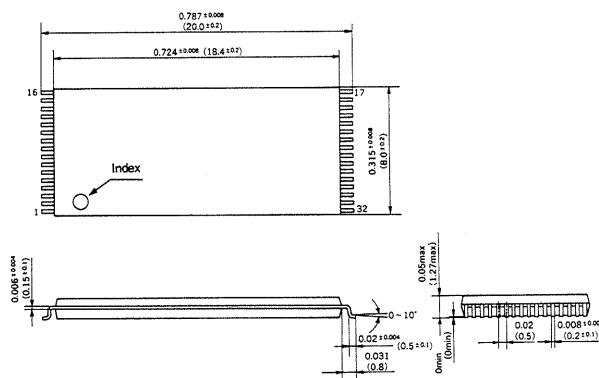
Plastic TSOP-32pin\*1  
(Under development)



unit : inch  
(mm)

\*1 SRM20100LTM70/85/100 has the same characteristics as SRM20100LC70/85/10.

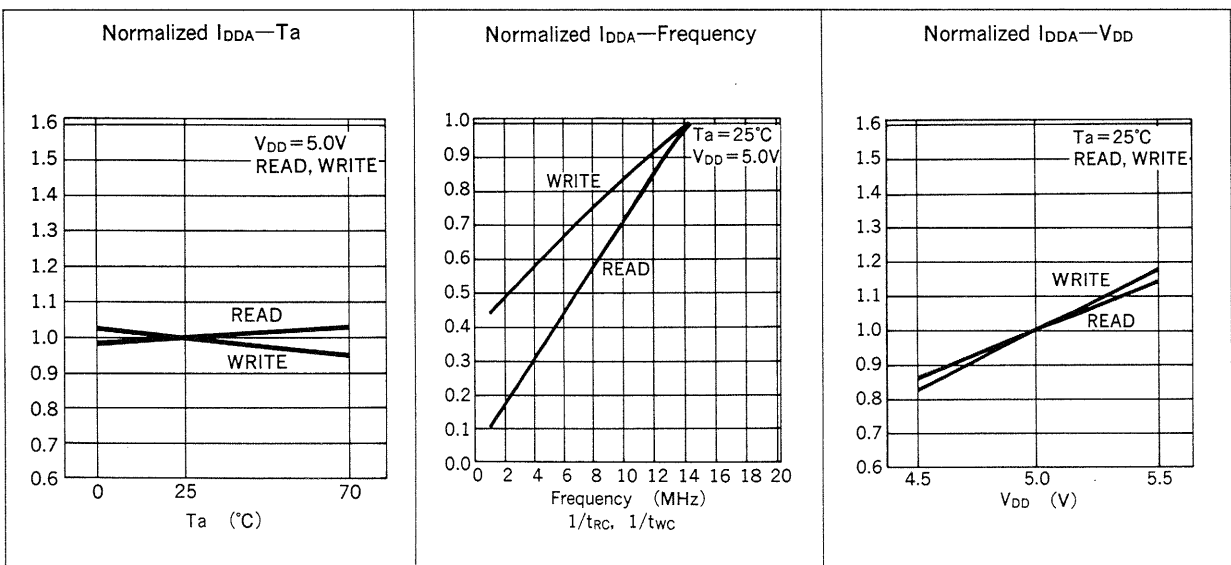
Plastic TSOPR-32pin\*2  
(Under development)



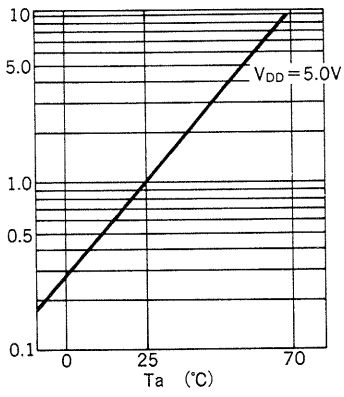
unit : inch  
(mm)

\*2 SRM20100LRM70/85/100 has the same characteristics as SRM20100LC70/85/10.

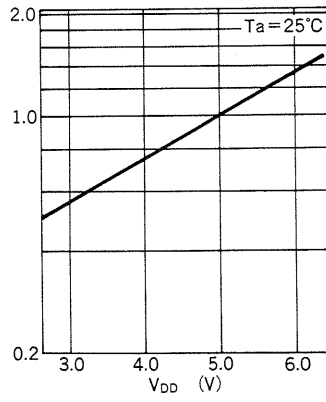
■ CHARACTERISTICS CURVES



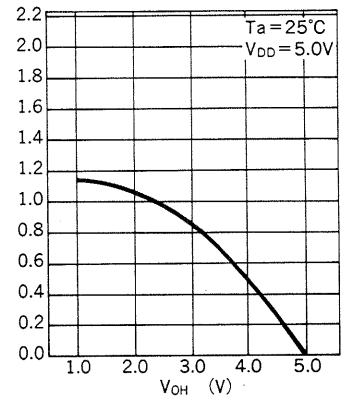
Normalized  $I_{DD1}$ — $T_a$



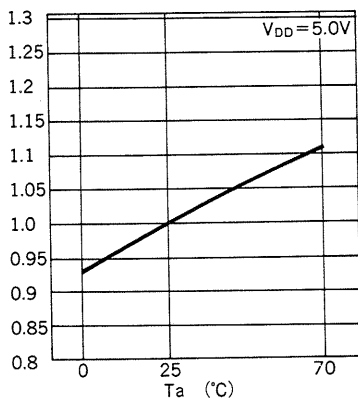
Normalized  $I_{DD1}$ — $V_{DD}$



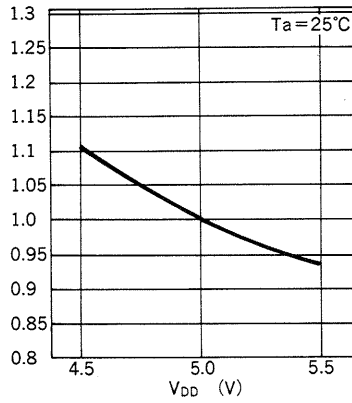
Normalized  $I_{OH}$ — $V_{OH}$



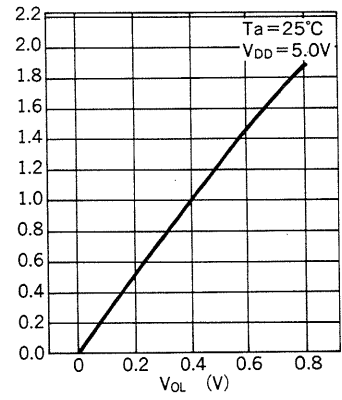
$t_{ACC}$   
Normalized  $t_{ACS1}$   
 $t_{ACS2}$ — $T_a$



$t_{ACC}$   
Normalized  $t_{ACS1}$   
 $t_{ACS2}$ — $V_{DD}$



Normalized  $I_{OL}$ — $V_{OL}$



$t_{ACC}$   
Normalized  $t_{ACS1}$   
 $t_{ACS2}$ — $C_L$

