



SPE0526 5-Line ESD Protection Array

DESCRIPTION

The SPE0526 are designed by TVS bi-direction device that is to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. SPE0526 is bidirectional devices that will protect up to five lines, and may be used on lines where the signal polarities swing above and below ground .

SPE0526 offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

SPE0526 may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SOT-363 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

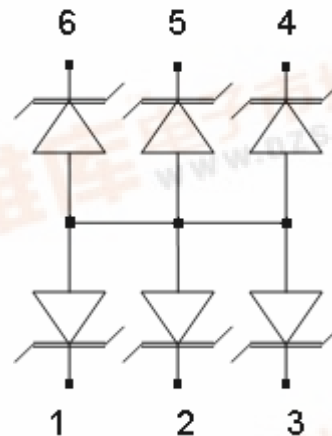
APPLICATIONS

- ◆ Cellular Handsets and Accessories
- ◆ Cordless Phone
- ◆ PDA
- ◆ Notebooks and Handhelds
- ◆ Portable Instrumentation
- ◆ Digital Cameras
- ◆ MP3 Player

FEATURES

- ◆ Transient protection for data lines to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
- ◆ Protects five bidirectional I/O lines
- ◆ Working voltage: 5V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages

PIN CONFIGURATION (SOT-363)



PART MARKING



Y : Year Code
W : Week Code



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ORDERING INFORMATION

| Part Number | Package | Part Marking |
|--------------|---------|--------------|
| SPE0526S36RG | SOT-363 | EAYW |

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPE0526S36RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

| Parameter | Symbol | Typical | Unit |
|---|--------|---------------|------|
| Peak Pulse Power (tp = 8/20 μs) | Ppk | 250 | W |
| Maximum Peak Pulse Current (tp = 8/20 μs) | Ipp | 7 | A |
| ESD per ICE 61000 – 4 – 2 (Air) | Vpp | ±15 | KV |
| ESD per ICE 61000 – 4 – 2 (Contact) | Vpp | ±8 | KV |
| Operating Junction Temperature | Tj | -55 ~ 150 | °C |
| Storage Temperature Range | TSTG | -55 ~ 150 | °C |
| Lead Soldering Temperature | TL | 260 (10sec) | °C |

ELECTRICAL CHARACTERISTICS

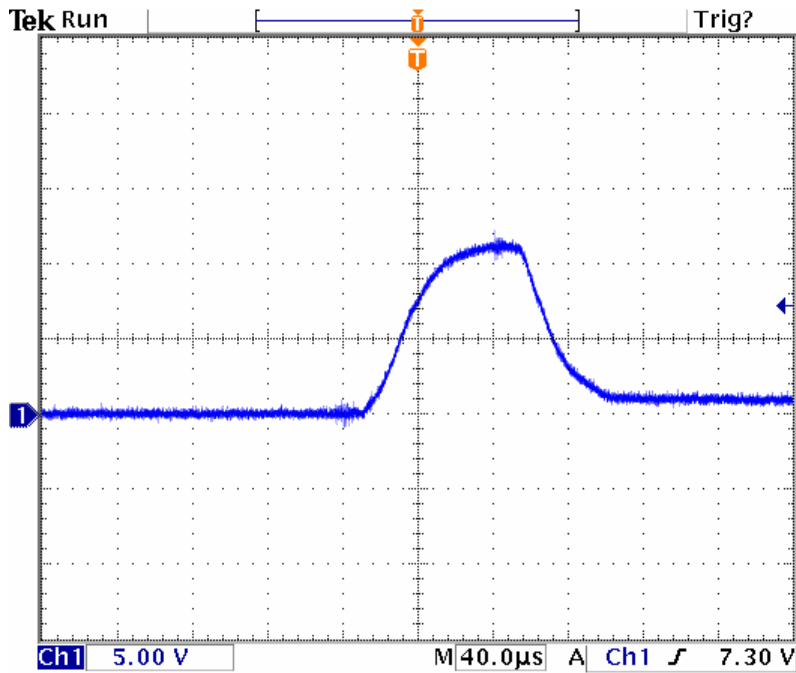
(TA=25°C Unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ | Max. | Unit |
|-----------------------------|--------|---|------|------|------|------|
| Reverse Stand – Off Voltage | VRWM | | | | 5 | V |
| Reverse Breakdown Voltage | VBR | It = 1mA | 6 | | | V |
| Reverse Leakage Current | IR | VRWM = 5V , T=25°C | | 0.01 | 1 | μA |
| Reverse Leakage Current | IR | VRWM = 3V , T=25°C | | 0.01 | 0.5 | μA |
| Clamping Voltage | Vc | Ipp = 1A , tp = 8/20 μs | | | 11.5 | V |
| Clamping Voltage | Vc | Ipp = 7A , tp = 8/20 μs | | | 15 | V |
| Junction Capacitance | Cj | Between I/O Pin and GND VR = 0V , f = 1MHz | | 5 | 10 | pF |



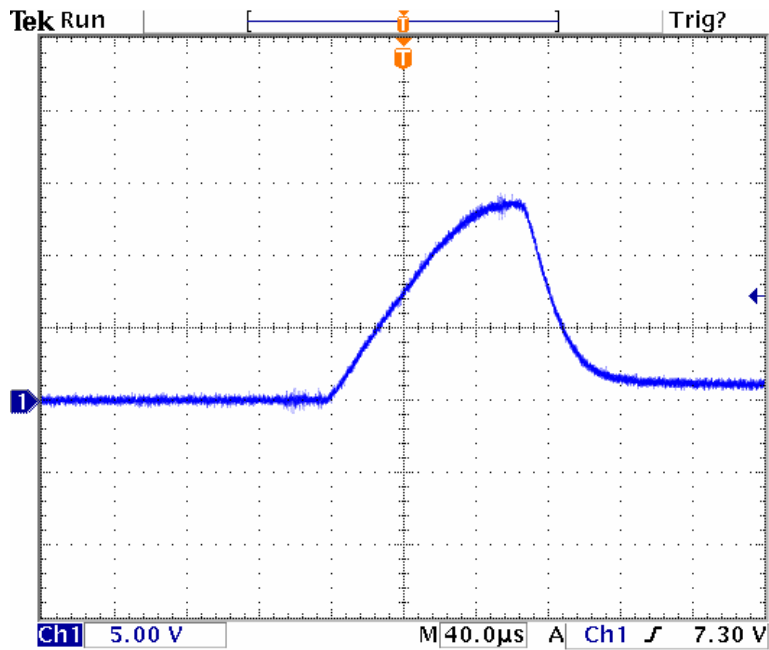
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TYPICAL CHARACTERISTICS



Clamping Voltage ($I_{pp} = 1A$, $t_p = 8/20 \mu s$)

26 Oct 2005
12:15:46



Clamping Voltage ($I_{pp} = 7A$, $t_p = 8/20 \mu s$)

26 Oct 2005
12:08:20



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TYPICAL CHARACTERISTICS

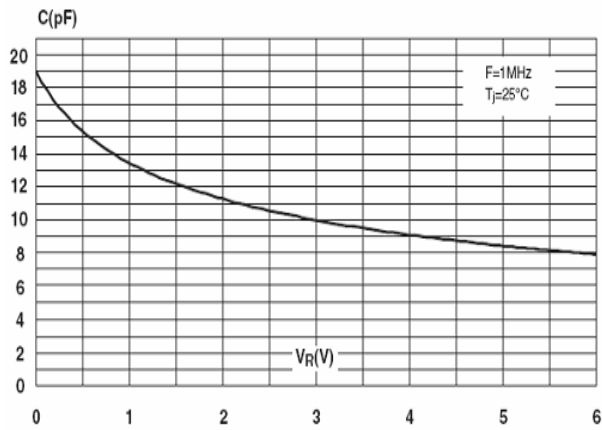


Fig 1 : Junction Capacitance V.S Reverse Voltage Applied

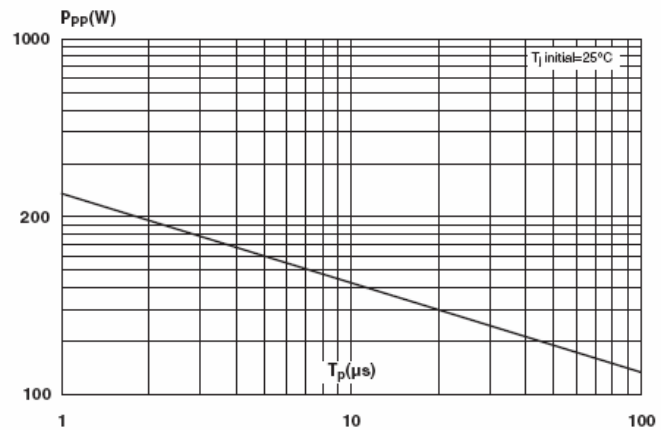


Fig 2 : Peak Plus Power V.S Exponential Plus Duration

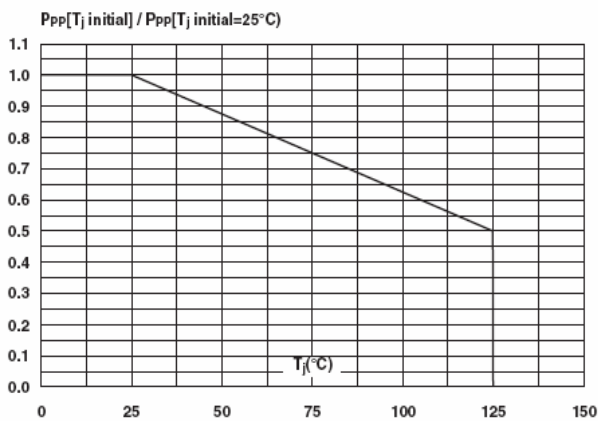


Fig 3 : Relative Variation of Peak Plus Power V.S Initial Junction Temperature

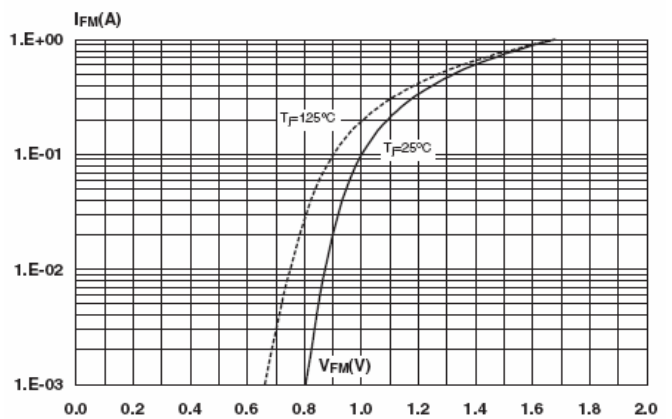


Fig 4 : Forward Voltage Drop V.S Peak Forward Current



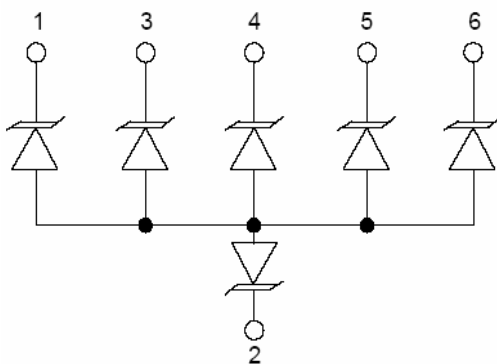
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APPLICATION NOTE

Device Connection for Protection of Five Data Lines

SPE0526 is designed to protect up to five bidirectional data lines. The device is connected as follows:

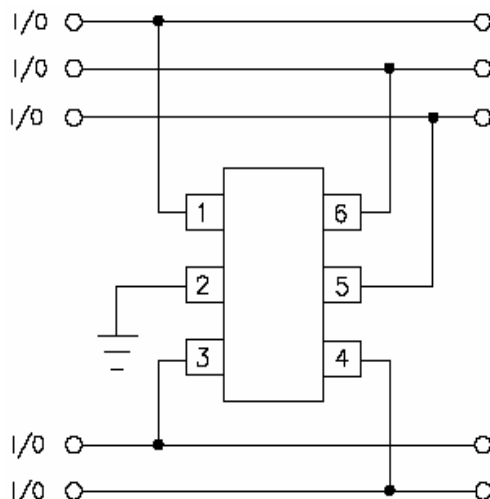
1. Bidirectional protection of five I/O lines is achieved by connecting pins 1, 3, 4, 5, and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.

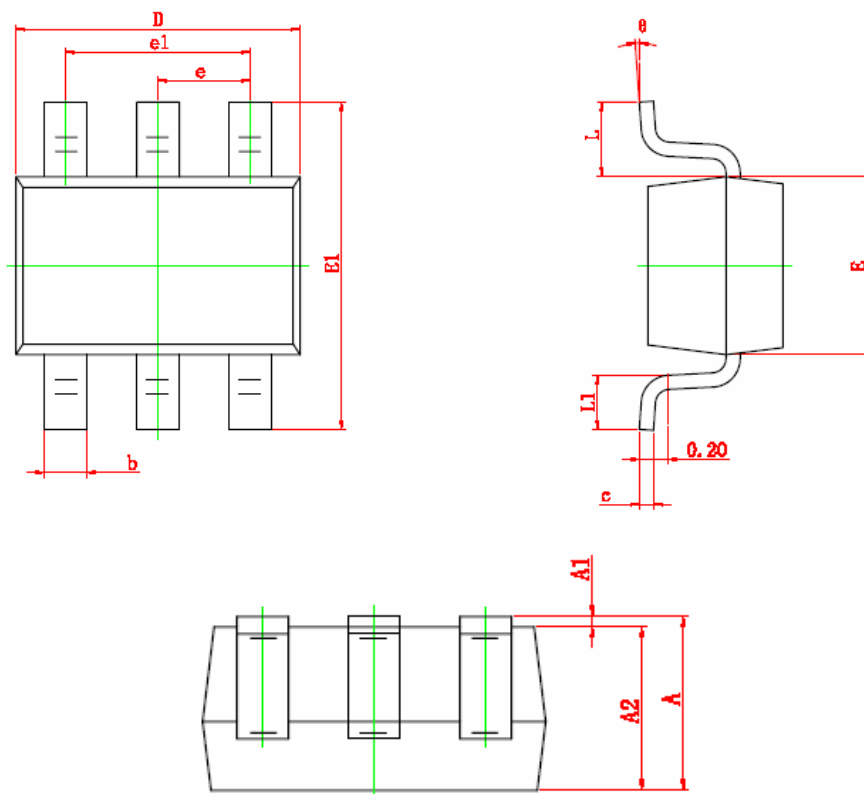




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SOT-363 PACKAGE OUTLINE



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.900 | 1.100 | 0.035 | 0.043 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 0.900 | 1.000 | 0.035 | 0.039 |
| b | 0.150 | 0.350 | 0.006 | 0.014 |
| c | 0.080 | 0.150 | 0.003 | 0.006 |
| D | 2.000 | 2.200 | 0.079 | 0.087 |
| E | 1.150 | 1.350 | 0.045 | 0.053 |
| E1 | 2.150 | 2.450 | 0.085 | 0.096 |
| e | 0.650 TYP | | 0.026 TYP | |
| e1 | 1.200 | 1.400 | 0.047 | 0.055 |
| L | 0.525 REF | | 0.021 REF | |
| L1 | 0.260 | 0.460 | 0.010 | 0.018 |
| θ | 0° | 8° | 0° | 8° |



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