ZARLINK SEMICONDUCTOR

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SP5024

3-Wire Bus Controlled Synthesiser

DS2452 - 2.1 December 1992

The SP5024 is a programming variant of the SP5510 allowing the design of one tuner with either I^2C bus or 3-wire bus format depending on which device is inserted. The SP5024, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-8 prescaler with its own preamplifier and a 15 bit programmable divider controlled by a serially - loaded data register. Four open-collector outputs, each independently programmable, are included. The device has two modes of operation selected by the 'mode selected input'. In mode 1 the comparison frequency is 7.8125kHz and the programmable divider MSB is bypassed; mode 2 comparison frequency is 6.25kHz. The comparison frequencies are both obtained from a 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete 1.3GHz Single Chip System
- Dual Standard 50kHz or 62.5kHz Step Size
- Low Power Consumption (5V 40mA)
- Programming Compatible with Toshiba TD6380 and TD6381 *
- Pin Compatible with SP5510 *
- Low Radiation
- Varactor Drive Amplifier Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

* See notes on pin compatibility

† Normal ESD handling procedures should be observed

APPLICATIONS

- Satellite TV When Combined With SP4902 2.5GHz Prescaler
- Cable Tuning Systems
- VCRs

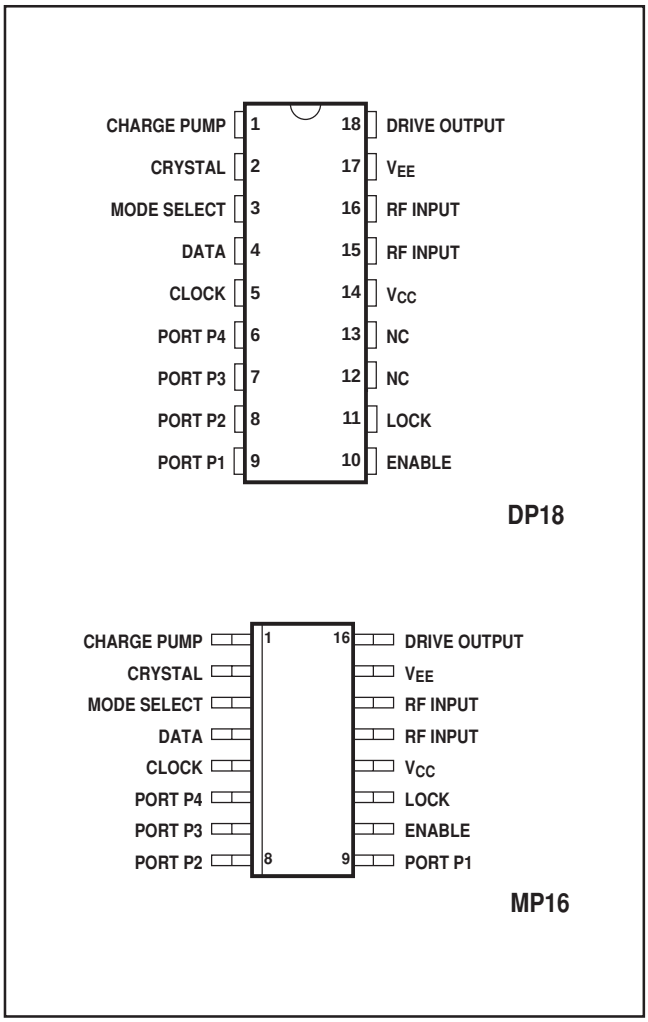

Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5024 DP - (18-lead plastic package)
SP5024S MP - (16-lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4·5V to +5·5V. Reference frequency = 4MHz. Pin numbers refer to SP5024 (DP package). These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Supply current	I_{CC}	14		40	55	mA	V_{CC} = 5V
Prescaler input voltage		15,16	12.5		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler input voltage		15, 16	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler input impedance Input capacitance		15,16		50 2		Ω pF	
High level input voltage		4,5,10	3		V_{CC}	V	
High level input voltage		3	4		V_{CC}	V	
Low level input voltage		3,4,5,10	0		0.6	V	
High level input current		4,5,10			1	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current		5			5	µA	V_{IN} = 0V, V_{CC} = 5·5V
Low level input current		4,10			-250	µA	V_{IN} = 0V, V_{CC} = 5·5V
High level input current		3			150	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current		3			-1	µA	V_{IN} = 0V, V_{CC} = 5·5V
Clock input hysteresis		5		0.4		V	
Clock rate		5			0.5	MHz	
Data set up time	t_2	4	300			ns	See Fig. 3
Data hold time	t_3	4	600			ns	See Fig. 3
Enable set up time	t_1	10	300			ns	See Fig. 3
Enable hold time	t_5	10	600			ns	See Fig. 3
Clock-to-enable time	t_4	10	300			ns	See Fig. 4
Charge pump output current		1		±150		µA	V pin 1 = 2·0V
Charge pump output leakage current		1			±5	nA	V pin 1 = 2·0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Charge pump drive output current		18	1			mA	V pin 18 = 0·7V
Charge pump amplifier gain				6400			Pin 18 Current 100µA
Oscillator temperature stability					2	ppm/°C	
Oscillator stability with supply voltage					2	ppm/V	
Recommended crystal series resistance			10		200	Ω	"Parallel resonant" crystal
Crystal oscillator drive level		2		40		mV p-p	
Crystal oscillator source impedance		2		-400		Ω	Nominal spread = ±15%

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Port and Lock sink current		6 - 9,11	10			mA	V_{OUT} = 0.7V
Port leakage current		6-9			10	µA	V_{OUT} = 13.2V
Lock leakage current		11			10	µA	$V_{OUT} = V_{CC}$
Varactor Drive Amp Disable		10	-350			µA	V_{IN} = <0V
Charge Pump Disable		4	-350			µA	V_{IN} = <0V

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Parameter	Pin SP5024	Pin SP5024 S	Value		Units	Conditions
			Min.	Max.		
Supply voltage	14	12	-0.3	-6	V	
Prescaler inputs	15, 16	13, 14		2.5	Vp-p	
Output ports	6-9	6-9	-0.3 -0.3	14 6	V V	Port in off state Port in on state
Total port output current	6-9	6-9		50	mA	
Prescaler DC offset	15, 16	13, 14	-0.3	V_{CC}+0.3	V	
Loop amplifier DC offset	1, 18	1, 16	-0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC}+0.3	V	
Data bus inputs	4, 5 ,10	4, 5 ,10	-0.7	V_{CC}+0.3	V	With V_{CC} applied
Storage temperature			-55	+125	°C	
Junction temperature				+150	°C	
DP 18 thermal resistance, chip-to-ambient DP 18 thermal resistance, chip-to-case				78 24	°C/W °C/W	
MP 16 thermal resistance, chip-to-ambient MP 16 thermal resistance, chip-to-case				111 41	°C/W °C/W	
Power consumption at 5V				275	mW	All ports off

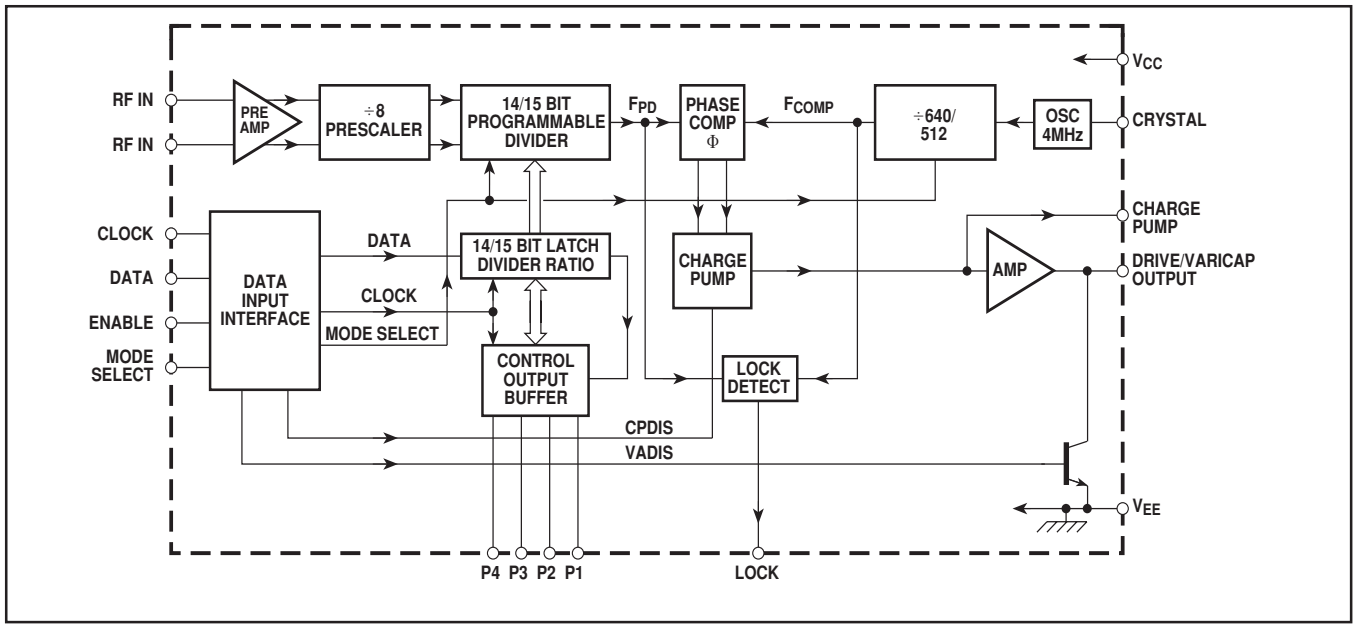

Fig.2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5024 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock, enable, three-wire data bus. The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format shown in Fig. 3.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 6.25kHz/7.8125kHz and, when multiplied back up to the synthesised LO, gives a minimum step size of 50kHz/62.5kHz, respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity. The input sensitivity and impedance are shown in Figs. 5 and 7, respectively.

The SP5024 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'Out of lock' is indicated by high impedance state.

The SP5024 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the normal data word.

PIN COMPATIBILITY

The SP5024 may be used in SP5510 applications which require 3-wire bus as opposed to I^2C bus data format. In SP5510 applications where the reference crystal is connected to pin 3, a small modification is required to ground the crystal as shown in Fig. 4.

Appropriate connections to the mode select input (pin 3) must also be made.

In mode 1 (pin 3 'HIGH') the SP5024 is programming and step size compatible with the Toshiba TD6380, and in mode 2 (pin 3 'LOW') it is compatible with the TD6381. In both modes a 4MHz crystal is used to derive F_{COMP}, unlike the TD6381 which requires a 3.2MHz crystal.

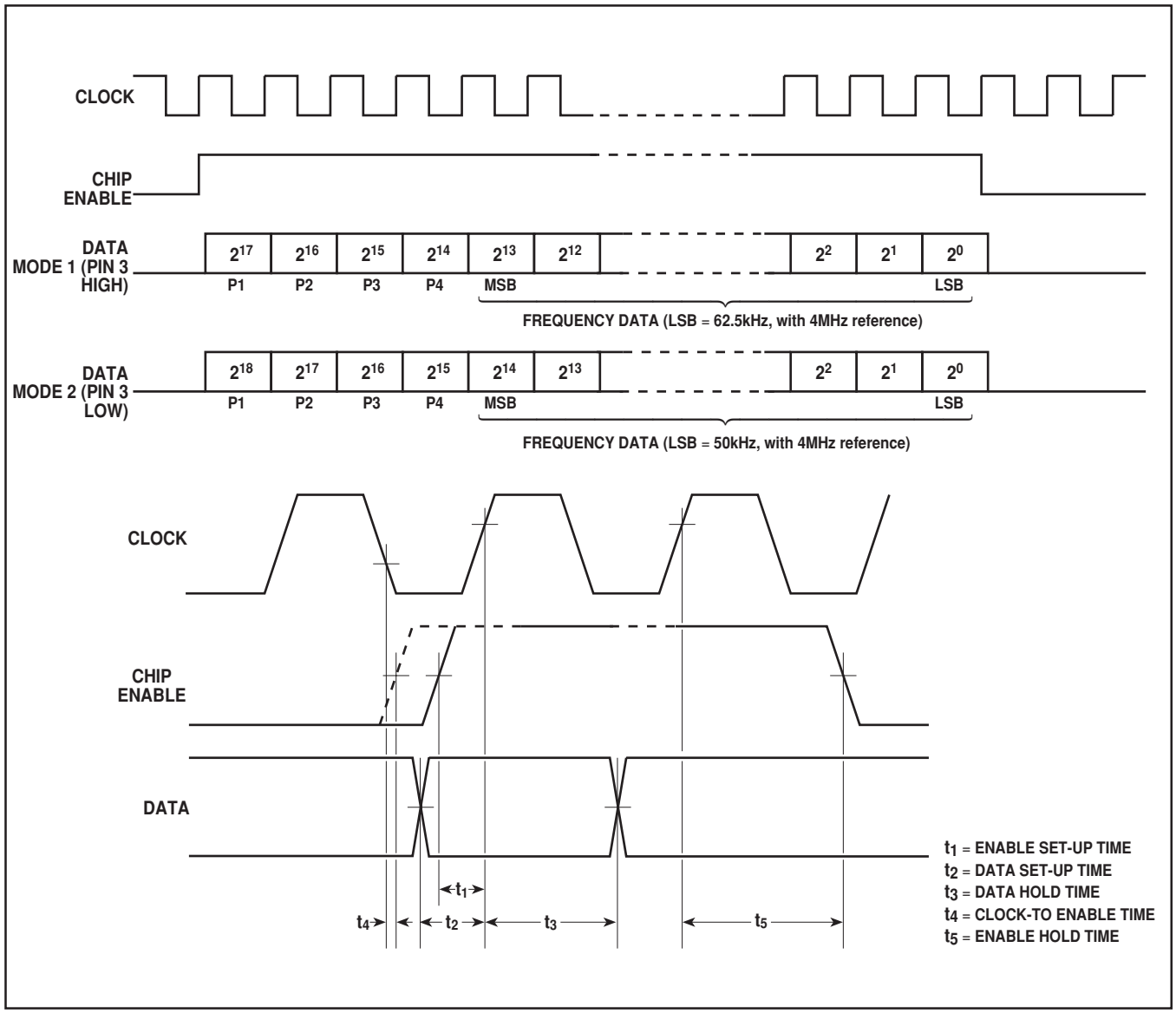

Fig. 3 Data format and timing

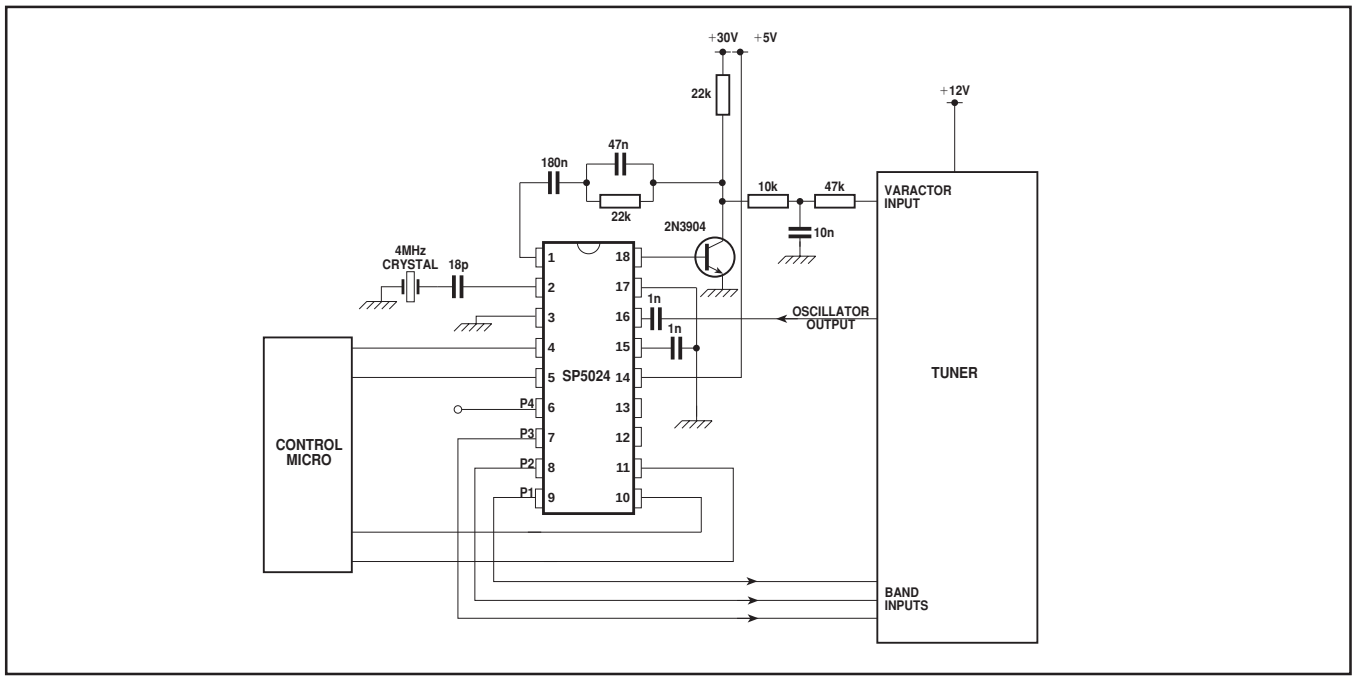

Fig. 4 Typical application (F_{STEP} = 50kHz)

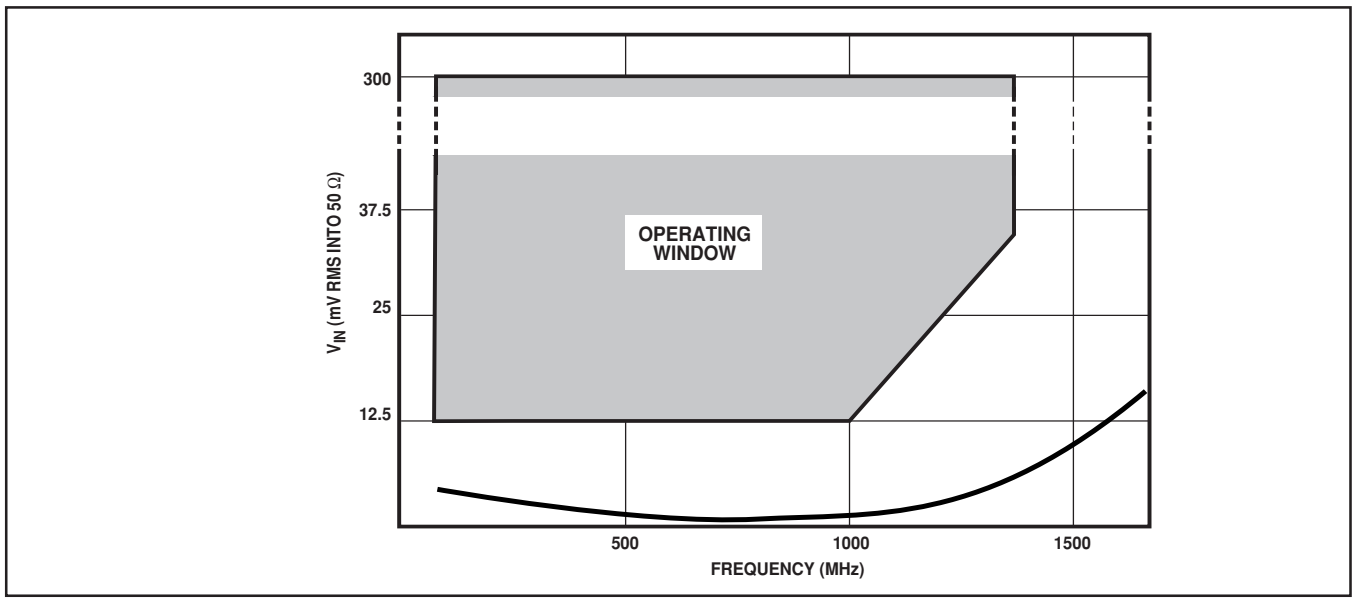

Fig. 5 Typical input sensitivity

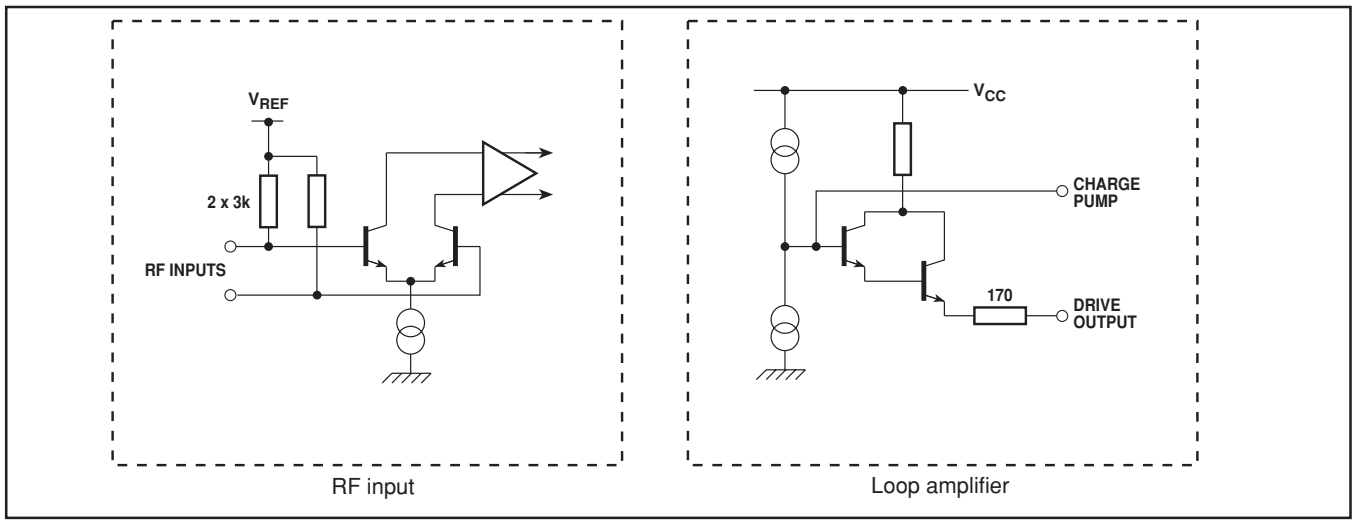

Fig.6a Input/Output interface circuits

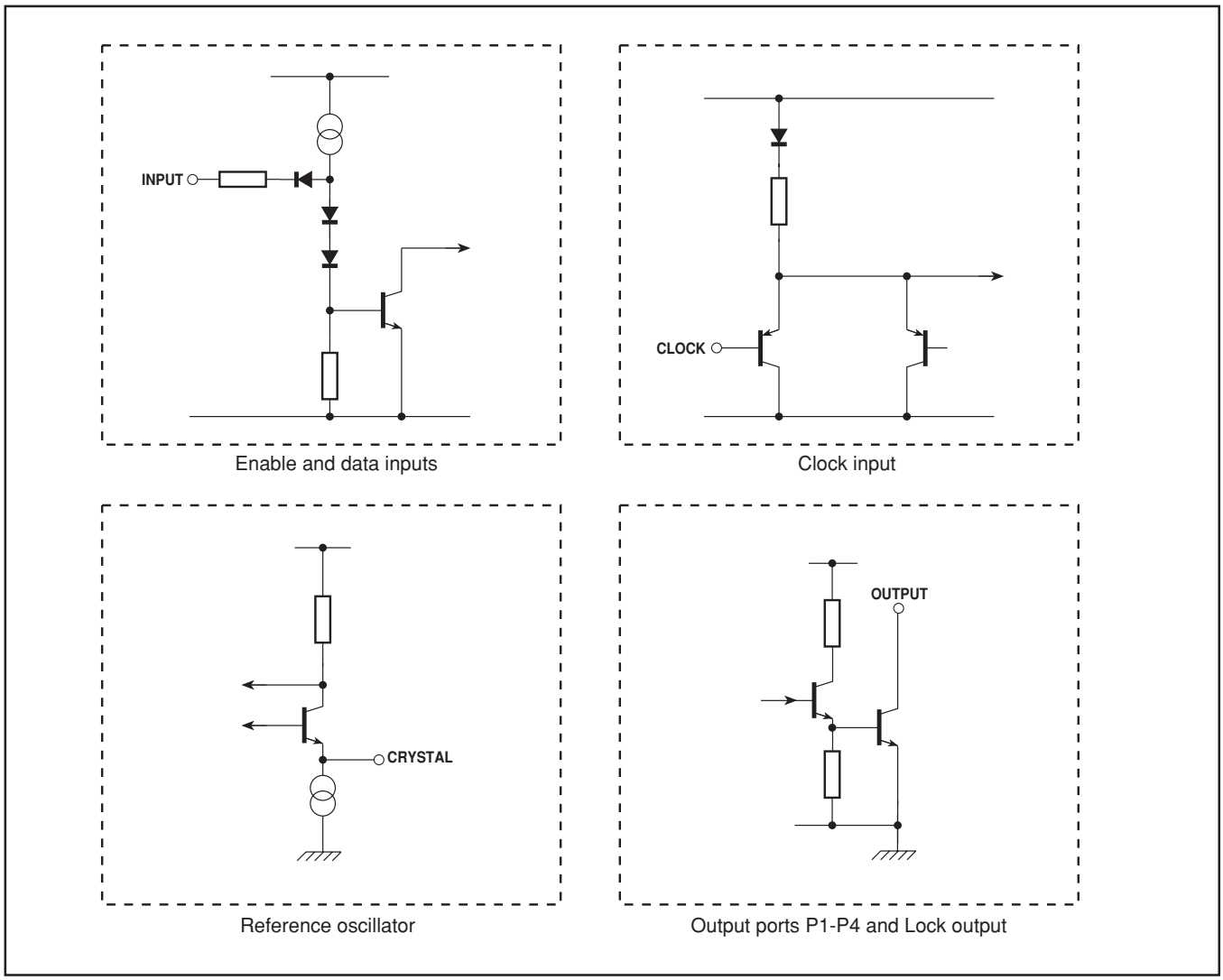

Fig.6b Input/Output interface circuits

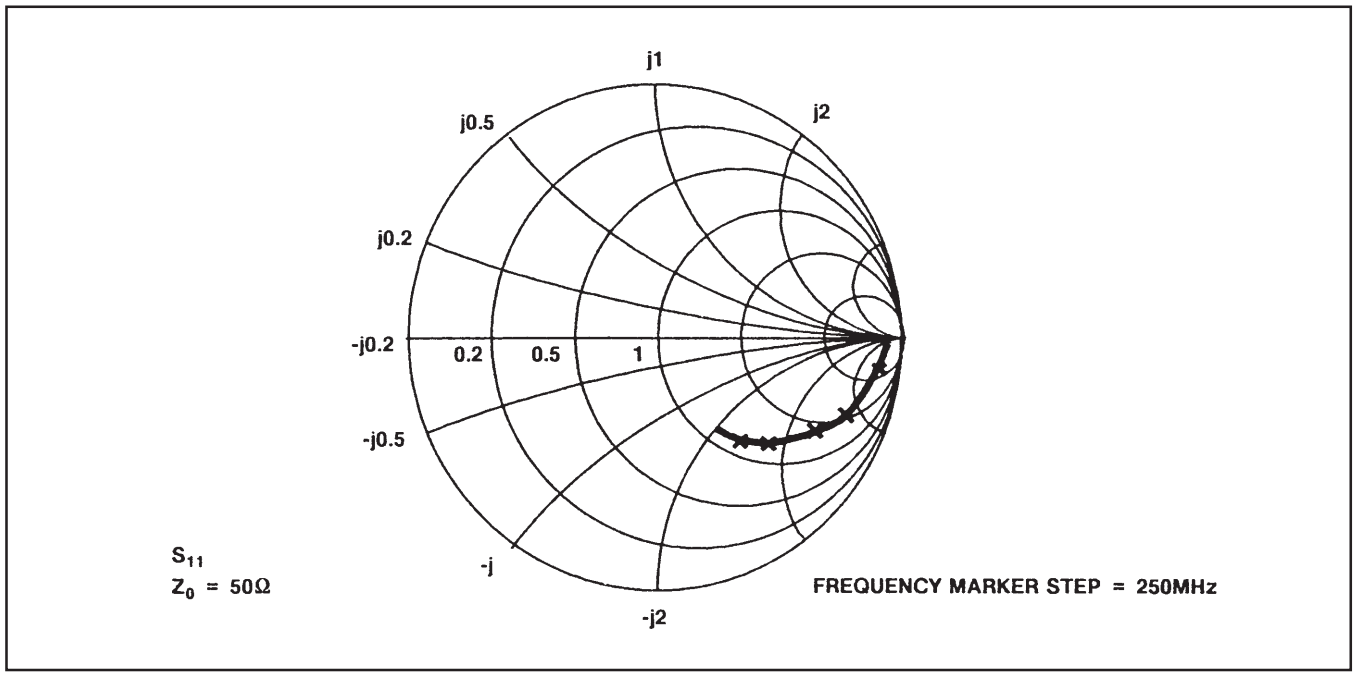

Fig.7 Typical input impedance

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