SUMMIT MICROELECTRONICS, Inc.

SMS1242

2.5V, 3V, 3.3V & 5V Dual Voltage, Dual Reset Microprocessor Supervisory Circuits

FEATURES

- **Supply voltage monitor**
  - **Nominal V_{RST} of 2.45V, 2.65V, 2.95V, 4.45V, 4.55V or 4.65V**
  - **RESET# Outputs Guaranteed true at V_{CC} = 1V**
  - **150ms Reset Delay Time**
- **Second voltage monitor**
  - **V_{SENSE} Input**
  - **1.25V threshold ±1%**
- **Manual Reset Input**
- **Includes 16k-bits nonvolatile memory**
  - **Industry standard 2-wire serial interface**

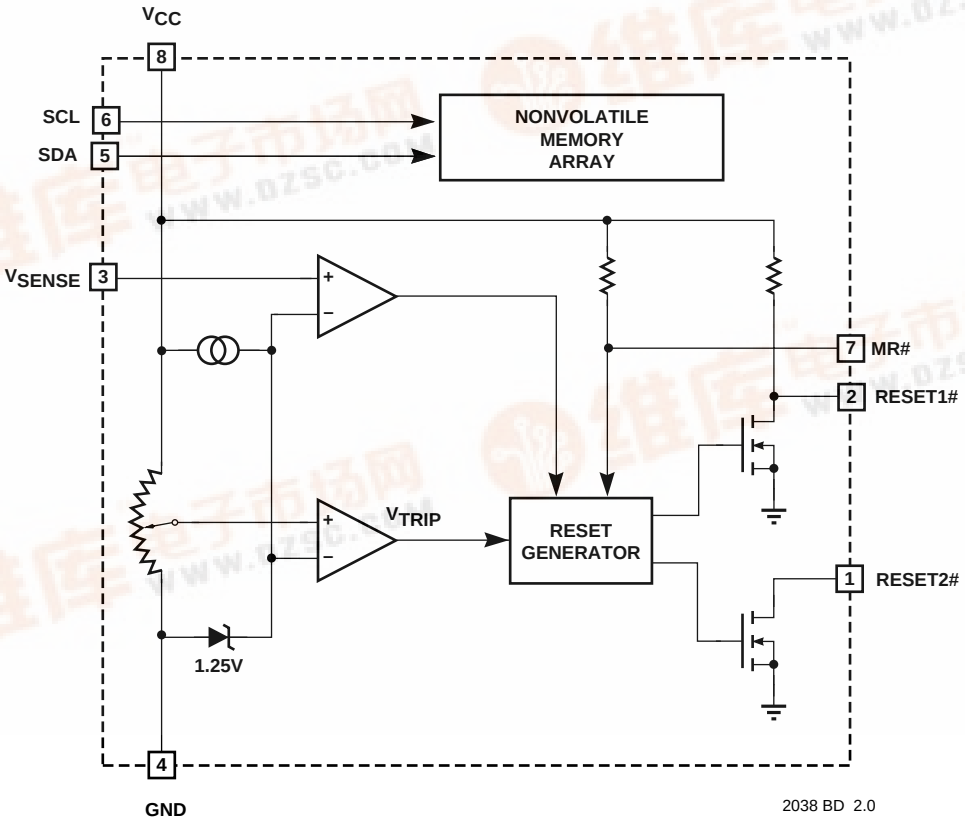
OVERVIEW

The SMS1242 microprocessor supervisory circuit reduces the complexity and number of components required to monitor the supply voltage in +5V, +3V and +2.5V systems. The SMS1242 will significantly improve system reliability and accuracy when compared to implementing the same functions with discrete components.

The SMS1242 provides reset output during power-up, power-down, and brown-out conditions. It has a 1.25V threshold input detector for power-fail warning, low battery detection, or monitoring a secondary power supply. The part also integrates a separate active low manual reset input.

It also has 16k-bits of nonvolatile memory accessible over an industry standard 2-wire serial interface.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	–55°C to 125°C
Storage Temperature	–65°C to 150°C
Terminal Voltage (With Respect to Ground)	–0.3V to 6V
Lead Solder Temperature (10 secs)	300°C

***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Operating supply voltage		1		5.5	V
I_{CC}	Supply current	$3.6V < V_{CC} < 5.5V$		25	50	µA
		$3.6V > V_{CC}$		25	50	µA
		Memory access (SMS1243 only)			3	mA
V_{RST}	Reset threshold	Device option A	4.375	4.425	4.475	V
		Device option B	4.625	4.675	4.725	V
		Device option C	4.425	4.475	4.525	V
		Device option D	2.425	2.450	2.475	V
		Device option E	2.625	2.650	2.675	V
		Device option F	2.925	2.950	2.975	V
V_{HYST}	V_{RST} Hysterisis			50		mV
t_{RST}	Reset pulse width		100	150	200	ms
V_{OL}	RESET1# output low voltage	$I_{SINK} = 1.2mA$, $V_{CC} = V_{RST}$ min.			0.3	V
		$I_{SINK} = 200µA$, $V_{CC} = 1.2V$			0.3	V
I_{MR}	MR# pullup current			100		µA
t_{MR}	MR# pulse width		50			ns
V_{IL}	MR# input threshold				0.6	V
V_{IH}	MR# input threshold		$0.7 \times V_{CC}$			V
V_{SNS}	V_{SENSE} input threshold	$V_{CC} = V_{RST}$ min., V_{SENSE} falling	1.20	1.25	1.30	V
V_{CC}	RESET2# output low voltage	$I_{SINK} = 1.2mA$, $V_{CC} = V_{RST}$ min.			0.3	V
		$I_{SINK} = 200µA$, $V_{CC} = 1.2V$			0.4	V

2038 Elect Table 2.0

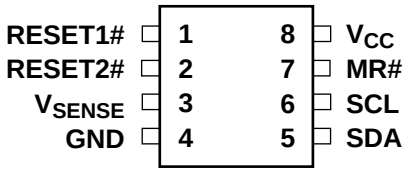
PIN NAMES

Pin	Signal	Function
1	RESET1#	Active low output with weak pullup. Driven low by: V_{SENSE} below threshold; or V_{CC} below threshold while MR# is below threshold. Remains low for 150ms after V_{SENSE}, or V_{CC} and MR#, is above threshold.
2	RESET2#	Same as Reset1#, except open drain connection
3	V_{SENSE}	Threshold detector input for the Resets
4	GND	Ground
5	SDA/GND	SMS1243 Data I/O, or ground
6	SCL/GND	SMS1243 Data Clock, or ground
7	MR#	Manual input for Resets
8	V_{CC}	Supply voltage

2038 Pin Table 2.0

PIN CONFIGURATION

8-Pin SOIC



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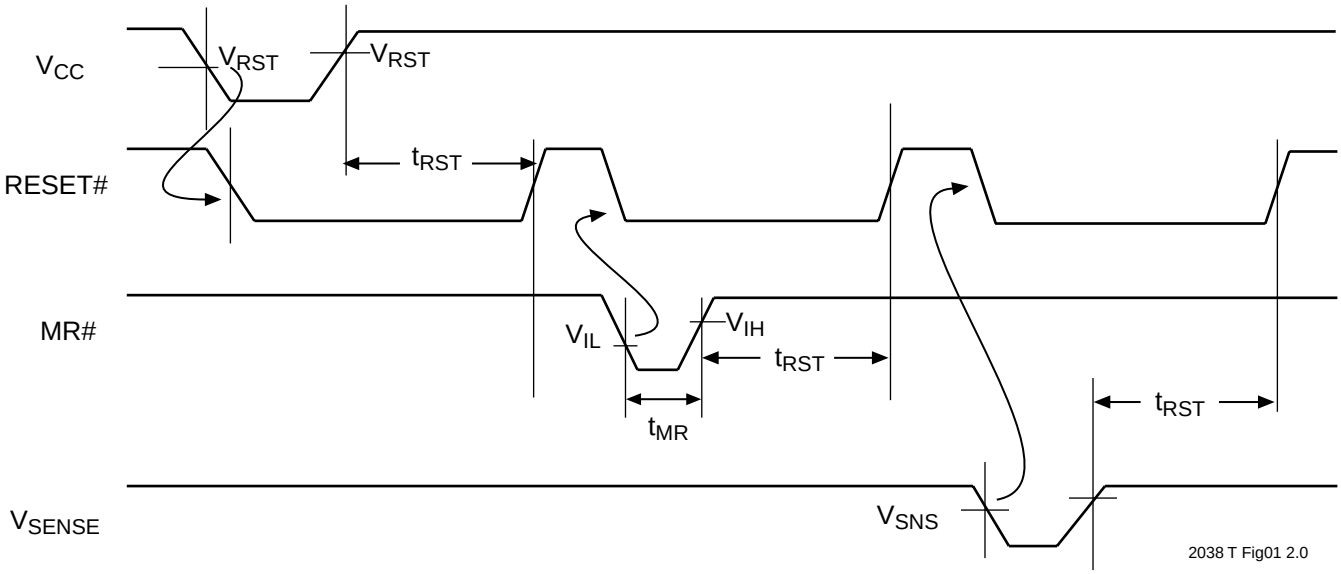

Figure 1. Reset Waveforms

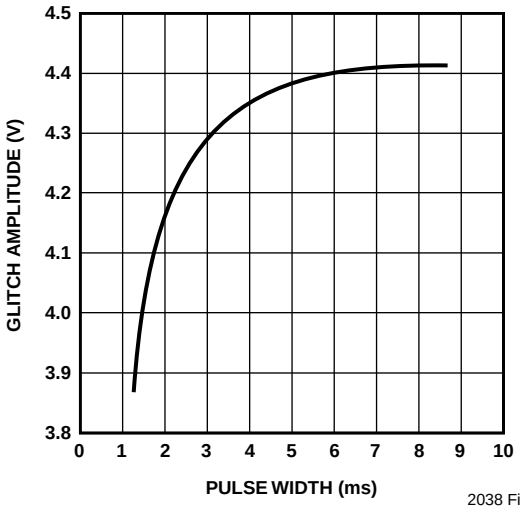

Figure 2. Supply Voltage Noise Rejection, V_{RST} =4.55V, T_A = 25ºC

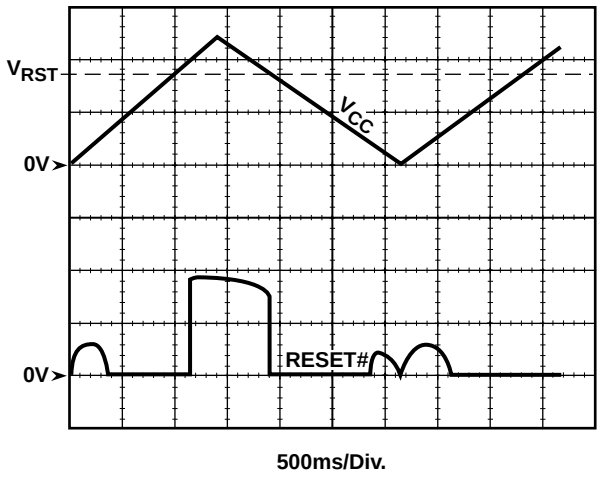

Figure 3. RESET Output vs. Supply

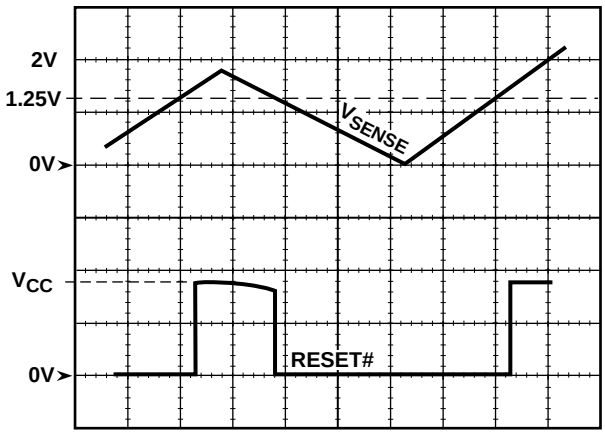

Figure 4. RESET Output vs. V_{SENSE}

DEVICE OPERATION

The SMS1242 provides a precision reset function for a microcontroller or microprocessor during power-up, power-down and brown-out conditions. The device will monitor two independent voltage supplies and will generate a reset condition when either supply is invalid. It is configured with two outputs, both driven by the same conditions. They are open drain and will track each other but the outputs are not internally tied together.

Because RESET1# and RESET2# are essentially open drain outputs (RESET1# has a weak internal pullup, RESET2# does not) they can be independently driven low by external signals. This can be very useful in a dual processor system or in a combined processor/ASIC system where, either for system operation or system test, the processors or ASICs must be independently held in reset without resetting the other portion of the system.

SUPPLY MONITOR

(Assume $V_{SENSE} > V_{SNS}$) During power-up the SMS1242 monitors the supply voltage. The RESET1# and RESET2# outputs are guaranteed to be driven low once V_{CC} reaches 1V. As V_{CC} rises RESET1# and RESET2# remain asserted until V_{CC} reaches the V_{RST} threshold. As V_{CC} passes through V_{RST} an internal timer is started to continue driving the outputs for an additional 150ms (nominal).

If a power-fail or brown-out condition occurs ($V_{CC} < V_{RST}$) RESET1# and RESET2# will be asserted. They will remain active so long as V_{CC} is below V_{RST}. Because the internal timer will be continuously reset so long as V_{CC} is below V_{RST}, a brownout condition that interrupts a previously initiated reset pulse causes an additional reset delay from the time the V_{CC} passes back through V_{RST}.

During power down conditions, once V_{CC} drops below V_{RST}, RESET1# and RESET2# are guaranteed to be asserted for $V_{CC} \geq 1V$.

V_{SENSE} MONITOR

(Assume V_{CC} is $>V_{RST}$) The SMS1242 continuously monitors the VSENSE input. The RESET1# and RESET2# outputs will be driven low so long as V_{SENSE} is < VSNS. As V_{SENSE} passes through V_{SNS} an internal timer is started to continue driving the outputs for an additional 150ms (nom.).

If a power-fail condition occurs (V_{SENSE} falls below V_{SNS}) RESET1# and RESET2# will be asserted. They will remain active so long as V_{SENSE} is below V_{SNS}. Because the internal timer will be continuously reset so long as V_{SENSE} is below V_{SNS}, a brownout condition that interrupts a previously initiated reset pulse causes an additional reset delay from the time V_{SENSE} becomes greater than V_{SNS}.

MANUAL RESET

The manual reset input allows RESET1# and RESET2# to be activated by a pushbutton switch. The switch is effectively debounced by the 100ms minimum t_{RST} (RESET pulse width). MR# can also be driven by an external logic input that meets the 50ns minimum pulse width required.

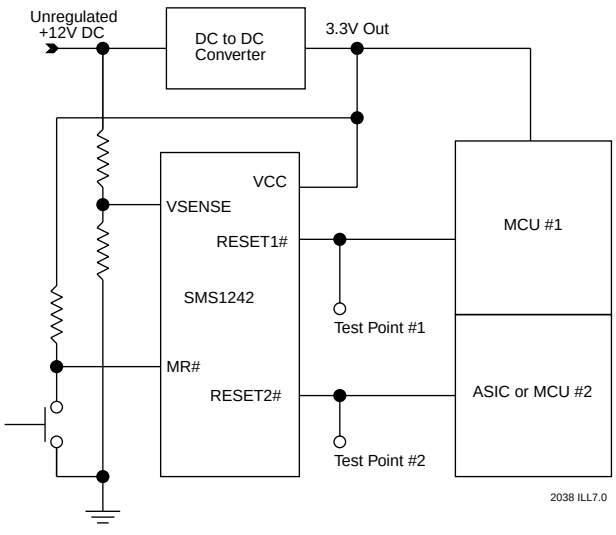

Figure 5. Typical Multi-MCU Implementation

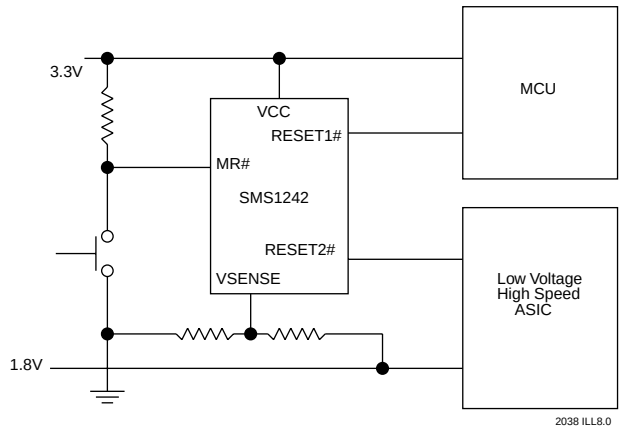

Figure 6. Typical Dual Voltage Implementation

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.3	3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.3		µs
t_{R}	SCL and SDA rise time			1000	ns
t_{F}	SCL and SDA fall time			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA	Noise suppresion		100	ns
t_{WR}	Write cycle time			5	ms

2038 Table01 2.0

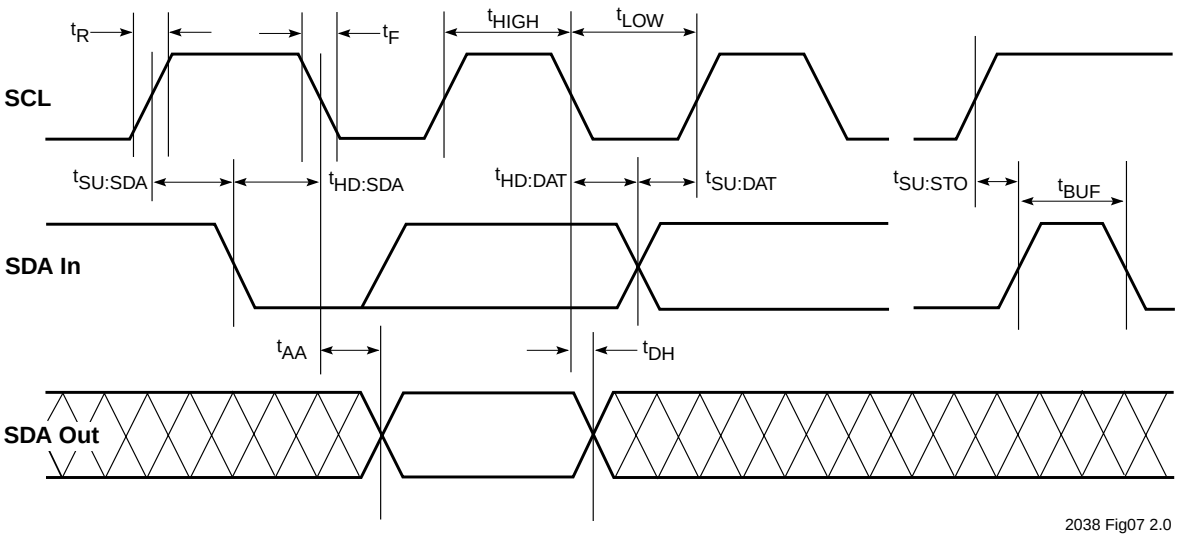

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Figure 7. Memory Timing

MEMORY OPERATION

The SMS1242 memory is configured as a 2k × 8 array. Data is read and written via an industry standard two-wire interface. The bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA) and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor located somewhere on the bus

Input Data Protocol

The protocol defines any device that sends data onto the bus as a "transmitter" and any device that receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases the SMS1242 will be a "slave" device since it never initiates a data transfer.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because changes on the data line while SCL is high will be interpreted as start or stop condition.

START and STOP Conditions

When both the data and clock lines are high the bus is said to be not busy. A high-to-low transition on the data line while the clock is high is defined as the "START" condition. A low-to-high transition on the data line while the clock is high is defined as the "STOP" condition.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line low to ACKnowledge that it received the eight bits of data.

The SMS1242 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMS1242 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word. In the READ mode the SMS1242 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected and no STOP condition is generated by the master, the SMS1242 will continue to transmit data. If an ACKnowledge is not detected the SMS1242 will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier. For the SMS1242 this is fixed as 1010_{BIN}. The next three bits are the Most Significant Bits of the data address. They are supplied for write operations, and are "don't care" for read operations.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. A "1" indicates a read operation; and a "0," a write operation.

Device Identifier				MS Address Bits			R / W
1	0	1	0	A10	A9	A8	1 / 0

2038 Table02 2.0

WRITE OPERATIONS

The SMS1242 allows two types of write operations: byte write and page write. A byte write operation writes a single byte during the nonvolatile write period (tWR). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte Write

Upon receipt of the word address the SMS1242 responds with an ACKnowledge. After receiving the next byte of data it responds with another ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS1242 begins the internal write cycle. While the internal write cycle is in progress the SMS1242 inputs are disabled and the device will not respond to any requests from the master.

Page Write

The SMS1242 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word the master can transmit up to 15 more bytes of data. After the receipt of each byte the SMS1242 will respond with an ACKnowledge.

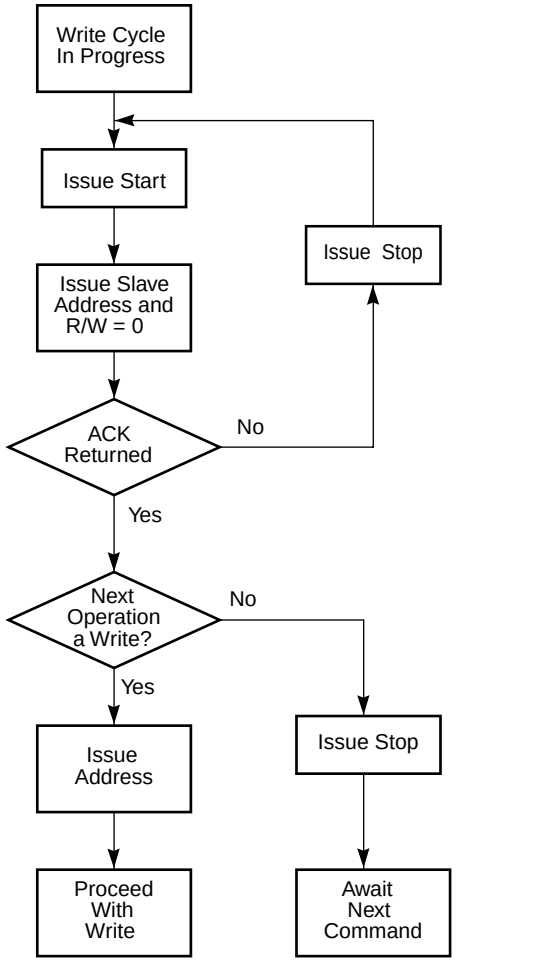
The SMS1242 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order bits of the address byte remain constant.

MEMORY OPERATION (Continued)

Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

Acknowledge Polling

When the SMS1242 is performing an internal WRITE operation it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete. See the flow diagram for the proper sequence of operations for polling.



2038 Flow01 2.0

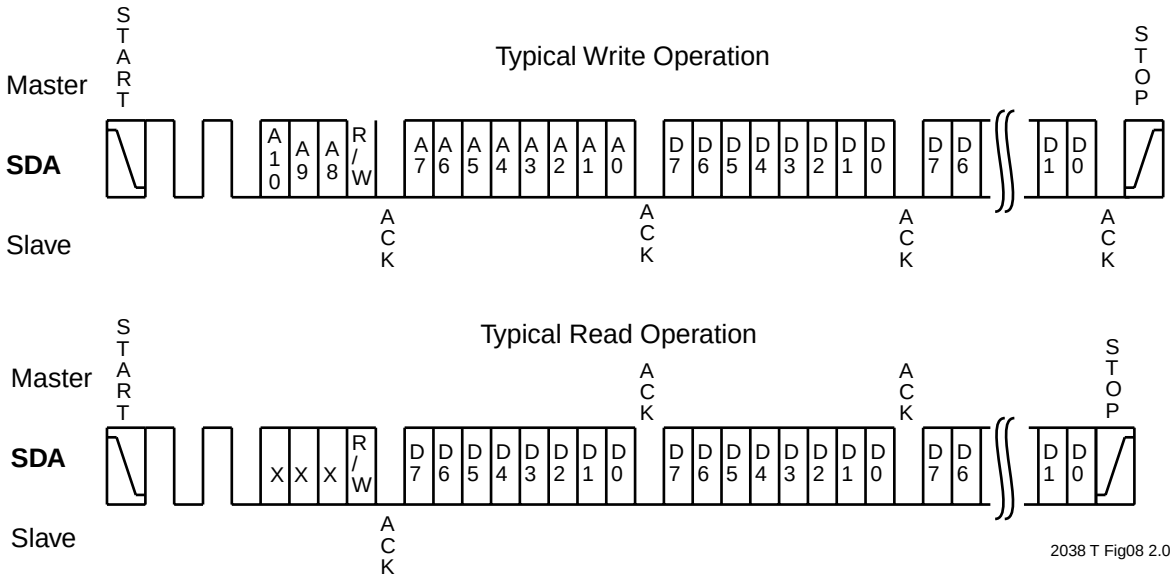
READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are two different read options:

1. Current Address Byte Read
2. Random Address Byte Read

Current Address Read

The SMS1242 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read



2038 T Fig08 2.0

Figure 8. Memory Operation

or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the SMS1242 receives the slave address field with the R/W bit set to "1" it issues an acknowledge and transmits the 8-bit word stored at address location n+1. The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS1242 discontinues data transmission.

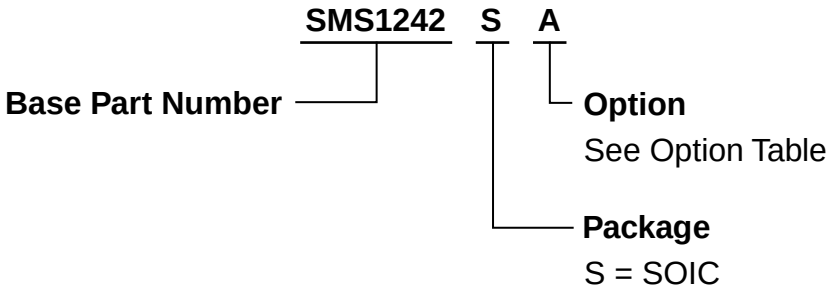
Random Address Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE), followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS1242 to the desired address. After the word address acknowledge is received by the master it immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMS1242 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The SMS1242 discontinues data transmission and reverts to its standby power mode.

Sequential READ

Sequential reads can be initiated as either a current address READ or a random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS1242. The SMS1242 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP condition. During a sequential read operation, the internal address counter is automatically incremented with each ACKnowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will roll-over, and the memory will continue to output data.

ORDERING INFORMATION



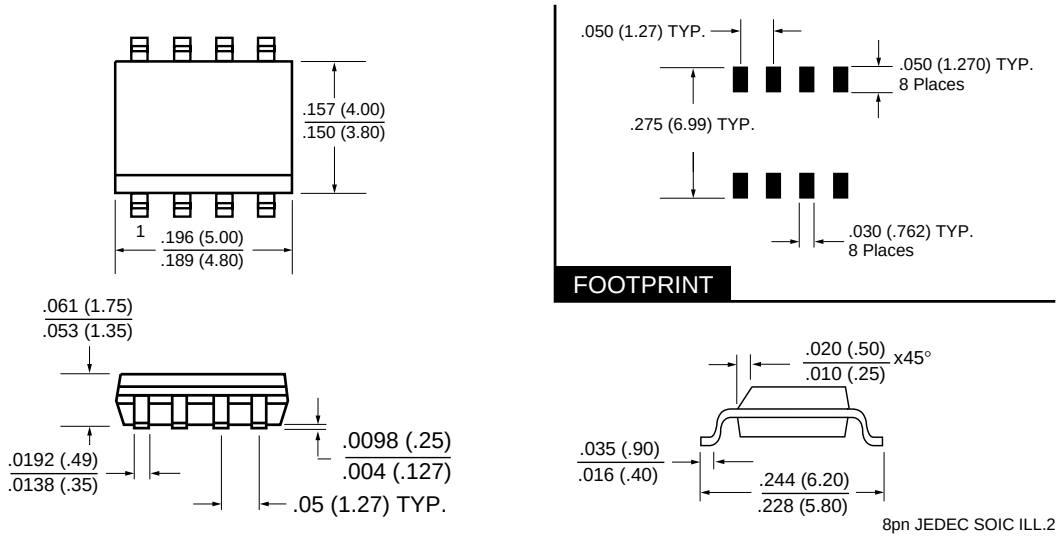
Part Number	Operating Voltage	V_{RST}	V_{SNS}	Operating Temperature Range	Lead Count & Package Style
SMS1242S-A	1V to 5.5V	4.425	1.25V	–40ºC to 85ºC	8 Pin SOIC
SMS1242S-B		4.475			
SMS1242S-C		4.676			
SMS1242S-D		4.450			
SMS1242S-E		2.650			
SMS1242S-F		2.950			
SMS1242S-*		PROG *			

2038 Option Table 2.0

Table 3. Order Options

PACKAGE

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



8pn JEDEC SOIC ILL.2