

TMS27C512 65536 BY 8-BIT UV ERASABLE TMS27PC512 65536 BY 8-BIT PROGRAMMABLE READ-ONLY MEMORIES

SMLS512G – NOVEMBER 1985 – REVISED SEPTEMBER 1997

description (continued)

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors.

The data outputs are 3-state for connecting multiple devices to a common bus. The TMS27C512 and the TMS27PC512 are pin compatible with 28-pin 512K MOS ROMs, PROMs, and EPROMs.

The TMS27C512 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27PC512 OTP PROM is supplied in a 32-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FM suffix).

The TMS27C512 and TMS27PC512 are offered with two choices of temperature ranges of 0°C to 70°C (JL and FML suffix) and – 40°C to 85°C (JE and FME suffix). See Table 1.

All package styles conform to JEDEC standards.

Table 1. Temperature Range Suffixes

| EPROM AND OTP PROM | SUFFIX FOR OPERATING FREE-AIR TEMPERATURE RANGES | |
|--------------------------|---|----------------|
| | 0°C TO 70°C | – 40°C TO 85°C |
| TMS27C512-xxx | JL | JE |
| TMS27PC512-xxx | FML | FME |

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. The device is programmed using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.



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operation

The seven modes of operation are listed in Table 2. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse) and 12 V on A9 for signature mode.

Table 2. Operation Modes

| FUNCTION | MODE† | | | | | | | |
|------------------|----------|----------------|----------|-------------|----------|-----------------|-------------------|--------|
| | READ | OUTPUT DISABLE | STANDBY | PROGRAMMING | VERIFY | PROGRAM INHIBIT | SIGNATURE MODE | |
| \bar{E} | V_{IL} | V_{IL} | V_{IH} | V_{IL} | V_{IL} | V_{IH} | V_{IL} | |
| \bar{G}/V_{PP} | V_{IL} | V_{IH} | X | V_{PP} | V_{IL} | V_{PP} | V_{IL} | |
| V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | |
| A9 | X | X | X | X | X | X | $V_H‡$ $V_H‡$ | |
| A0 | X | X | X | X | X | X | V_{IL} V_{IH} | |
| DQ0–DQ7 | Data Out | Hi-Z | Hi-Z | Data In | Data Out | Hi-Z | CODE | |
| | | | | | | | MFG | DEVICE |
| | | | | | | | 97 | 85 |

† X can be V_{IL} or V_{IH} .

‡ $V_H = 12 V \pm 0.5 V$.

read/output disable

When the outputs of two or more TMS27C512s or TMS27PC512s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the \bar{E} and \bar{G}/V_{PP} pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS27C512 and TMS27PC512 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL/CMOS signal to the \bar{E} pin. In this mode all outputs are in the high-impedance state.

erasure (TMS27C512)

Before programming, the TMS27C512 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 angstroms). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity \times exposure time) is 15-W·s/cm². A typical 12-mW/cm², filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C512, the window should be covered with an opaque label.



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initializing (TMS27PC512)

The one-time programmable TMS27PC512 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and OTP PROM are programmed using the TI SNAP! Pulse programming algorithm illustrated by the flowchart in Figure 1, which programs in a nominal time of seven seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100- μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved with $\overline{\text{G}}/V_{\text{PP}} = 13 \text{ V}$, $V_{\text{CC}} = 6.5 \text{ V}$, and $\overline{\text{E}} = V_{\text{IL}}$. Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{\text{E}}$ is pulsed.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{\text{CC}} = 5 \text{ V}$, $\overline{\text{G}}/V_{\text{PP}} = V_{\text{IL}}$, and $\overline{\text{E}} = V_{\text{IL}}$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{\text{E}}$ pin.

program verify

Programmed bits can be verified when $\overline{\text{G}}/V_{\text{PP}}$ and $\overline{\text{E}} = V_{\text{IL}}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. the signature code for these devices is 9785. A0 selects the manufacturer's code 97 (Hex), and A0 high selects the device code 85, as shown in Table 3.

Table 3. Signature Mode

| IDENTIFIER† | PINS | | | | | | | | | |
|-------------------|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | A0 | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 | HEX |
| Manufacturer Code | V_{IL} | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 97 |
| Device Code | V_{IH} | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 85 |

† $\overline{\text{E}} = \overline{\text{G}} = V_{\text{IL}}$, A9 = V_{H} , A1–A8 = V_{IL} , A10–A15 = V_{IL} , $\overline{\text{PGM}} = V_{\text{IH}}$ or V_{IL} .



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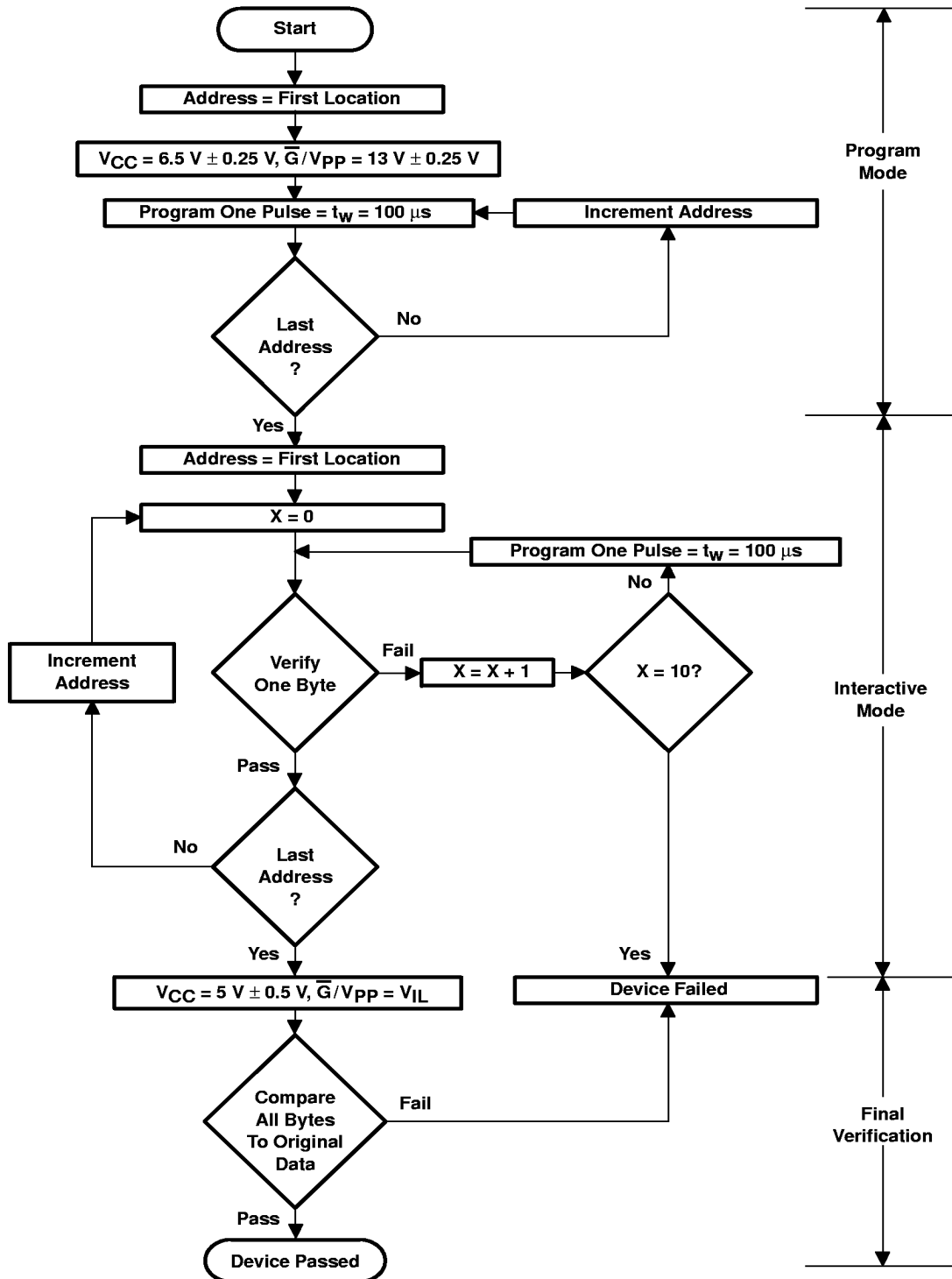


Figure 1. SNAP! Pulse Programming Flow Chart

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recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|-----------------------|--------------------------------|------------------------------------|-----------------------|--------------------|--------------------|------|
| V _{CC} | Supply voltage | Read mode (see Note 2) | 4.5 | 5 | 5.5 | V |
| | | SNAP! Pulse programming algorithm | 6.25 | 6.5 | 6.75 | |
| \overline{G}/V_{PP} | Supply voltage | SNAP! Pulse programming algorithm | 12.75 | 13 | 13.25 | V |
| V _{IH} | High-level dc input voltage | TTL | 2 | V _{CC} +1 | | V |
| | | CMOS | V _{CC} – 0.2 | | V _{CC} +1 | |
| V _{IL} | Low-level dc input voltage | TTL | – 0.5 | 0.8 | | V |
| | | CMOS | – 0.5 | 0.2 | | |
| T _A | Operating free-air temperature | TMS27C512-__JL TMS27PC512-__FML | 0 | 70 | | °C |
| T _A | Operating free-air temperature | TMS27C512-__JE TMS27PC512-__FME | – 40 | 85 | | °C |

NOTE 2: V_{CC} must be applied before or at the same time as \overline{G}/V_{PP} and removed after or at the same time as \overline{G}/V_{PP} . The device must not be inserted into or removed from the board when V_{pp} or V_{CC} is applied.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|---|---|---|------|-----|------|
| V _{OH} | High-level dc output voltage | I _{OH} = – 2.5 mA | 3.5 | | V | |
| | | I _{OH} = – 20 μA | V _{CC} – 0.1 | | | |
| V _{OL} | Low-level dc output voltage | I _{OL} = 2.1 mA | 0.4 | | V | |
| | | I _{OL} = 20 μA | 0.1 | | | |
| I _I | Input current (leakage) | V _I = 0 V to 5.5 V | ±1 | | μA | |
| I _O | Output current (leakage) | V _O = 0 V to V _{CC} | ±1 | | μA | |
| I _{PP} | \overline{G}/V_{PP} supply current (during program pulse) | \overline{G}/V_{PP} = 13 V | 35 50 | | mA | |
| I _{CC1} | V _{CC} supply current (standby) | TTL-input level | V _{CC} = 5.5 V, \overline{E} = V _{IH} | | μA | |
| | | CMOS-input level | V _{CC} = 5.5 V, \overline{E} = V _{CC} | | | |
| I _{CC2} | V _{CC} supply current (active) | V _{CC} = 5.5 V, \overline{E} = V _{IL} , t _{cycle} = minimum cycle time, outputs open | 15 30 | | mA | |

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|--------------------|---|--|-------|------|-----|------|
| C _I | Input capacitance | V _I = 0 V, f = 1 MHz | 6 10 | | pF | |
| C _O | Output capacitance | V _O = 0 V, f = 1 MHz | 10 14 | | pF | |
| C _{G/VPP} | \overline{G}/V_{PP} input capacitance | \overline{G}/V_{PP} = 0 V, f = 1 MHz | 20 25 | | pF | |

† Capacitance measurements are made on a sample basis only.

‡ Typical values are at T_A = 25°C and nominal voltages.



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switching characteristics over recommended ranges of operating conditions

| PARAMETER | TEST CONDITIONS (SEE NOTES 3 AND 4) | '27C512-10 '27PC512-10 | | '27C512-12 '27PC512-12 | | UNIT |
|--|---|---------------------------|-----|---------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{a(A)}$ Access time from address | $C_L = 100$ pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | 100 | | 120 | | ns |
| $t_{a(E)}$ Access time from chip enable | | 100 | | 120 | | ns |
| $t_{en(G)}$ Output enable time from \overline{G}/V_{PP} | | 55 | | 55 | | ns |
| t_{dis} Output disable time from \overline{G}/V_{PP} or \overline{E} , whichever occurs first† | | 0 | | 45 | | ns |
| $t_{v(A)}$ Output data valid time after change of address, \overline{E} , or \overline{G}/V_{PP} , whichever occurs first† | | 0 | | 0 | | ns |

| PARAMETER | TEST CONDITIONS (SEE NOTES 3 AND 4) | '27C512-15 '27PC512-15 | | UNIT | |
|--|---|---------------------------|-----|------|----|
| | | MIN | MAX | | |
| $t_{a(A)}$ Access time from address | $C_L = 100$ pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | 150 | | ns | |
| $t_{a(E)}$ Access time from chip enable | | 150 | | ns | |
| $t_{en(G)}$ Output enable time from \overline{G}/V_{PP} | | 75 | | ns | |
| t_{dis} Output disable time from \overline{G}/V_{PP} or \overline{E} , whichever occurs first† | | 0 | | 60 | ns |
| $t_{v(A)}$ Output data valid time after change of address, \overline{E} , or \overline{G}/V_{PP} , whichever occurs first† | | 0 | | 0 | ns |

| PARAMETER | TEST CONDITIONS (SEE NOTES 3 AND 4) | '27C512-20 '27PC512-20 | | '27C512-25 '27PC512-25 | | UNIT |
|--|---|---------------------------|-----|---------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{a(A)}$ Access time from address | $C_L = 100$ pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns | 200 | | 250 | | ns |
| $t_{a(E)}$ Access time from chip enable | | 200 | | 250 | | ns |
| $t_{en(G)}$ Output enable time from \overline{G}/V_{PP} | | 75 | | 100 | | ns |
| t_{dis} Output disable time from \overline{G}/V_{PP} or \overline{E} , whichever occurs first† | | 0 | | 60 | | ns |
| $t_{v(A)}$ Output data valid time after change of address, \overline{E} , or \overline{G}/V_{PP} , whichever occurs first† | | 0 | | 0 | | ns |

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled.

NOTES: 3. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (see Figure 2).

4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: $V_{CC} = 6.50$ V and $\overline{G}/V_{PP} = 13$ V (SNAP! Pulse), $T_A = 25^\circ\text{C}$ (see Note 3)

| PARAMETER | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{dis(G)}$ Disable time, output from \overline{G}/V_{PP} | 0 | 130 | ns |

NOTE 3: For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low.



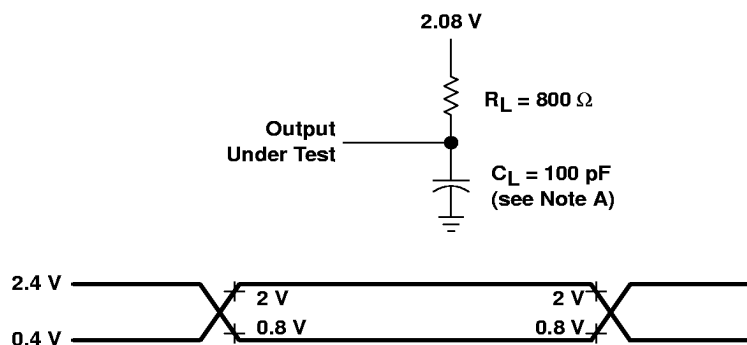
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timing requirements for programming

| | | MIN | NOM | MAX | UNIT |
|-----------------------------|---|-----|-----|-----|---------------|
| $t_w(\text{IPGM})$ | Pulse duration, initial program | 95 | 100 | 105 | μs |
| $t_{\text{su}}(\text{A})$ | Setup time, address | 2 | | | μs |
| $t_{\text{su}}(\text{D})$ | Setup time, data | 2 | | | μs |
| $t_{\text{su}}(\text{VPP})$ | Setup time, $\overline{\text{G}}/\text{VPP}$ | 2 | | | μs |
| $t_{\text{su}}(\text{VCC})$ | Setup time, VCC | 2 | | | μs |
| $t_{\text{h}}(\text{A})$ | Hold time, address | 0 | | | μs |
| $t_{\text{h}}(\text{D})$ | Hold time, data | 2 | | | μs |
| $t_{\text{h}}(\text{VPP})$ | Hold time, $\overline{\text{G}}/\text{VPP}$ | 2 | | | μs |
| $t_{\text{rec}}(\text{PG})$ | Recovery time, $\overline{\text{G}}/\text{VPP}$ | 2 | | | μs |
| t_{EHD} | Data valid from $\overline{\text{E}}$ low | | | 1 | μs |
| $t_r(\text{PG})\text{G}$ | Rise time, $\overline{\text{G}}/\text{VPP}$ | 50 | | | ns |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and fixture capacitance.
 B. The ac testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

Figure 2. AC Testing Output Load Circuit

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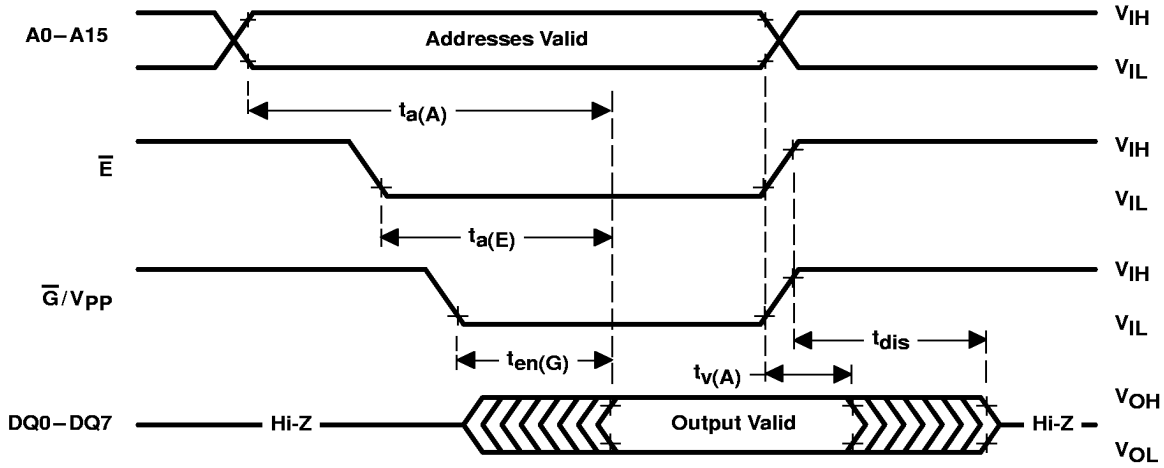
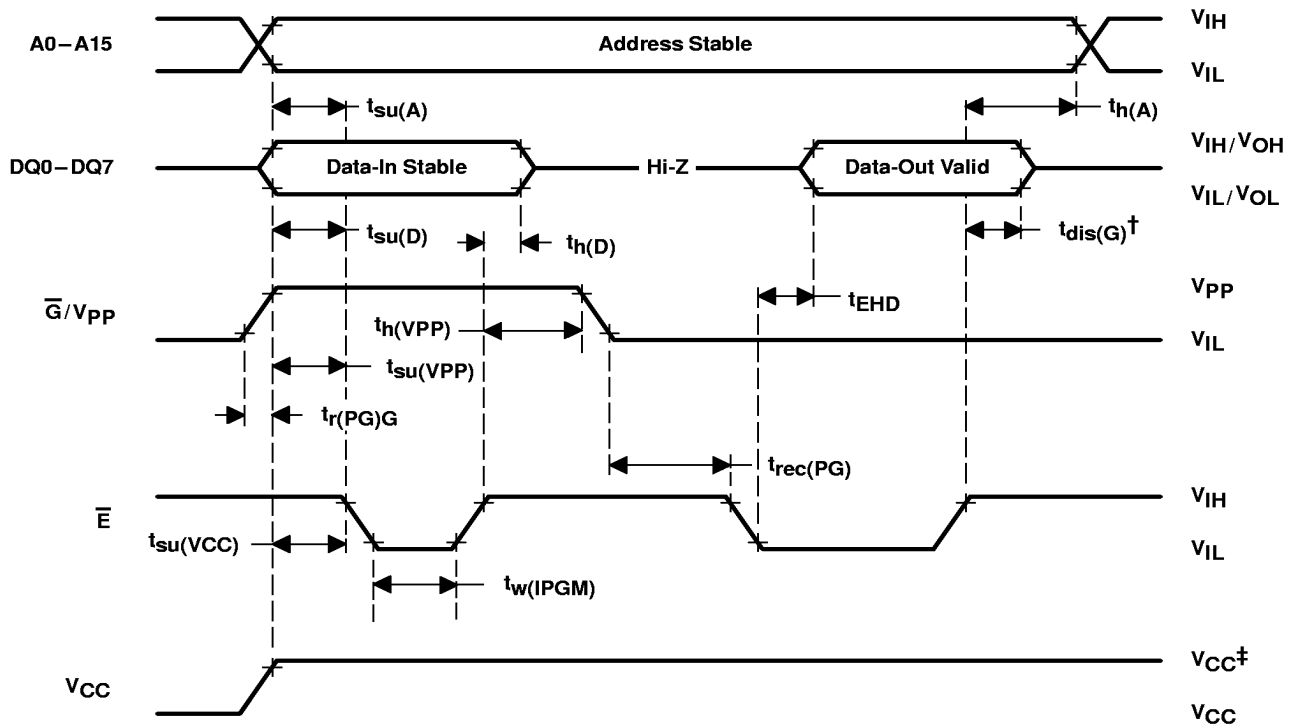


Figure 3. Read-Cycle Timing



$^{\dagger} t_{dis(G)}$ is a characteristic of the device but must be accommodated by the programmer.

$^{\ddagger} 13\text{-V } \bar{G}/V_{pp}$ and $6.5\text{-V } V_{CC}$ for SNAP! Pulse programming.

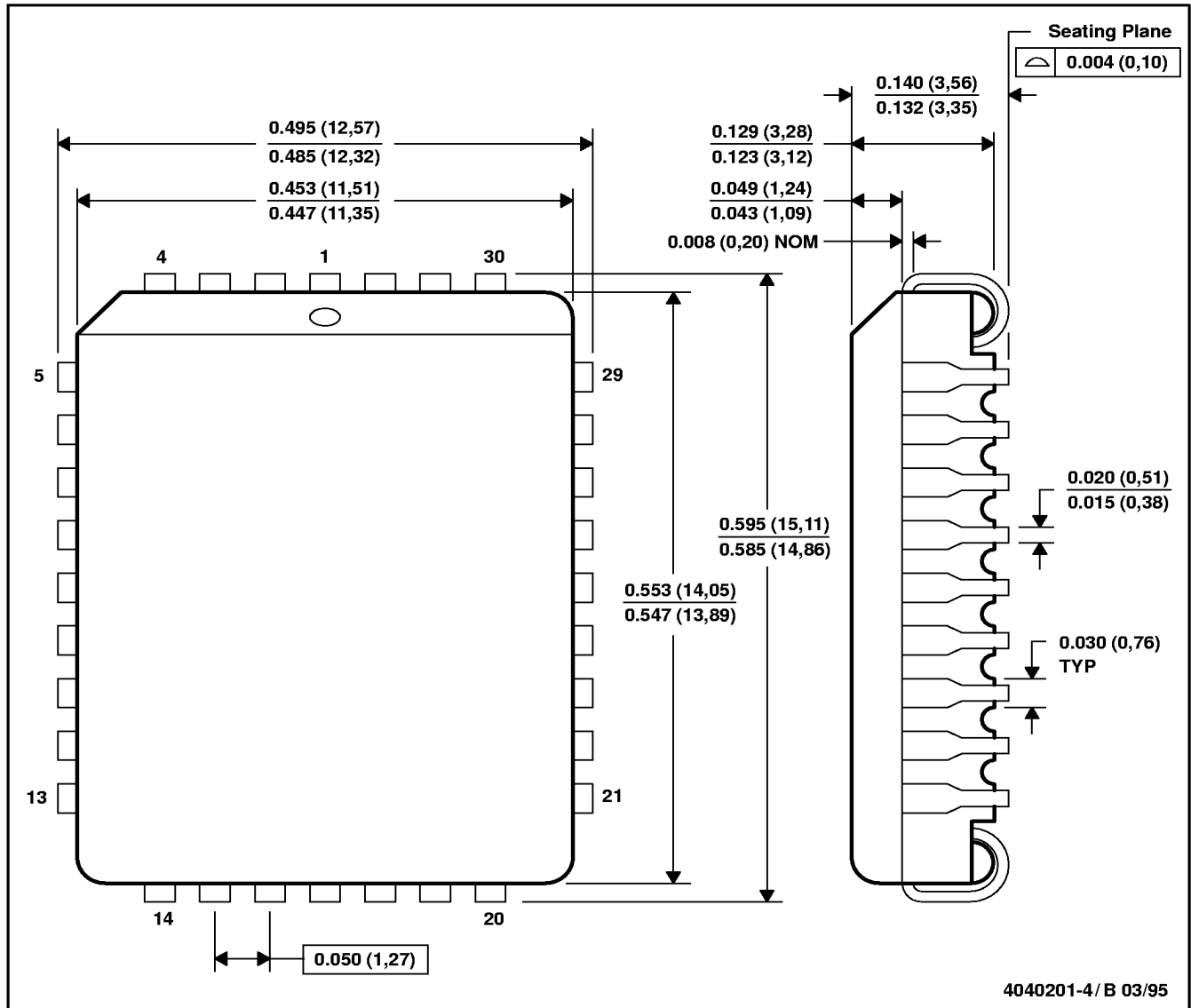
Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

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FM (R-PQCC-J32)

PLASTIC J-LEADED CHIP CARRIER



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-016

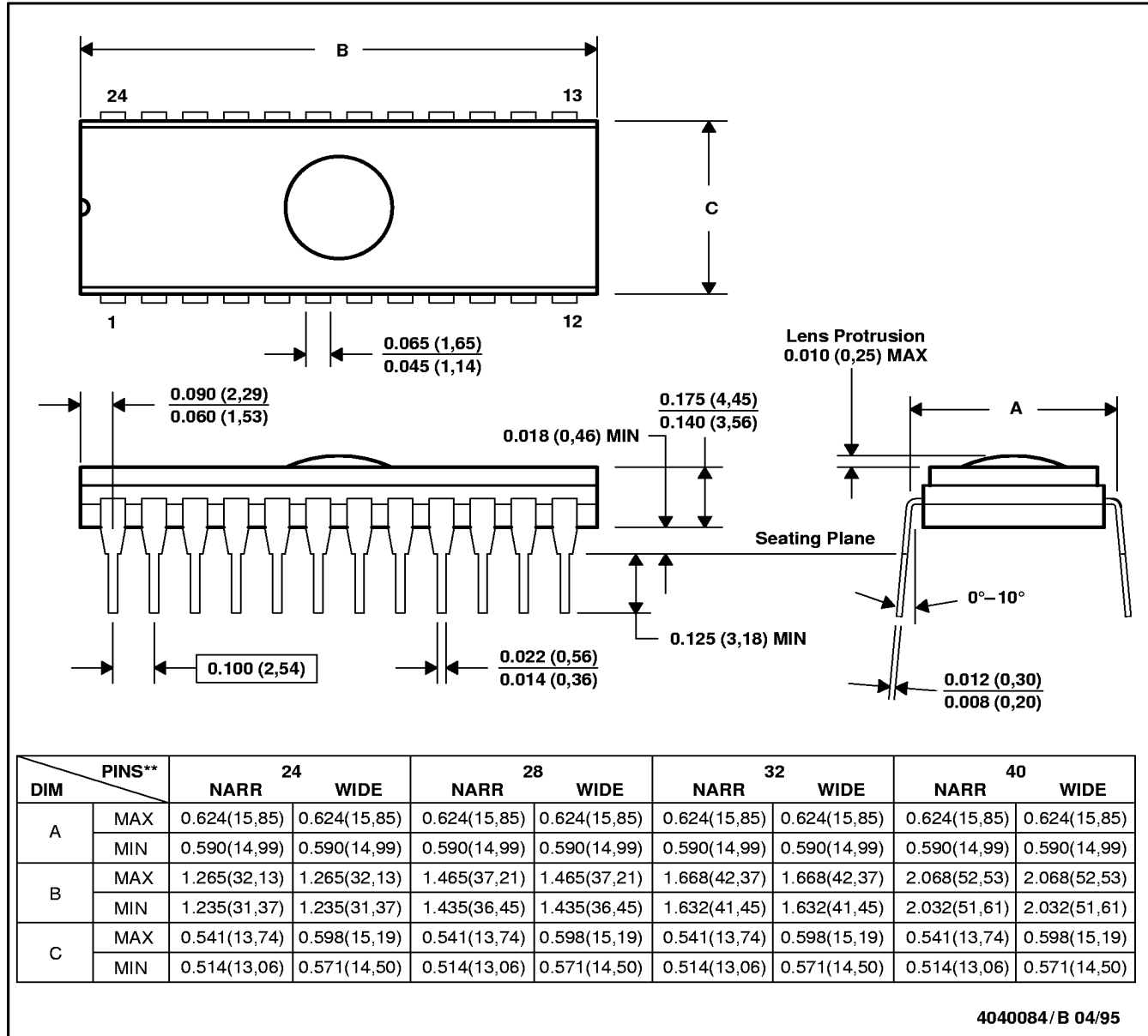
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J (R-CDIP-T)**

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

