



SLVDA2.8LC

ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Ethernet - 10/100/1000 Base T
- ✓ Cellular Phone Base Stations
- ✓ Switching Stations
- ✓ Audio/Video Inputs
- ✓ Handheld Devices

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20µs - Level 2(Line-Ground) & Level 3(Line-Line)

FEATURES

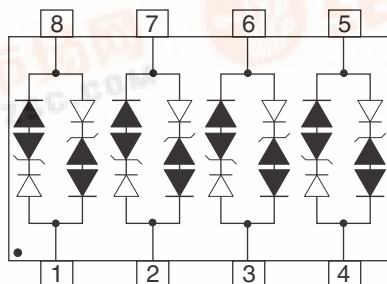
- ✓ 600 Watts Peak Pulse Power per Line (tp = 8/20µs)
- ✓ Provides Protection for Four (4) Line Pairs
- ✓ **LOW LEAKAGE CURRENT < 1.0µA**
- ✓ **ULTRA LOW CAPACITANCE: 1.25pF**
- ✓ RoHS Compliant in Lead-Free Versions

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8
- ✓ Weight 70 milligrams (Approximate)
- ✓ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
 - Tin-Lead - Sn/Pb, 85/15: 240-245°C
 - Pure-Tin - Sn, 100: 260-270°C
- ✓ Flammability Rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Device Marking: Marking Code, Logo, Date Code & Pin One Defined By DOT on Package



PIN CONFIGURATION



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	600	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	30	A
Lead Soldering Temperature	T_{\parallel}	260°C (10 Sec)	°C
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified

PART NUMBER	DEVICE MARKING CODE	RATED STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE	MINIMUM SNAP BACK VOLTAGE	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Fig. 42)	MAXIMUM LEAKAGE CURRENT	TYPICAL CAPACITANCE
		V_{WM} VOLTS	@ 1mA $V_{(BR)}$ VOLTS	@ $I_{SB} = 50mA$ V_{SB} VOLTS	@ $I_P = 1A$ V_C VOLTS	@ $I_P = 5A$ V_C VOLTS	@ 8/20 μs $V_C @ I_{PP}$	@ V_{WM} I_D μA	@ 0V, 1MHz C pF
SLVDA2.8LC	LV2.8	2.8	3.0	2.8	4.6	6.2	21.0V@30.0A	1.0	5

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

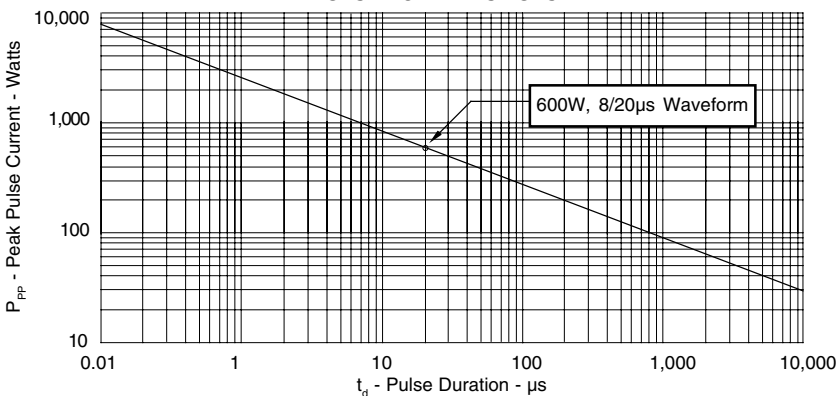
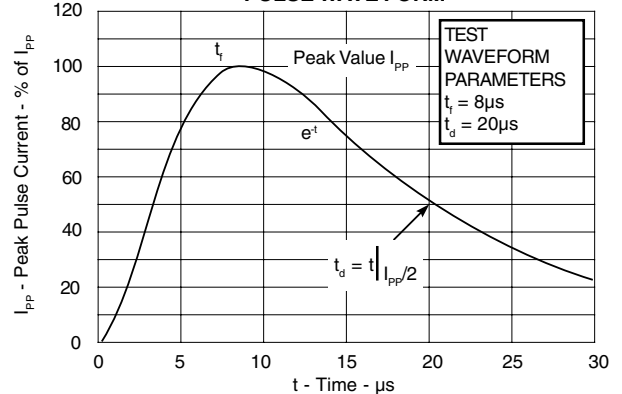
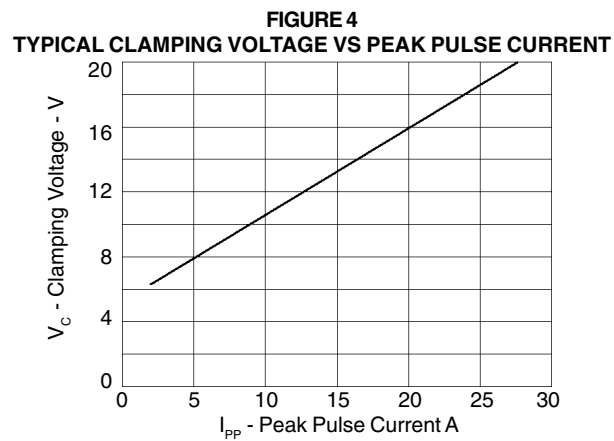
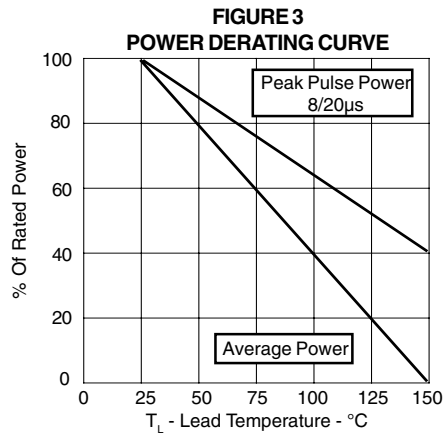


FIGURE 2
PULSE WAVEFORM



GRAPHS



APPLICATION NOTE

Electronic equipment is susceptible to damage caused by Electrostatic Discharge (ESD), Electrical Fast Transients (EFT), and tertiary lightning effects. Knowing that equipment can be damaged, the SLVDA2.8LC was designed to provide the level of protection required to safe guard sensitive high speed data circuits. This product can be used to provide a level of protection to meet bidirectional requirements either in a common-mode or differential-mode configuration.

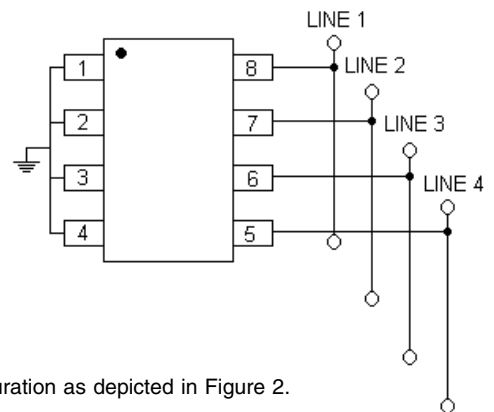
BIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

The SLVDA2.8LC can provide up to four (4) lines of protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to pin 8
- ✓ Line 2 is connected to pin 7
- ✓ Line 3 is connected to pin 6
- ✓ Line 4 is connected to pin 5
- ✓ Pins 1, 2, 3, and 4 are connected to ground

Figure 1: Bidirectional Common-Mode Protection



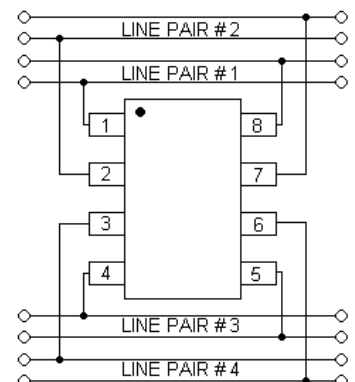
BIDIRECTIONAL DIFFERENTIAL-MODE CONFIGURATION (Figure 2)

The SLVDA2.8LC can provide up to four line pairs (4) of protection in a differential-mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ Line Pair # 1 is connected to pin 8 and 1
- ✓ Line Pair # 2 is connected to pin 7 and 2
- ✓ Line Pair # 3 is connected to pin 5 and 4
- ✓ Line Pair # 4 is connected to pin 6 and 3

Figure 2: Bidirectional Differential-Mode Protection



CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

PACKAGE OUTLINE & DIMENSIONS

