Silicon Image

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Technology

SiI 1160
PanelLink Transmitter

Data Sheet

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Application Information

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Revision History

Revision	Date	Comment
A	07/07/04	Data Sheet – 1st release
B	03/01/05	Data Sheet – 2nd release – added I^2C registers and pins, added dual zone PLL information, corrected recommended R_{EXT_SWING} value from 380Ω to 510Ω, corrected package JEDEC code, added reset description.

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General Description

The SiI 1160 transmitter uses PanelLink Digital technology to support displays up to UXGA resolution. It supports up to true-color panels (24 bits per pixel, 16.7M colors) in 1 or 2 pixels-per-clock mode.

All PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface. The SiI 1160 transmitter follows this strategy by offering a pin-compatible upgrade to the SiI 160 transmitter that also brings longer cable support.

PanelLink Digital technology simplifies the PC & display interface by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital solution that is quicker to market and lower in cost.

Features

- Scaleable Bandwidth: 25-165 MHz (VGA to UXGA)
- Backwards compatible replacement for the SiI 160 transmitter
- High Skew Inter pair Tolerance: 1 full input clock cycle (6ns at 165 MHz)
- Flexible interface: single or dual pixel input at up to 48 bits
- Cable Distance Support: over 20m DVI cable
- Fully DVI 1.0 compliant
- Advanced on-chip input clock jitter filter to ensure clean output to receiver
- Available in Universal package for both standard and Pb-Free (environmentally-friendly) applications.

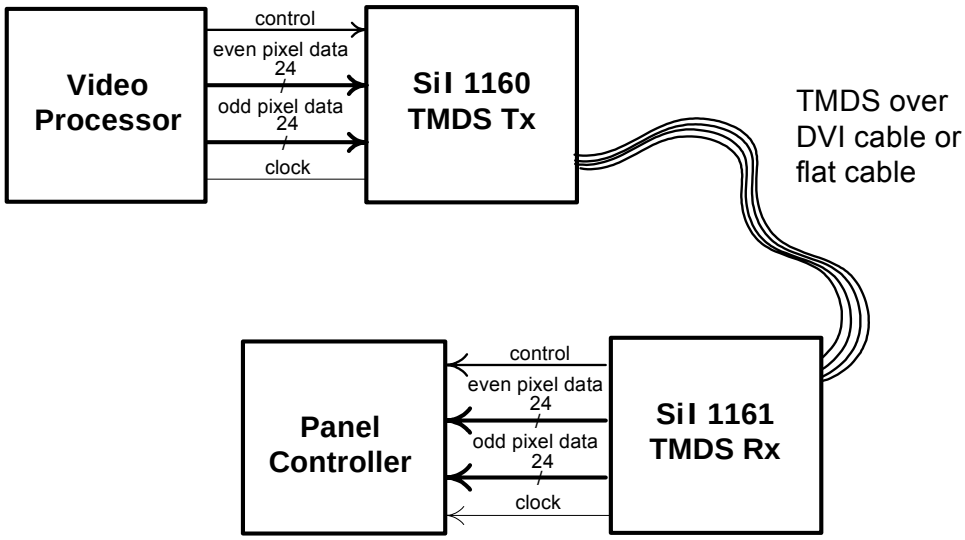


Figure 1. System Block Diagram – Typical Application

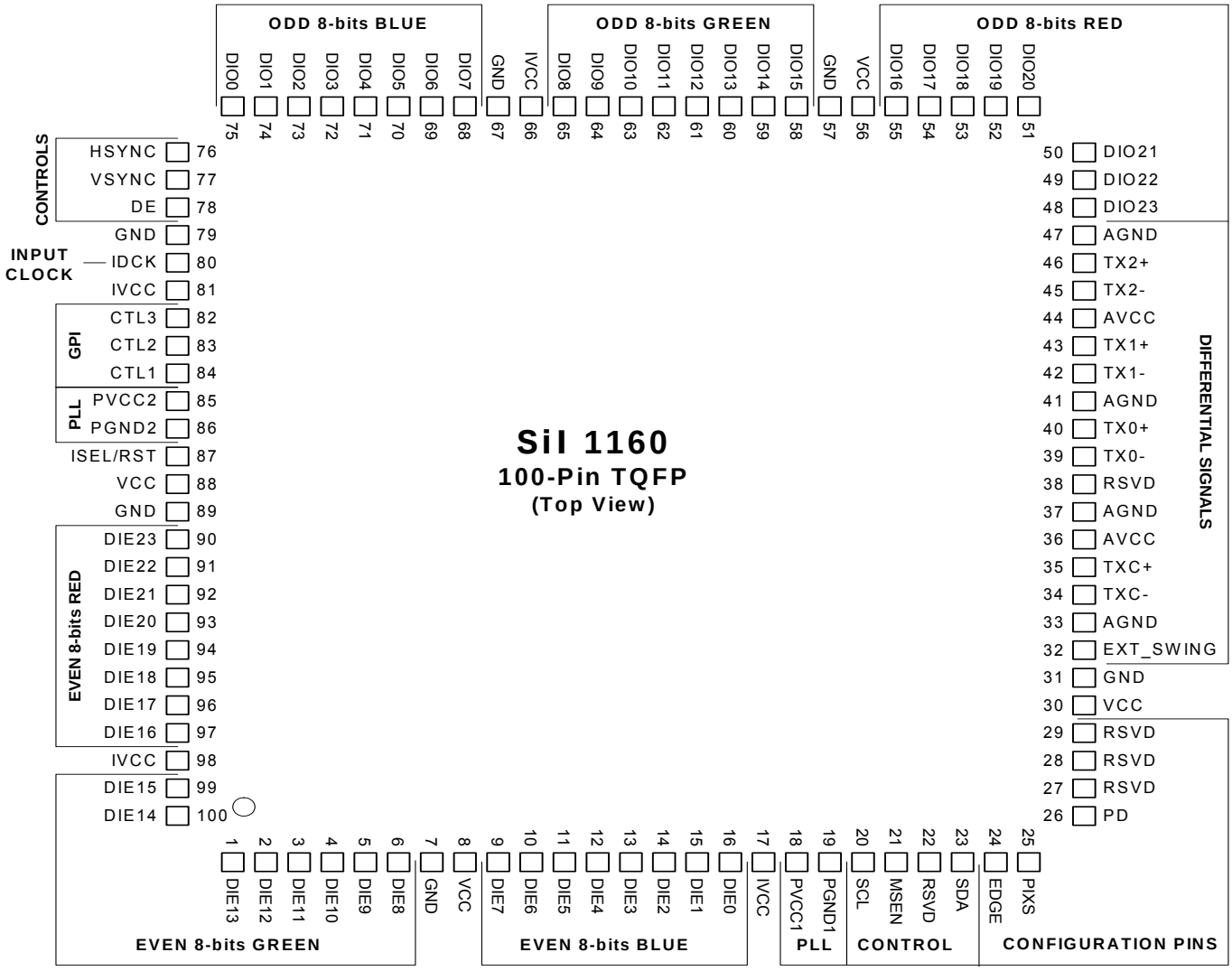


Figure 2. Pin Diagram for SiI 1160

Functional Description

The SiI 1160 Tx is a DVI 1.0 compliant PanelLink transmitter in a compact package. It provides 48 bits for data input to allow for panel support up to UXGA. Figure 3 shows the functional blocks of the chip.

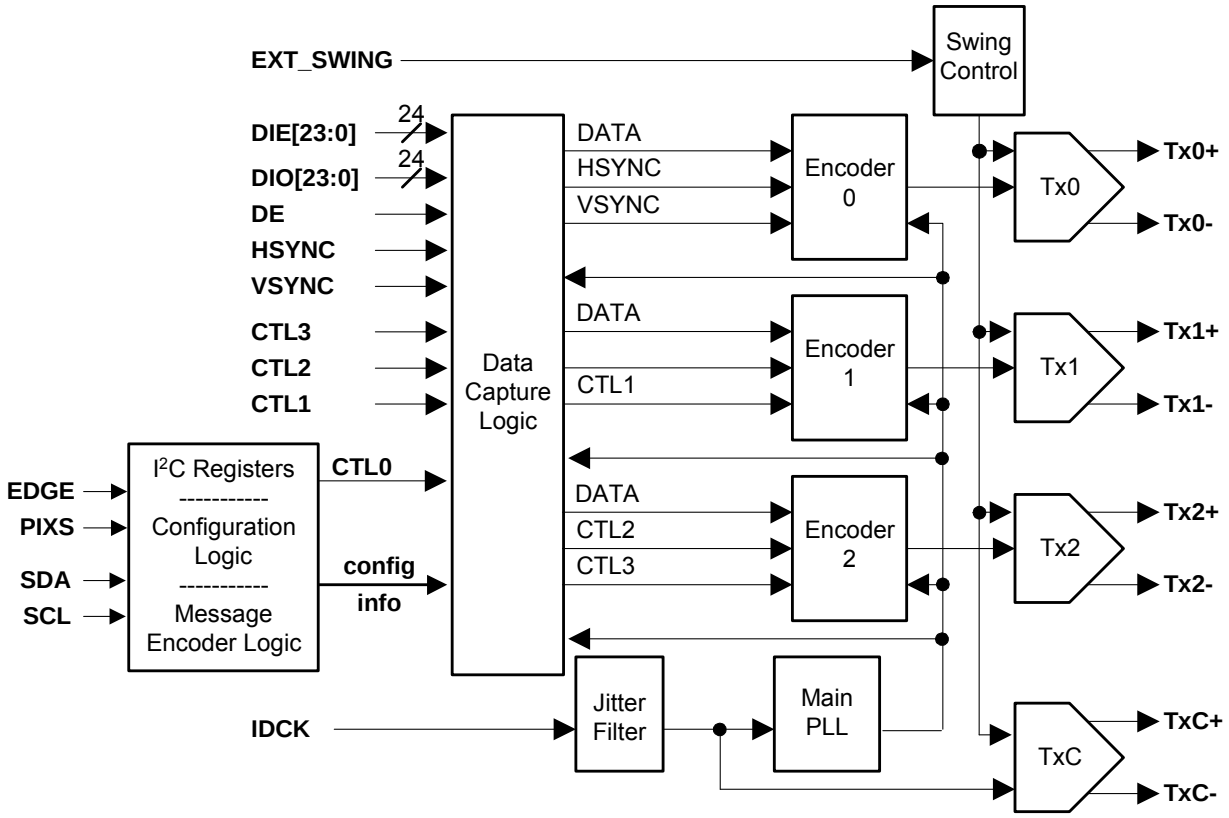


Figure 3. Functional Block Diagram

Electrical Specifications

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}[1]	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O[2]	Input Voltage	-0.3		V_{CC}+ 0.3	V
T_j	Junction Temperature (with power applied)			125	°C
T_{STG}	Storage Temperature	-65		150	°C

Note
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under normal operating conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C
θ_{JA}	Thermal Resistance (junction to ambient)[1]			53	°C/W

Note
1. Airflow at 0m/s.

Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Input Voltage		2.4			V
V_{OL}	Low-level Input Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{OL}	Input Leakage Current	High Impedance	-10		10	µA

Note
1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3 ns or one third of the clock cycle.

DC Specifications

Under normal operating conditions, with R_{EXT_SWING} = 510Ω and using source termination, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50Ω	510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]			AVCC		V
I_{DOS}	Differential Output Short Circuit Current[1]	V_{OUT} = 0 V			5	µA
I_{PD}	Power-down Current[2]				5	mA
I_{CCT}	Transmitter Supply Current	IDCK= 165 MHz, two pixel per clock mode IVCC = VCC, Worst Case Pattern[3]		140	200	mA

Notes
1. Guaranteed by design.
2. Assumes all inputs to the transmitter are not toggling.
3. The Worst Case Pattern consists of a black and white checkerboard pattern, each checker one pixel wide.

AC Specifications

Under normal operating conditions with source termination and the recommended R_{EXT_SWING} value unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
T_{CIP}	IDCK Period, 1 Pixel/Clock		6	40	ns
F_{CIP}	IDCK Frequency, 1 Pixel/Clock		25	165	MHz
T_{CIP}	IDCK Period, 2 Pixels/Clock		12	80	ns
F_{CIP}	IDCK Frequency, 2 Pixels/Clock		12	81	MHz
T_{CIH}	IDCK High Time at 165MHz		2		ns
T_{CIL}	IDCK Low Time at 165MHz		2		ns
T_{SIDF}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to IDCK falling edge	EDGE = 0	1.5		ns
T_{HIDF}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from IDCK falling edge	EDGE = 0	1.5		ns
T_{SIDR}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to IDCK rising edge	EDGE = 1	1.5		ns
T_{HIDR}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from IDCK rising edge	EDGE = 1	1.5		ns
T_{DDF}	VSYNC, HSYNC, and CTL[3:1] Delay from DE falling edge[1]		T_{CIP}		ns
T_{DDR}	VSYNC, HSYNC, and CTL[3:1] Delay to DE rising edge[1]		T_{CIP}		ns
T_{HDE}	DE high time[1]			$8191T_{CIP}$	ns
T_{LDE}	DE low time[1]		$128T_{CIP}$		ns
T_{I2CDVD}	SDA Data Valid Delay from SCL high to low transition	C_L = 400pf		1000	ns
T_{RESET}	ISEL/RST Signal High Time required for valid I^2C reset		50		µs

Notes
1. Guaranteed by design.
2. All TMDS signaling is guaranteed to meet the DVI 1.0 specifications.
3. All Standard mode I^2C (100kHz and 400kHz) timing requirements are guaranteed by design.

Input Timing Diagrams

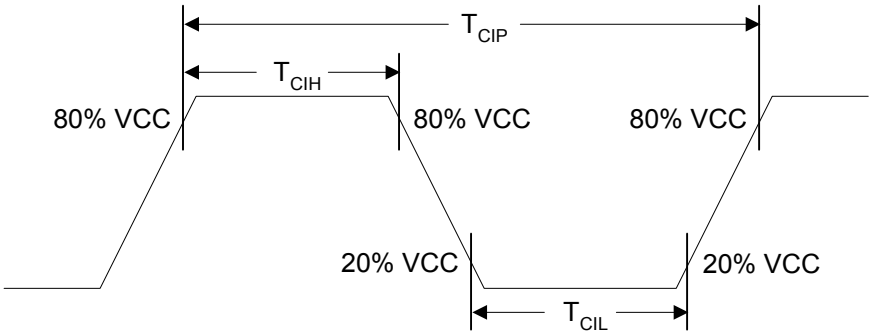


Figure 4. Clock Cycle High/Low Times

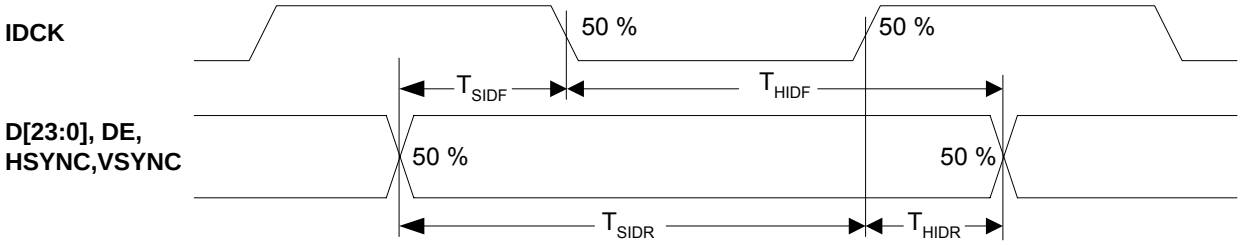


Figure 5. Input Data Setup/Hold Time to IDCK

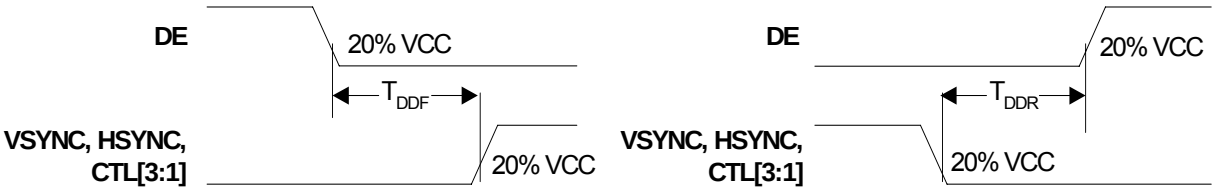


Figure 6. VSYNC, HSYNC and CTL[3:1] Delay Time from DE

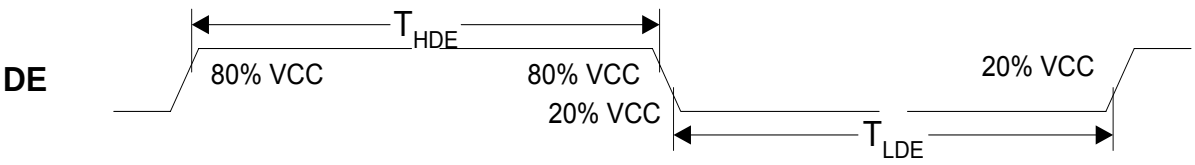


Figure 7. DE High and Low Times

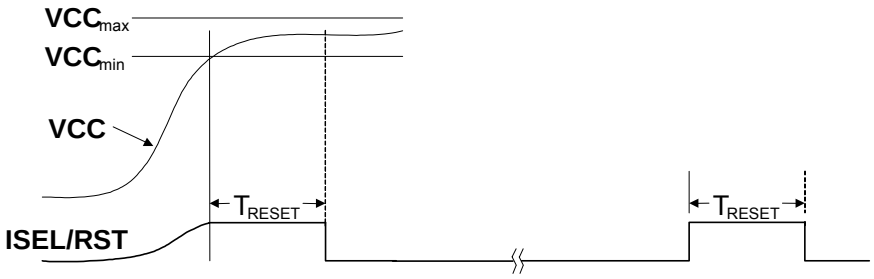


Figure 8. Reset Timing at Power-Up or Prior to First I^2C Access

Pin Descriptions

Input Pins

Pin Name	Pin #	Type	Description
DIE23- DIE0	See SiI 1160 Pin Diagram	In	Input Even Data[23:0] corresponds to 24-bit pixel data for 1-pixel/clock input mode and to the first 24-bit pixel data for 2-pixels/clock mode. Input data is synchronized with Input data clock (IDCK). Data can be latched on the rising of the falling edge of IDCK depending on whether EDGE is high or low, respectively. Refer to TFT Panel Data Mapping in this document and DSTN Panel Data Mapping application note (SiI-AN-0007-A), which tabulates the relationship between the input data to the transmitter and output data from the Receiver
DIO23- DIO0	See SiI 1160 Pin Diagram	In	Input Odd Data[23:0] corresponds to the second 24-bit pixel data for 2-pixels/clock mode. Tie all pins to low when not in use. Input data is synchronized with Input data clock (IDCK). Data can be latched on the rising of the falling edge of IDCK depending on whether EDGE is high or low, respectively. Dual Link is not supported.
IDCK	80	In	Input Data Clock. Input data and control signals can be valid either on the falling or the rising edge of IDCK as selected by the EDGE pin.
DE	78	In	Input Data Enable. This signal qualifies the active data area. DE is always required by the transmitter and must be high during active display time and low during blanking time.
HSYNC VSYNC	76 77	In In	Horizontal Sync input control signal. Vertical Sync input control signal.

Control and Configuration Pins

Pin Name	Pin #	Type	Description
EDGE	24	In	Data/Control Latching Edge. A LOW level indicates that all input signals(DIE/DIO[23:0], HSYNC, VSYNC, DE and CTL[3:1] are latched on the falling edge of IDCK, while a HIGH level(3.3V) indicates that all input signals are latched on the rising edge of IDCK. When the I^2C interface is enabled (ISEL/RST=LOW), this pin is ignored and the EDGE register bit is used instead.
PIXS	25	In	Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using DIE[23:0]. A HIGH level (3.3V) indicates two pixels (up to 48-bits) per clock mode using DIE[23:0] for the first pixel and DIO[23:0] for the second pixel.
CTL1	84	In	General Input control signal 1.
SS_CLK_IN			Spread Spectrum Clock Input (future). A planned future variation of this device will allow a spread spectrum version of SS_CLK_OUT to be driven into this pin, at which time pin 29 will become CTL1.
CTL2	83	In	General Input control signal 2.
SS_CLK_OUT		Out	Spread Spectrum Clock Output (future). A planned future variation of this device will allow a clock to be driven out of this pin for conditioning by a spread spectrum device, at which time pin 28 will become CTL2.
CTL3	82	In	General Input control signal 3.
RSVD	27	In	Reserved. Must be tied **HIGH** for normal operation.
SS_EN#			Spread Spectrum Enable. A planned future variation of this device will use this pin to enable pins 83 and 84 to handle spread spectrum clock. Low = Spread Spectrum feature enabled on pins 83 and 84 High = Pins 83 and 84 are CTL2 and CTL1 outputs (default)

Power Management Pins

Pin Name	Pin #	Type	Description
PD	26	In	Power Down (active LOW). A HIGH level indicates normal operation. A LOW level indicates power down mode. During power down mode, all data (DIE/DIO[23:0]), data enable (DE), clock (IDCK) and control signals (HSYNC, VSYNC, CTL[3:1]), input buffers are disabled, all output buffers are tri-stated and all internal circuitry is powered down. When the I^2C interface is enabled (ISEL/RST=LOW), this pin is ignored and the PD register bit is used instead. Tie this pin low if not used.

Differential Signal Data Pins

Pin Name	Pin #	Type	Description
TX0+	40	Analog	TMDS Low Voltage Differential Signal input data pairs.
TX0-	39	Analog	
TX1+	43	Analog	These pins are tri-stated when PD is asserted.
TX1-	42	Analog	
TX2+	46	Analog	
TX2-	45	Analog	
TXC+	35	Analog	TMDS Low Voltage Differential Signal input clock pair.
TXC-	34	Analog	These pins are tri-stated when PD is asserted.
EXT_SWING	32	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. This resistor determines the amplitude of the voltage swing. A smaller resistor value sets a larger voltage swing and vice versa. For remote display applications with source termination, a 510Ω resistor is recommended (see page 24). Without the source termination, use a 560Ω resistor.

Local Control (I^2C) Interface

The transmitter can operate with or without an I^2C interface connection. Refer to the Feature Information section for details on using the I^2C registers.

Pin Name	Pin #	Type	Description
ISEL/RST	87	In	I^2C Interface Select. If LOW, then the I^2C interface is active. If HIGH, the interface is inactive and chip configuration is taken from strap and default settings. This pin also acts as an asynchronous reset to the I^2C interface controller. Switching this input from HIGH to LOW after a minimum T_{RESET} high time resets the I^2C logic.
MSEN	21	Out	Monitor Sense. The behavior of this output depends on whether the I^2C interface is enabled or disabled. No I^2C (ISEL = HIGH) MSEN=HIGH: a powered on receiver is detected at the TMDS outputs. MSEN=LOW: a powered on receiver is not detected. This Receiver Sense function can only be used in DC-coupled systems. I^2C enabled (ISEL = LOW) The output is programmable through the I^2C interface and can indicate the Hot Plug or Receiver Sense signal state, or can instead generate a status change interrupt for those signals. This pin is an open collector output. An external pull-up resistor (5KΩ recommended) is required on this pin if the MSEN signal will be used. Otherwise the signal should be tied low.
SCL	20	In	I^2C Clock. When the I^2C interface is enabled (ISEL=LOW), this pin acts as the I^2C clock input. This pin is an open collector output. It must be pulled high to VCC through a resistor; a value of 2.2KΩ is recommended for I^2C applications, 2-5KΩ otherwise. This pin is not 5V-tolerant.
SDA	23	In/Out	I^2C Data. When the I^2C interface is enabled (ISEL=LOW), this pin acts as the I^2C data input and output. This pin is an open collector output. It must be pulled high to VCC through a resistor; a value of 2.2KΩ is recommended for I^2C applications, 2-5KΩ otherwise. This pin is not 5V-tolerant.

Reserved Pins

It is preferable to tie indicated pins HIGH through a 2-5KΩ resistor; direct connection to VCC is not recommended.

Pin Name	Pin #	Type	Description
RSVD	22	In	Reserved. Must be tied **HIGH** for normal operation.
RSVD	28	In	Reserved. Must be tied **HIGH** for normal operation.
RSVD	29	In	Reserved. Must be tied **HIGH** for normal operation.
RSVD	38	--	Reserved. Should be left unconnected (but can be tied to AVCC for existing SiI 160 designs).

Power and Ground Pins

Pin Name	Pin #	Type	Description
VCC	8,30,56,88	Power	Digital Core VCC, must be set to 3.3V.
GND	7,31,57,67,79,89	Ground	Digital Core GND.
IVCC	17,66,81,98	Power	Input VCC, must be set to 3.3V.
AVCC	36,44	Power	Analog VCC must be set to 3.3V.
AGND	33,37,41,47	Ground	Analog GND.
PVCC1	18	Power	Primary PLL Analog VCC must be set to 3.3V.
PVCC2	85	Power	Filter PLL Analog VCC must be set to 3.3V.
PGND1	19	Ground	PLL Analog GND. PGND1 should not be directly connected to PGND2 before being connected to the GROUND plane. They should be connected individually to the GROUND plane.
PGND2	86	Ground	PLL Analog GND. PGND2 should not be directly connected to PGND1 before being connected to the GROUND plane. They should be connected individually to the GROUND plane.

Feature Information

I²C Interface

The SiI 1160 Tx provides an I²C slave interface for more precise control of the chip features. Use of this interface is optional and is selected by the ISEL/RST pin. If not used, the chip register settings return to a default state; the EDGE and PD features then come under the control of the respective strap pins instead.

The I²C slave state machine operates from an internal clock derived from the incoming SCL signal. No video clock and input is required to read and write to the I²C registers from address 0x00 to 0x0F. These accesses can also take place using only the SCL clock in power down mode.

The transmitter responds to the seven-bit binary I²C address of 0x70. A read or write transaction is determined by bit 0 of the I²C address. Setting this bit to 0 will enable a write transaction and setting this bit to 1 will enable a read transaction.

The I²C read operation is shown in Figure 9, and the write operation in Figure 10. Page mode is not supported.

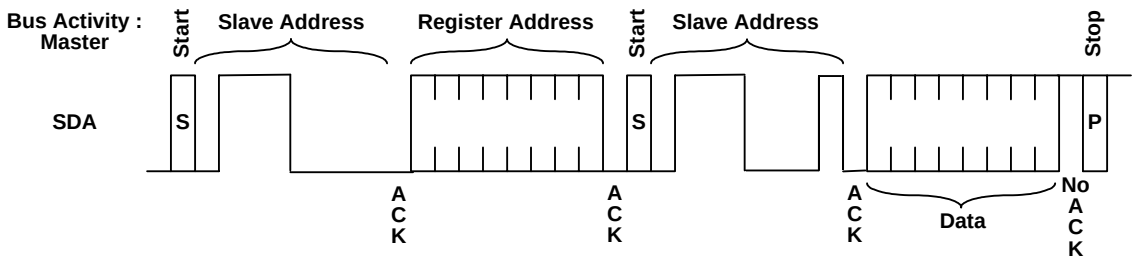


Figure 9. I²C Byte Read

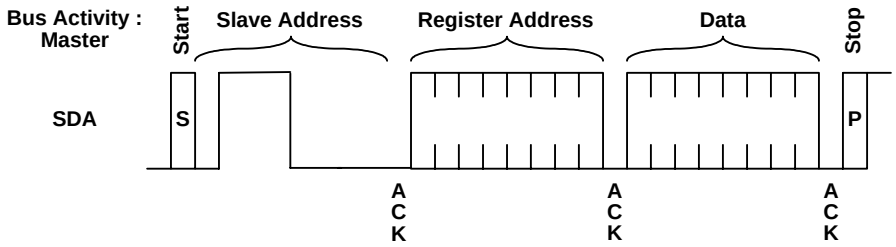


Figure 10. I²C Byte Write

I²C Register Mapping

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value	Notes
0x0	VND_IDL								0x01	
0x1	VND_IDH								0x00	
0x2	DEV_IDL								0x06	
0x3	DEV_IDH								0x00	
0x4	DEV_REV								0x00	
0x5	RSVD									4
0x6	FRQ_LOW								0x19	
0x7	FRQ_HIGH								0x64	
0x8	RSVD write to 00		VEN	HEN	RSVD write to 01		EDGE	PD	00110100	3, 5, 6
0x9	RSVD					RSEN	RSVD		read only	
0xA	RSVD write to 1000000							CTL0	10000001	5, 6
0xB-0xD	RSVD									4
0xE	RSVD write to 00		EZONE	ZONEF	ZONEO	RSVD write to 001			00000001	
0xF	RSVD									4

Notes:

1. Hexadecimal values use a prefix of '0x'. All values use bit 7 as most significant, bit 0 as least significant.
2. Read-only or read/write capabilities are noted on the next page.
3. On any reset assertion event, registers that have default values lose their previously programmed value and are set back to the default values listed.
4. Registers listed as RSVD and shaded gray are reserved for factory use and should not be accessed.
5. Write RSVD bits to the values indicated when writing other bits in the register.
6. Write PD to 1 for normal operation; write CTL0 to 0 for HDMI applications.

Table 1. General I²C Register Bits

Register Name	Access	Description
VND_IDL	RO	Vendor ID Low byte (0x01)
VND_IDH	RO	Vendor ID High byte (0x00)
DEV_IDL	RO	Device ID Low byte (0x06)
DEV_IDH	RO	Device ID High byte (0x00)
DEV_REV	RO	Device Revision (0x00)
FRQ_LOW	RO	IDCK. Low frequency limit is 25MHz. (0x19)
FRQ_HIGH	RO	IDCK High frequency limit is 165MHz. Value is offset over 65MHz. (0x64)
HEN	RW	Horizontal Sync Enable 0 – HSYNC input is transmitted as fixed LOW 1 – HSYNC input is transmitted as input. → Default
VEN	RW	Vertical Sync Enable 0 – VSYNC input is transmitted as fixed LOW 1 – VSYNC input is transmitted as input. → Default
EDGE	RW	Edge Select (same function as EDGE pin) 0 – Input data low order bits latched first → Default 1 – Input data high order bits latched first
PD	RW	Power Down mode (same function as PD# pin) 0 – Power Down. → Default after RESET 1 – Normal operation
RSEN	RO	Receiver Sense. This bit is HIGH if a powered on receiver is connected to the transmitter outputs, LOW otherwise. This function is only available for use in DC-coupled systems.
CTL0	RW	Control 0. CTL0, CTL1, CTL2, CTL3 are sent over TMDS interface when DE is LOW. CTL1-3 are driven in from external pins, but CTL0 is not available externally and therefore must be set through this register. Set to 0 for HDMI applications. 0 – Transmit CTL0 as LOW 1 – Transmit CTL0 as HIGH Note that when not in I²C mode, CTL0 is always transmitted as HIGH.

Notes:
1. RO = Read Only Registers
2. RW = Read/Write Registers
3. 'Default' indicates value set after a reset event. Not all bits default to a defined state after reset.

Dual Zone PLL

The SiI 1160 Tx offers a dual-zone PLL that changes its operational parameters depending on the frequency zone selected. In the low zone, operation is ideal in the low frequency range, from 20MHz to around 120MHz. High zone operation is optimized in the high frequency range, above 100MHz. In the overlapping range, either low zone or high zone operation can be used.

Operating zone optimization contributes to robust operation over long cables. For example, optimized PLL characteristics account for the ability of the transmitter to send video at UXGA over 20m cables.

PLL zone selection is controlled either manually or automatically. Manual zone control is the preferred mode of operation.

Manual Zone Control

Whenever the application allows it, PLL zone selection should be made manually. The I²C register bits ZONEF and EZONE allow the host graphics controller to set the optimal zone for the current video resolution being transmitted. For frequencies over 100MHz, the controller should select high zone PLL operation. Table 2 describes the relevant register bits.

Automatic Zone Control

For applications that are not able to program the I^2C registers, the chip incorporates an automatic zone control circuit. This circuit determines whether the input pixel clock is operating in the low frequency range or the high frequency range, and sets the PLL zone selection accordingly. The chip defaults to the automatic mode of zone selection after reset.

The zone determination depends primarily on input frequency, but is also affected by operating voltage and chip temperature. Therefore, it is possible for an automatic zone switch to occur while video input is stable, causing momentary (~1μs) unevenness in the video output clock and data streams. This could occur, for example, while the chip is still warming up to its normal operating temperature. However, the automatic selection circuit provides wide hysteresis to ensure that there will not be any oscillation around the zone switch point.

Table 2. Dual Zone PLL I^2C Control Register Bits

Register Name	Access	Description
ZONEF	RW	Zone Force. Enable external selection of main PLL operating zone. When ZONEF=1, the main PLL zone is selected by EZONE. 0 – Automatic zone selection – EZONE bit disabled (default) 1 – Manual zone selection – EZONE bit enabled
EZONE	RW	External Zone Select. Selects operating zone of main PLL, but only when ZONEF=1 (disabled by default). 0 – Low zone (recommended for 20-120MHz) 1 – High zone (recommended for > 100MHz)
ZONEO	RO	Zone Output – indicates current operating zone. When ZONEF=0 (automatic), ZONEO indicates that PLL is operating in zone optimized for: 0 = Lower frequencies 1 = Higher frequencies. When ZONEF=1 (manual), ZONEO information is not used.

Reset Description

The input pin ISEL/RST serves as an asynchronous reset for the I^2C slave controller in I^2C mode. The programming registers, which are accessible over the I^2C bus, lose their previously programmed values as soon as ISEL/RST is switched from HIGH to LOW. I^2C registers whose default values are not correct for normal operation must then be manually set to their appropriate value.

ISEL/RST serves only to set the registers to their default values, and to restore the interface to a known initial state. Without an initial reset, the I^2C interface may not respond properly. The minimum ISEL/RST high time for proper reset, after nominal VCC values have been reached, is T_{RESET}.

Register bit function PD is disabled after reset to eliminate any unexpected chip output before initialization. The state of this bit is set during the reset period according to the following rule: After a reset, the chip is turned off; the power down control bit, PD, is forced to 0. When the chip comes out of reset (ISEL/RST goes LOW), the TMDS outputs will be disabled and the transmitter will be turned off. To turn the transmitter back on, the PD bit must be set to 1 over the I^2C bus.

TFT Panel Data Mapping

The following TFT data mapping tables are strictly listed for single link TFT applications only. For DSTN mapping please refer to Application Note SiI-AN-0007-A. SiI 1151 and SiI 1161 have the same pinout.

Table 3. One Pixel/Clock Input/Output TFT Mode

TFT VGA Output		Tx Input Data		Rx Output Data		TFT Panel Input	
24-bpp	18-bpp	1160	164	1161	141B	24-bpp	18-bpp
B0		DIE0	D0	QE0	Q0	B0	
B1		DIE1	D1	QE1	Q1	B1	
B2	B0	DIE2	D2	QE2	Q2	B2	B0
B3	B1	DIE3	D3	QE3	Q3	B3	B1
B4	B2	DIE4	D4	QE4	Q4	B4	B2
B5	B3	DIE5	D5	QE5	Q5	B5	B3
B6	B4	DIE6	D6	QE6	Q6	B6	B4
B7	B5	DIE7	D7	QE7	Q7	B7	B5
G0		DIE8	D8	QE8	Q8	G0	
G1		DIE9	D9	QE9	Q9	G1	
G2	G0	DIE10	D10	QE10	Q10	G2	G0
G3	G1	DIE11	D11	QE11	Q11	G3	G1
G4	G2	DIE12	D12	QE12	Q12	G4	G2
G5	G3	DIE13	D13	QE13	Q13	G5	G3
G6	G4	DIE14	D14	QE14	Q14	G6	G4
G7	G5	DIE15	D15	QE15	Q15	G7	G5
R0		DIE16	D16	QE16	Q16	R0	
R1		DIE17	D17	QE17	Q17	R1	
R2	R0	DIE18	D18	QE18	Q18	R2	R0
R3	R1	DIE19	D19	QE19	Q19	R3	R1
R4	R2	DIE20	D20	QE20	Q20	R4	R2
R5	R3	DIE21	D21	QE21	Q21	R5	R3
R6	R4	DIE22	D22	QE22	Q22	R6	R4
R7	R5	DIE23	D23	QE23	Q23	R7	R5
Shift CLK	Shift CLK	IDCK	IDCK	ODCK	ODCK	Shift CLK	Shift CLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE	DE	DE

For 18-bit mode, the Flat Panel Graphics Controller interfaces to the transmitter exactly the same as in the 24-bit mode; however, 6 bits per channel (color) are used instead of 8. It is recommended that unused data bits be tied low. As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified. The data is sent during active display time while the control signals are sent during blank time. Note that the three data channels (CH0, CH1, CH2) are mapped to Blue, Green and Red data respectively.

Table 4. Two Pixels/Clock Input/Output TFT Mode

TFT VGA Output		Tx Input Data	Rx Output Data	TFT Panel Input	
24-bpp	18-bpp	1160	1161	24-bpp	18-bpp
B0 - 0		DIE0	QE0	B0 - 0	
B1 - 0		DIE1	QE1	B1 - 0	
B2 - 0	B0 - 0	DIE2	QE2	B2 - 0	B0 - 0
B3 - 0	B1 - 0	DIE3	QE3	B3 - 0	B1 - 0
B4 - 0	B2 - 0	DIE4	QE4	B4 - 0	B2 - 0
B5 - 0	B3 - 0	DIE5	QE5	B5 - 0	B3 - 0
B6 - 0	B4 - 0	DIE6	QE6	B6 - 0	B4 - 0
B7 - 0	B5 - 0	DIE7	QE7	B7 - 0	B5 - 0
G0 - 0		DIE8	QE8	G0 - 0	
G1 - 0		DIE9	QE9	G1 - 0	
G2 - 0	G0 - 0	DIE10	QE10	G2 - 0	G0 - 0
G3 - 0	G1 - 0	DIE11	QE11	G3 - 0	G1 - 0
G4 - 0	G2 - 0	DIE12	QE12	G4 - 0	G2 - 0
G5 - 0	G3 - 0	DIE13	QE13	G5 - 0	G3 - 0
G6 - 0	G4 - 0	DIE14	QE14	G6 - 0	G4 - 0
G7 - 0	G5 - 0	DIE15	QE15	G7 - 0	G5 - 0
R0 - 0		DIE16	QE16	R0 - 0	
R1 - 0		DIE17	QE17	R1 - 0	
R2 - 0	R0 - 0	DIE18	QE18	R2 - 0	R0 - 0
R3 - 0	R1 - 0	DIE19	QE19	R3 - 0	R1 - 0
R4 - 0	R2 - 0	DIE20	QE20	R4 - 0	R2 - 0
R5 - 0	R3 - 0	DIE21	QE21	R5 - 0	R3 - 0
R6 - 0	R4 - 0	DIE22	QE22	R6 - 0	R4 - 0
R7 - 0	R5 - 0	DIE23	QE23	R7 - 0	R5 - 0
B0 - 1		DIO0	QO0	B0 - 1	
B1 - 1		DIO1	QO1	B1 - 1	
B2 - 1	B0 - 1	DIO2	QO2	B2 - 1	B0 - 1
B3 - 1	B1 - 1	DIO3	QO3	B3 - 1	B1 - 1
B4 - 1	B2 - 1	DIO4	QO4	B4 - 1	B2 - 1
B5 - 1	B3 - 1	DIO5	QO5	B5 - 1	B3 - 1
B6 - 1	B4 - 1	DIO6	QO6	B6 - 1	B4 - 1
B7 - 1	B5 - 1	DIO7	QO7	B7 - 1	B5 - 1
G0 - 1		DIO8	QO8	G0 - 1	
G1 - 1		DIO9	QO9	G1 - 1	
G2 - 1	G0 - 1	DIO10	QO10	G2 - 1	G0 - 1
G3 - 1	G1 - 1	DIO11	QO11	G3 - 1	G1 - 1
G4 - 1	G2 - 1	DIO12	QO12	G4 - 1	G2 - 1
G5 - 1	G3 - 1	DIO13	QO13	G5 - 1	G3 - 1
G6 - 1	G4 - 1	DIO14	QO14	G6 - 1	G4 - 1
G7 - 1	G5 - 1	DIO15	QO15	G7 - 1	G5 - 1
R0 - 1		DIO16	QO16	R0 - 1	
R1 - 1		DIO17	QO17	R1 - 1	
R2 - 1	R0 - 1	DIO18	QO18	R2 - 1	R0 - 1
R3 - 1	R1 - 1	DIO19	QO19	R3 - 1	R1 - 1
R4 - 1	R2 - 1	DIO20	QO20	R4 - 1	R2 - 1
R5 - 1	R3 - 1	DIO21	QO21	R5 - 1	R3 - 1
R6 - 1	R4 - 1	DIO22	QO22	R6 - 1	R4 - 1
R7 - 1	R5 - 1	DIO23	QO23	R7 - 1	R5 - 1
ShiftClk/2	ShiftClk/2	IDCK	ODCK	Shift CLK	Shift CLK
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE

Table 5. 24-bit One Pixel/Clock Input with 24-bit Two Pixels/Clock Output TFT Mode

TFT VGA Output	Tx Input Data		Rx Output Data	TFT Panel Input
24-bpp	1160	164	1161	24-bpp
B0	DIE0	D0	QE0	B0 - 0
B1	DIE1	D1	QE1	B1 - 0
B2	DIE2	D2	QE2	B2 - 0
B3	DIE3	D3	QE3	B3 - 0
B4	DIE4	D4	QE4	B4 - 0
B5	DIE5	D5	QE5	B5 - 0
B6	DIE6	D6	QE6	B6 - 0
B7	DIE7	D7	QE7	B7 - 0
G0	DIE8	D8	QE8	G0 - 0
G1	DIE9	D9	QE9	G1 - 0
G2	DIE10	D10	QE10	G2 - 0
G3	DIE11	D11	QE11	G3 - 0
G4	DIE12	D12	QE12	G4 - 0
G5	DIE13	D13	QE13	G5 - 0
G6	DIE14	D14	QE14	G6 - 0
G7	DIE15	D15	QE15	G7 - 0
R0	DIE16	D16	QE16	R0 - 0
R1	DIE17	D17	QE17	R1 - 0
R2	DIE18	D18	QE18	R2 - 0
R3	DIE19	D19	QE19	R3 - 0
R4	DIE20	D20	QE20	R4 - 0
R5	DIE21	D21	QE21	R5 - 0
R6	DIE22	D22	QE22	R6 - 0
R7	DIE23	D23	QE23	R7 - 0
			QO0	B0 - 1
			QO1	B1 - 1
			QO2	B2 - 1
			QO3	B3 - 1
			QO4	B4 - 1
			QO5	B5 - 1
			QO6	B6 - 1
			QO7	B7 - 1
			QO8	G0 - 1
			QO9	G1 - 1
			QO10	G2 - 1
			QO11	G3 - 1
			QO12	G4 - 1
			QO13	G5 - 1
			QO14	G6 - 1
			QO15	G7 - 1
			QO16	R0 - 1
			QO17	R1 - 1
			QO18	R2 - 1
			QO19	R3 - 1
			QO20	R4 - 1
			QO21	R5 - 1
			QO22	R6 - 1
			QO23	R7 - 1
Shift CLK	IDCK	IDCK	ODCK	Shift CLK/2
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE

Table 6. 18-bit One Pixel/Clock Input with 18-bit Two Pixels/Clock Output TFT Mode

TFT VGA Output	Tx Input Data		Tx Output Data		TFT Panel Input
18-bpp	**1160**	**164**	**1161**	**141B**	**18-bpp**
	DIE0	D0	QE0		
	DIE1	D1	QE1		
B0	DIE2	D2	QE2	Q0	B0 - 0
B1	DIE3	D3	QE3	Q1	B1 - 0
B2	DIE4	D4	QE4	Q2	B2 - 0
B3	DIE5	D5	QE5	Q3	B3 - 0
B4	DIE6	D6	QE6	Q4	B4 - 0
B5	DIE7	D7	QE7	Q5	B5 - 0
	DIE8	D8	QE8		
	DIE9	D9	QE9		
G0	DIE10	D10	QE10	Q6	G0 - 0
G1	DIE11	D11	QE11	Q7	G1 - 0
G2	DIE12	D12	QE12	Q8	G2 - 0
G3	DIE13	D13	QE13	Q9	G3 - 0
G4	DIE14	D14	QE14	Q10	G4 - 0
G5	DIE15	D15	QE15	Q11	G5 - 0
	DIE16	D16	QE16		
	DIE17	D17	QE17		
R0	DIE18	D18	QE18	Q12	R0 - 0
R1	DIE19	D19	QE19	Q13	R1 - 0
R2	DIE20	D20	QE20	Q14	R2 - 0
R3	DIE21	D21	QE21	Q15	R3 - 0
R4	DIE22	D22	QE22	Q16	R4 - 0
R5	DIE23	D23	QE23	Q17	R5 - 0
			QO0		
			QO1		
			QO2	Q18	B0 - 1
			QO3	Q19	B1 - 1
			QO4	Q20	B2 - 1
			QO5	Q21	B3 - 1
			QO6	Q22	B4 - 1
			QO7	Q23	B5 - 1
			QO8		
			QO9		
			QO10	Q24	G0 - 1
			QO11	Q25	G1 - 1
			QO12	Q26	G2 - 1
			QO13	Q27	G3 - 1
			QO14	Q28	G4 - 1
			QO15	Q29	G5 - 1
			QO16		
			QO17		
			QO18	Q30	R0 - 1
			QO19	Q31	R1 - 1
			QO20	Q32	R2 - 1
			QO21	Q33	R3 - 1
			QO22	Q34	R4 - 1
			QO23	Q35	R5 - 1
Shift CLK	IDCK	IDCK	ODCK	Shift CLK/2	Shift CLK/2
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE

Table 7. Two Pixels/Clock Input with One Pixel/Clock Output TFT Mode

TFT VGA Output		Tx Input Data	Rx Output Data		TFT Panel Input	
24-bpp	18-bpp	1160	1161	141B	24-bpp	18-bpp
B0 - 0		DIE0	QE0	Q0	B0	
B1 - 0		DIE1	QE1	Q1	B1	
B2 - 0	B0 - 0	DIE2	QE2	Q2	B2	B0
B3 - 0	B1 - 0	DIE3	QE3	Q3	B3	B1
B4 - 0	B2 - 0	DIE4	QE4	Q4	B4	B2
B5 - 0	B3 - 0	DIE5	QE5	Q5	B5	B3
B6 - 0	B4 - 0	DIE6	QE6	Q6	B6	B4
B7 - 0	B5 - 0	DIE7	QE7	Q7	B7	B5
G0 - 0		DIE8	QE8	Q8	G0	
G1 - 0		DIE9	QE9	Q9	G1	
G2 - 0	G0 - 0	DIE10	QE10	Q10	G2	G0
G3 - 0	G1 - 0	DIE11	QE11	Q11	G3	G1
G4 - 0	G2 - 0	DIE12	QE12	Q12	G4	G2
G5 - 0	G3 - 0	DIE13	QE13	Q13	G5	G3
G6 - 0	G4 - 0	DIE14	QE14	Q14	G6	G4
G7 - 0	G5 - 0	DIE15	QE15	Q15	G7	G5
R0 - 0		DIE16	QE16	Q16	R0	
R1 - 0		DIE17	QE17	Q17	R1	
R2 - 0	R0 - 0	DIE18	QE18	Q18	R2	R0
R3 - 0	R1 - 0	DIE19	QE19	Q19	R3	R1
R4 - 0	R2 - 0	DIE20	QE20	Q20	R4	R2
R5 - 0	R3 - 0	DIE21	QE21	Q21	R5	R3
R6 - 0	R4 - 0	DIE22	QE22	Q22	R6	R4
R7 - 0	R5 - 0	DIE23	QE23	Q23	R7	R5
B0 - 1		DIO0				
B1 - 1		DIO1				
B2 - 1	B0 - 1	DIO2				
B3 - 1	B1 - 1	DIO3				
B4 - 1	B2 - 1	DIO4				
B5 - 1	B3 - 1	DIO5				
B6 - 1	B4 - 1	DIO6				
B7 - 1	B5 - 1	DIO7				
G0 - 1		DIO8				
G1 - 1		DIO9				
G2 - 1	G0 - 1	DIO10				
G3 - 1	G1 - 1	DIO11				
G4 - 1	G2 - 1	DIO12				
G5 - 1	G3 - 1	DIO13				
G6 - 1	G4 - 1	DIO14				
G7 - 1	G5 - 1	DIO15				
R0 - 1		DIO16				
R1 - 1		DIO17				
R2 - 1	R0 - 1	DIO18				
R3 - 1	R1 - 1	DIO19				
R4 - 1	R2 - 1	DIO20				
R5 - 1	R3 - 1	DIO21				
R6 - 1	R4 - 1	DIO22				
R7 - 1	R5 - 1	DIO23				
ShiftClk/2	ShiftClk/2	IDCK	ODCK	ODCK	ShiftClk	ShiftClk
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
DE	DE	DE	DE	DE	DE	DE

Design Recommendations

Differences Between SiI 160 and SiI 1160

The SiI 1160 Tx is a pin-compatible upgrade to the SiI 160 Tx. It provides improved cable length support without any changes to the pinout. Interrupt capability is also a new option using the optional MSEN pin. The SiI 1160 Tx can also act as to repeat HDMI signals when its internal registers are programmed appropriately; this application requires the use of an I^2C interface, optionally available on the SDA and SCL pins.

Table 8. New Pin Functions for SiI 1160 Tx

Pin	SiI 160	SiI 1160
20	RSVD – Tied HIGH	Optional I^2C interface pin SCL
21	RSVD – Tied LOW	Optional interrupt output MSEN
23	RSVD – Tied HIGH	Optional I^2C interface pin SDA
87	RSVD – Tied HIGH	ISEL/RST

EXT_SWING Selection

The recommended R_{EXT_SWING} resistor value for the EXT_SWING pin is provided in the Pin Descriptions section. This value can be adjusted as needed to optimize the DVI signal swing levels according to the needs of the application. This adjustment might become necessary, for example, when deviating from the recommended source termination values (described in the Source Termination Resistors on Differential Outputs section) to optimize for a specific cabling environment.

PCB Ground Planes

All ground pins on the device should be connected to the same, contiguous ground plane in the PCB. This helps to avoid ground loops and inductances from one ground plane segment to another. Such low-inductance ground paths are critical for return currents, which affect EMI performance. The entire ground plane surrounding the PanelLink transmitter should be one piece, and include the ground vias for the DVI connector.

Voltage Ripple Regulation

The power supply to PVCC is very important to the proper operation of the Transmitter chips. PVCC does not draw much current so any voltage regulator that can supply 50mA or more is sufficient. A suggested regulator circuit using a low-dropout regulator is shown in Figure 11. Note that alternative voltage regulator circuits should be considered only if they meet the LM317 standards of line/load regulation.

Decoupling and bypass capacitors are also involved with power supply connections, as described in detail in Figure 14 and Figure 15.

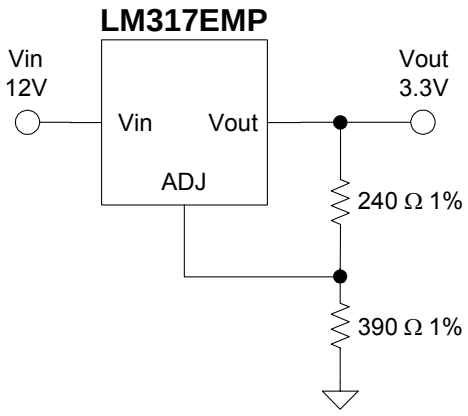


Figure 11. Voltage Regulation using LM317EMP

Spread Spectrum Support

TMDS architecture is inherently jitter-tolerant. Spread spectrum clocking can be applied to the clock and parallel data inputs of the SiI 1160 to allow for reduced EMI. The spread will be propagated throughout the system due to TMDS clock architecture, which passes nearly all low-frequency components of the incoming clock without attenuation. The amount of spread that can be applied without affecting the DVI eye is limited to ±0.5% with the current part, depending on the spreading algorithm employed by the external spread spectrum device.

A planned future variation of this chip will allow its internal clock to be coupled directly to a spread spectrum device. The expected result will be the ability to accommodate larger amounts of spread, and it will also work in 48-bit mode as well as 24-bit mode. Designs should make accommodations using pins 27, 83, and 84 as noted in the Pin Descriptions section so that the planned part can become a drop-in replacement for the SiI 1160.

Figure 12 illustrates how a design can anticipate the expected future chip version. Contact PhaseLink Corporation for additional information on their spread spectrum device.

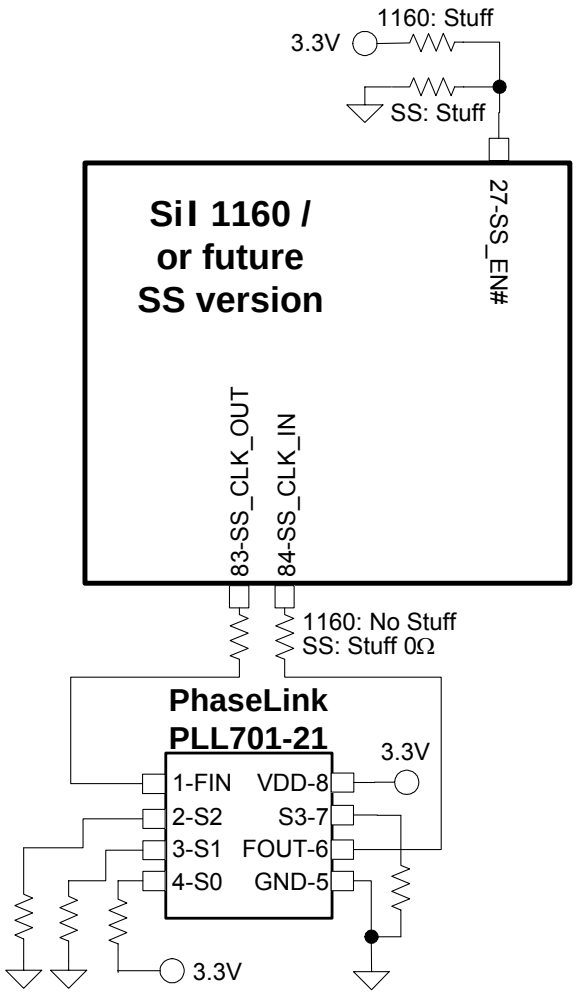


Figure 12. Planned Spread Spectrum Support Circuit

Reset Circuit for I²C Application

If the design uses the I²C interface to control the transmitter features, it must also provide a means of toggling the ISEL/RST pin to achieve the correct T_{RESET} timing. If a local microcontroller is hosting the I²C connection, the easiest way to provide the reset is to connect a GPIO pin from the microcontroller to the transmitter chip as shown in Figure 13. The reset pulse can then be commanded either at power-up time or just prior to initial use of the I²C interface as shown in Figure 8.

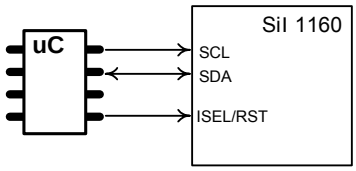


Figure 13. Typical Reset Circuit

Power Control

The low-power standby state feature of the chip provides a design option of leaving the chip always powered, as opposed to powering it on and off. Leaving the chip powered and using the PD pin to put it in a lower power state may result in faster system response time, depending on the system Vcc supply ramp-up delay.

Table 9 provides information on chip functional mode current requirements. These values are not specifications, but are representative of typical chip power consumption. PVCC1 and PVCC2 are the power planes that are most sensitive to excessive noise. Noise on these planes can be more easily controlled when they are regulated separately from digital VCC.

Table 9. Power Consumption Characteristics

Symbol	Parameter	Conditions	Typ	Units
I_{CCT}	Total Transmitter Operating Current	165MHz	see spec.	
I_{AVCC}	Current on AVCC		17-19	% of total I_{CCT}
I_{PVCC1}	Current on PVCC1		31-33	% of total I_{CCT}
I_{PVCC2}	Current on PVCC2		10-11	% of total I_{CCT}
$I_{VCC} + I_{IVCC}$	Current on digital core VCC and input plan IVCC		38-41	% of total I_{CCT}
$I_{VCCPD} + I_{IVCCPD}$	Standby mode current on VCC and IVCC	PD pin driven low[1] DVI clock stopped	>97	% of total I_{PD}

Note
1. For I²C mode: bit PD=0.

Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 15. Place these components as close as possible to the PanelLink device pins, and avoid routing through vias if possible, as shown in Figure 14, which is representative of the various types of power pins on the transmitter.

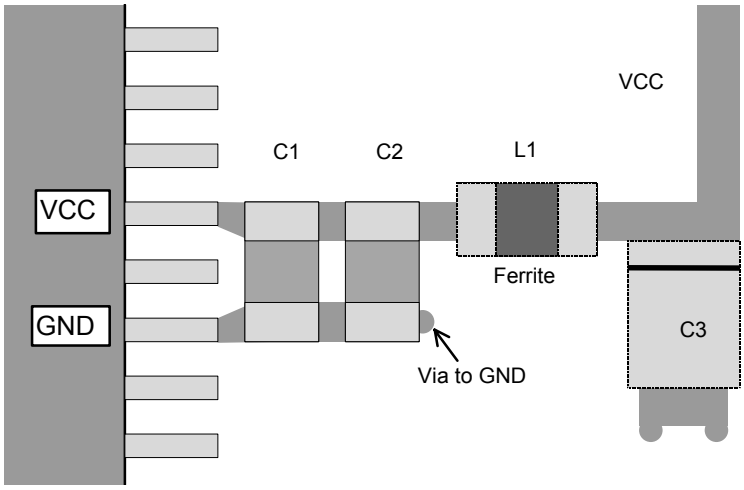


Figure 14. Decoupling and Bypass Capacitor Placement

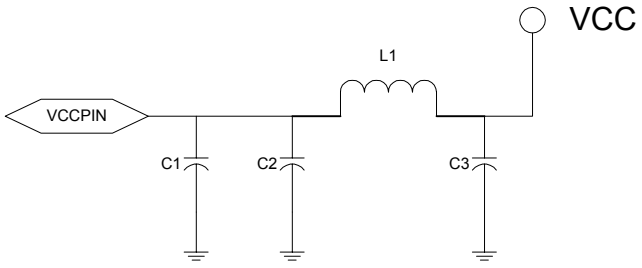


Figure 15. Decoupling and Bypass Schematic

The values shown in Table 10 are recommendations that should be adjusted according to the noise characteristics of the specific board-level design. Pins in one group (such as IVCC) may share C2, L1, and C3, each pin having C1 placed as close to the pin as possible. PGND1 and PGND2 should be tied individually to ground.

Table 10. Recommended Components for Bypass and Decoupling Circuits

C1	C2	C3	L1
100 – 300 pF	2.2 – 10 uF	10 uF	200+ Ω

Series Damping Resistors on Outputs

Series resistors are often effective in lowering data-related emissions and reducing reflections. Series resistors with a value close to the impedance of the board traces are generally most effective in reducing reflections from the inputs of the transmitter. If used, resistors should be placed close to the output pins of the VGA Source or Graphics chip, as shown in Figure 16.

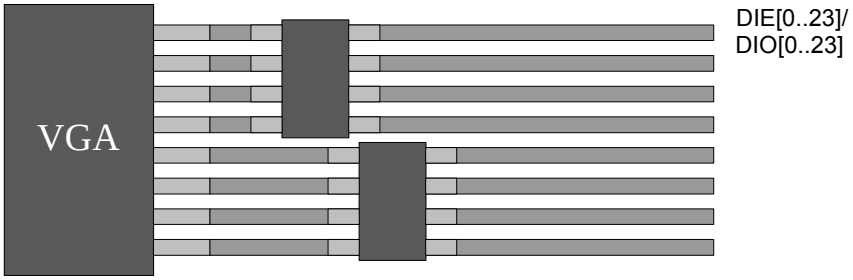


Figure 16. Series Input Damping Resistors for Driving Source

Source Termination Resistors on Differential Outputs

Source termination, consisting of a 300Ω resistor and a 0.1µF capacitor, may be used on the differential outputs of the SiI 1160 to improve signal swings. See Figure 17 for an illustration. Repeat the circuit for each of the four differential output pairs: TX0+, TX1+, TX2+, TXC+.

Note that the specific value for the source termination resistor and capacitor will depend on the PCB layout and construction. Different values may be needed to create optimum DVI-compliant output waveforms from the transmitter.

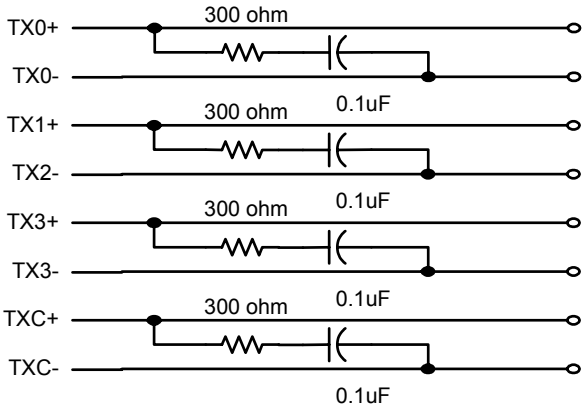


Figure 17. Differential Output Source Terminations

Source termination suppresses signal reflection to prevent non-DVI compliant receivers from erroneously sampling the TMDS signals at high frequencies (beyond 135MHz). The impact on DVI compliant receivers is minimal. Therefore Silicon Image recommends source termination for most applications.

Note that the capacitor is required to meet DVI idle mode DC offset requirements and must not be omitted. Note also that the signal suppression requires the R_{EXT_SWING} value to be changed.

Power consumption will be slightly higher when using source termination.

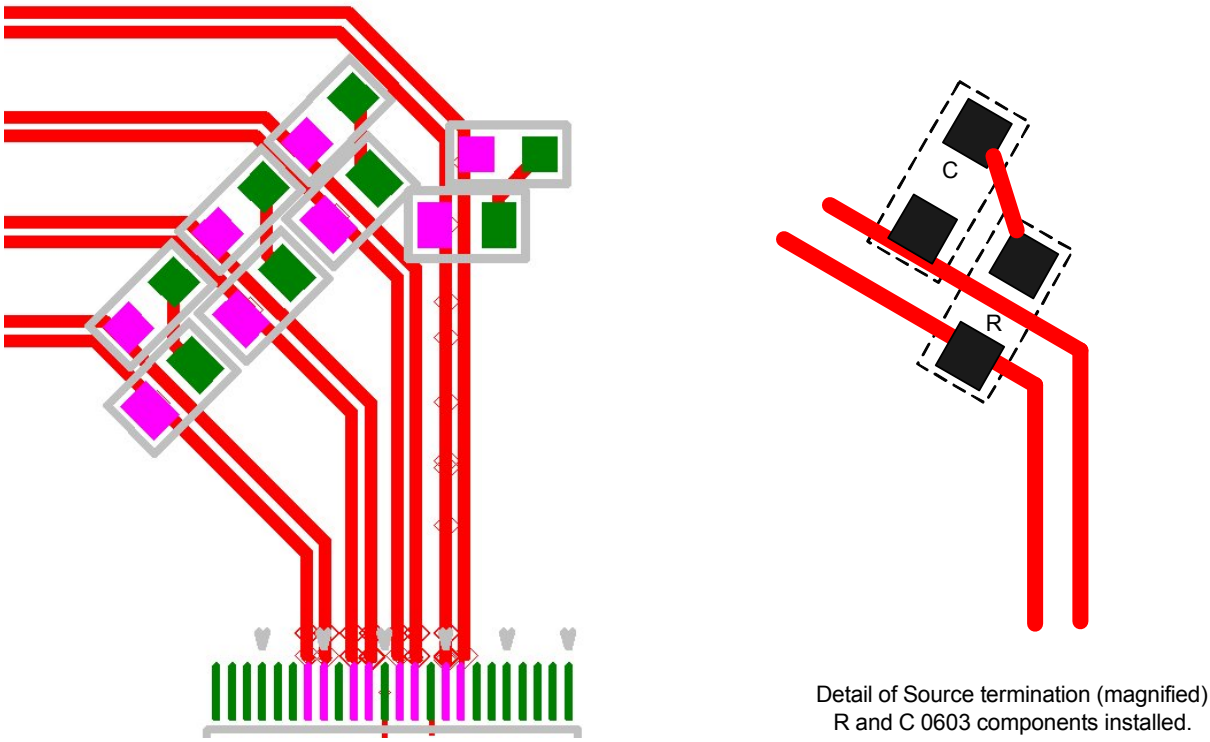


Figure 18. Source Termination Layout Illustration

The layout in Figure 18 has been developed to minimize trace stubs on the differential TMDS lines, while providing pads for the source termination components (left-hand magnified view). Source termination components should be placed close to the transmitter pins. The resistor and capacitor are shown installed on the pads provided (right-hand magnified view).

Differential Trace Routing

The routing for the SiI 1160 chip is relatively simple since no spiral skew compensation is needed. However, a few small precautions are required to achieve the full performance and reliability of DVI.

The Transmitter can be placed fairly far from the output connector, but care should be taken to route each differential signal pair together and achieve impedance of 100Ω between the differential signal pair. However, note that the longer the differential traces are between the transmitter and the output connector, the higher the chance that external signal noise will couple onto the low-voltage signals and affect image quality.

Do not split or have asymmetric trace routing between the differential signal pair. Vias are very inductive and can cause phase delay problems if applied unevenly within a differential pair. Vias should be minimized or avoided if possible by placing all differential traces on the top layer of the PCB.

Figure 19 illustrates an incorrect routing of the differential signal from the SiI 1160 to the DVI connector. Figure 20 illustrates the correct method to route the differential signal from the SiI 1160 to the DVI connector. Figure 21 illustrates recommended routing for differential traces at the DVI connector.

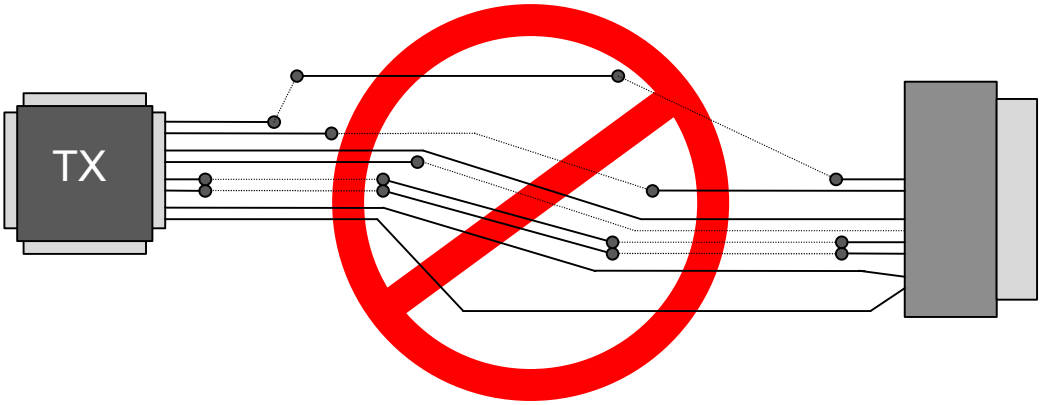


Figure 19. Example of Incorrect Differential Signal Routing

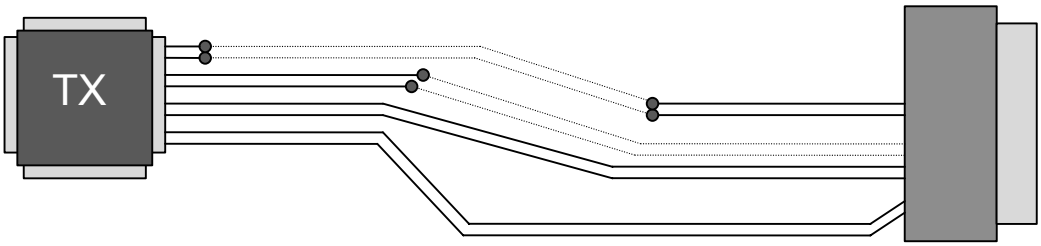


Figure 20. Example of Correct Differential Signal Routing

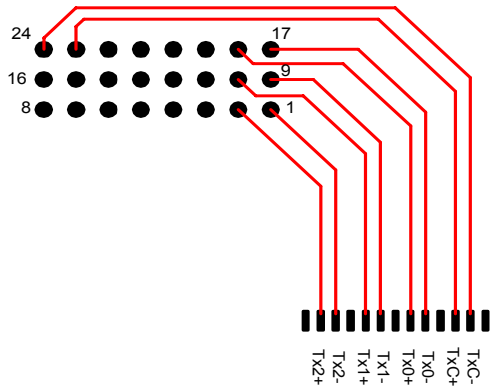


Figure 21. Differential Trace Routing to DVI Connector (Top Side View)

In addition to following the trace routing recommendations, length differences between intra-pair traces listed in column 2 of Table 11 and inter-pair traces listed in column 3 of Table 11, should be controlled to minimize DVI skew.

Spacing between inter-pair DVI traces should be observed to reduce trace-to-trace couplings. For example, having wider gaps between inter-pair DVI traces will minimize noise coupling. It is also strongly advised that ground not be placed adjacent to the DVI traces on the same layer. Table 11 lists the recommended limits for the parameters listed above.

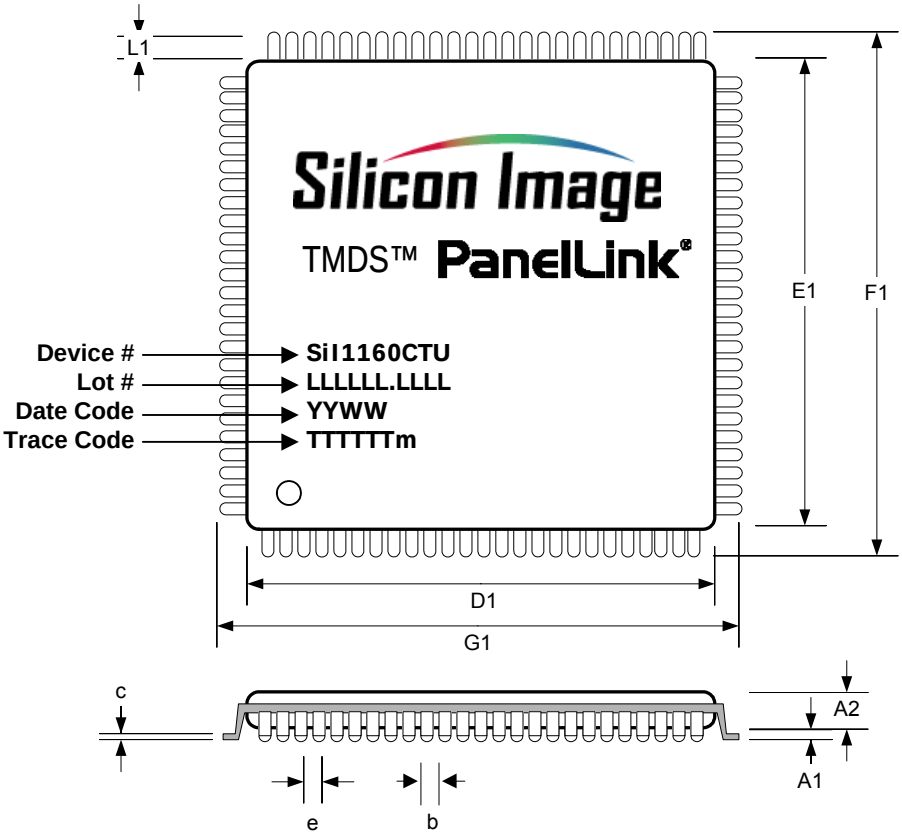
Table 11. Routing Guidelines for DVI Traces

Parameter	Intra-pair (length of each trace within a pair)	Inter-pair (length of each pair compared to other pairs)	Recommended Inter–pair Trace Separation Based on 2 Layer Board	Recommended Inter–pair Trace Separation Based on 4 Layer Board
Max	±0.75 inch	±3 inch		
Min			2x trace width	2x trace width

Package Dimensions

Package

100-pin TQFP Package Dimensions and Marking Specification



JEDEC Package Code MS-026-AED

		typ	max
A	Thickness		1.20
A1	Stand-off		0.15
A2	Body Thickness	1.00	1.05
D1	Body Size	14.00	
E1	Body Size	14.00	
F1	Footprint	16.00	
G1	Footprint	16.00	
L1	Lead Length	1.00	
b	Lead Width	0.20	
c	Lead Thickness		0.20
e	Lead Pitch	0.50	

Dimensions in millimeters.
Overall thickness A=A1+A2.

Package: SiI1160CTU

Legend	Description
LLLLLL.LLLL	Lot Number
YY	Year of Mfr
WW	Week of Mfr
TTTTTT	Trace Code
m	Maturity Code =0: engineering samples =1: pre-production >1: production

Figure 22. 100-pin TQFP Package Dimensions (JEDEC code MS-026-AED)

Ordering Information

Standard Part Number: SiI1160CTU
('U' indicates Universal package usable in both standard and lead-free environments)

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