Si5365

PRELIMINARY DATA SHEET

PIN-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

Description

The Si5365 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel, in which the application requires clock multiplication without jitter attenuation. The Si5365 accepts four clock inputs ranging from 19.44 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. The Si5365 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8 or 2.5 V supply, the Si5365 is ideal for providing clock multiplication in high performance timing applications.

Applications

- SONET/SDH OC-48/OC-192 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Test and measurement

Features

- Selectable output frequencies ranging from 19.44 to 1050 MHz
- Low jitter clock outputs w/jitter generation as low as 0.6 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (30 kHz to 1.3 MHz)
- Four clock inputs w/manual or automatically controlled hitless switching
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm outputs
- Digitally-controlled output phase adjust
- Pin-programmable settings
- On-chip voltage regulator for 1.8 or 2.5 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS compliant

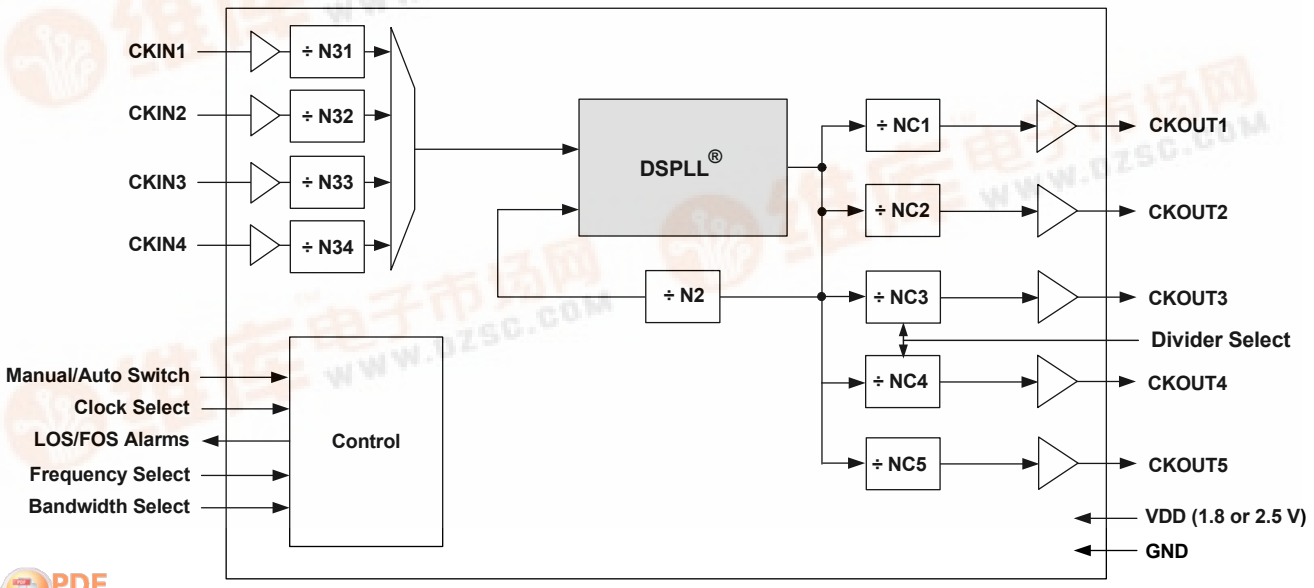


Table 1. Performance Specifications
(V_{DD} = 1.8 or 2.5 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}		2.25	2.5	2.75	V
			1.62	1.8	1.98	V
Supply Current	I_{DD}	f_{OUT} = 622.08 MHz All CKOUTs enabled LVPECL format output	—	394	435	mA
		Only CKOUT1 enabled	—	253	284	mA
		f_{OUT} = 19.44 MHz All CKOUTs enabled CMOS format output	—	278	321	mA
		Only CKOUT1 enabled	—	229	261	mA
		Tristate/Sleep Mode	—	TBD	TBD	mA
Input Clock Frequency (CKIN1, CKIN2, CKIN3, CKIN4)	CK_F	Input frequency and clock multiplication ratio pin-selectable from table of values using FRQSEL and FRQTBL settings. Consult Silicon Laboratories configuration software DSPLL*sim* or Any-Rate Precision Clock Family Reference Manual at www.silabs.com/timing for table selections.	19.44	—	707.35	MHz
Output Clock Frequency (CKOUT1, CKOUT2, CKOUT3, CKOUT4, CKOUT5)	CK_{OF}		19.44	—	1049.76	MHz
Input Clocks (CKIN1, CKIN2, CKIN3, CKIN4)						
Differential Voltage Swing	CKN_{DPP}		0.25	—	1.9	V_{PP}
Common Mode Voltage	CKN_{VCM}	1.8 V ±10%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
Rise/Fall Time	CKN_{TRF}	20–80%	—	—	11	ns
Duty Cycle	CKN_{DC}	Whichever is less	40	—	60	%
			50	—	—	ns
Output Clocks (CKOUT1, CKOUT2, CKOUT3, CKOUT4, CKOUT5)						
Common Mode	V_{OCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	V_{OD}		1.1	—	1.9	V
Single Ended Output Swing	V_{SE}		0.5	—	0.93	V
Rise/Fall Time	CKO_{TRF}	20–80%	—	230	350	ps

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 1. Performance Specifications (Continued)
(V_{DD} = 1.8 or 2.5 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Duty Cycle	CKO_{DC}		45	—	55	%
PLL Performance						
Jitter Generation	J_{GEN}	f_{OUT} = 622.08 MHz, LVPECL output format 50 kHz–80 MHz	—	0.6	TBD	ps rms
		12 kHz–20 MHz	—	0.6	TBD	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB
Phase Noise	CKO_{PN}	f_{OUT} = 622.08 MHz 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	TBD	TBD	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	40	—	ºC/W

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.75	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
Operating Junction Temperature	T_{JCT}	–55 to 150	ºC
Storage Temperature Range	T_{STG}	–55 to 150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ)		2	kV
ESD MM Tolerance		200	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

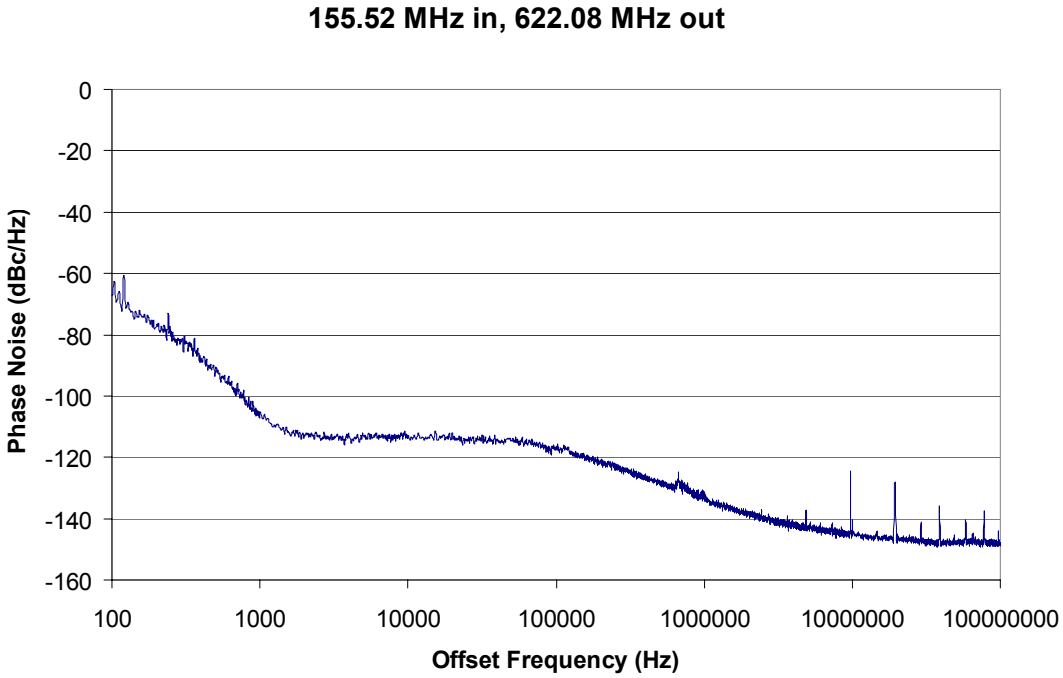
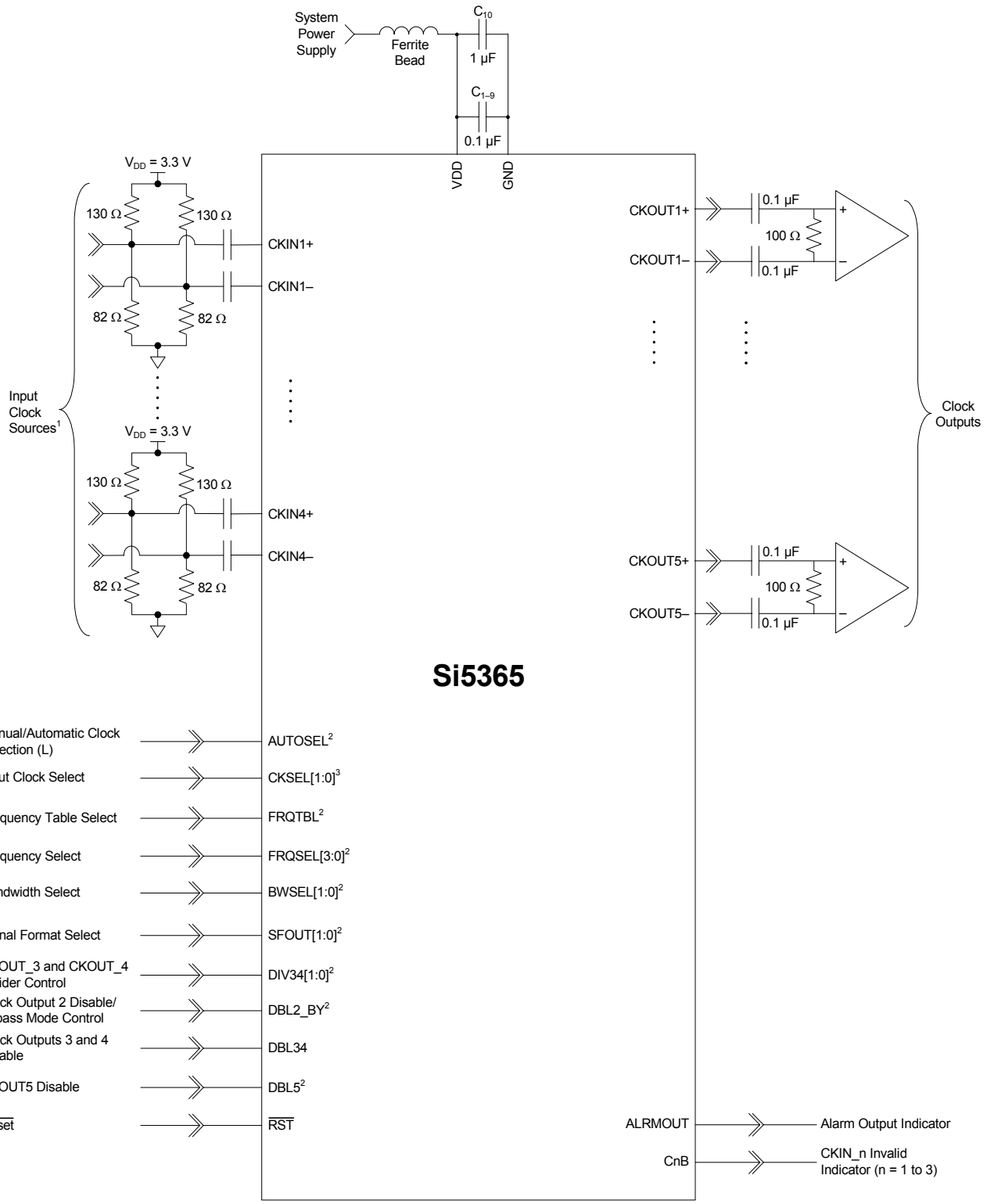


Figure 1. Typical Phase Noise Plot



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (V_{DD}/2), and H (V_{DD}).
3. Assumes manual input clock selection.

Figure 2. Si5365 Typical Application Circuit

1. Functional Description

The Si5365 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel, in which the application requires clock multiplication without jitter attenuation. The Si5365 accepts four clock inputs ranging from 19.44 to 707 MHz and generates five frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. By default the four clock inputs are at the same frequency and the five clock outputs are at the same frequency. Two of the output clocks can be divided down further to generate an integer sub-multiple frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. In addition to providing clock multiplication in SONET and datacom applications, the Si5365 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to look up valid Si5365 frequency translations. This utility can be downloaded from www.silabs.com/timing. This information is also available in the Any-Rate Precision Clock Family Reference Manual, also available from www.silabs.com/timing.

The Si5365 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5365 PLL loop bandwidth is digitally programmable via the BWSEL[1:0] pins and supports a range from 30 kHz to 1.3 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5365 monitors all input clocks for loss-of-signal and provides a LOS alarm when it detects a missing clock.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5365 has five differential clock outputs. The signal format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8 or 2.5 V supply.

1.1. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for more detailed information about the Si5365. The FRM can be downloaded from www.silabs.com/timing.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. This utility can be downloaded from www.silabs.com/timing.

2. Pin Descriptions: Si5365

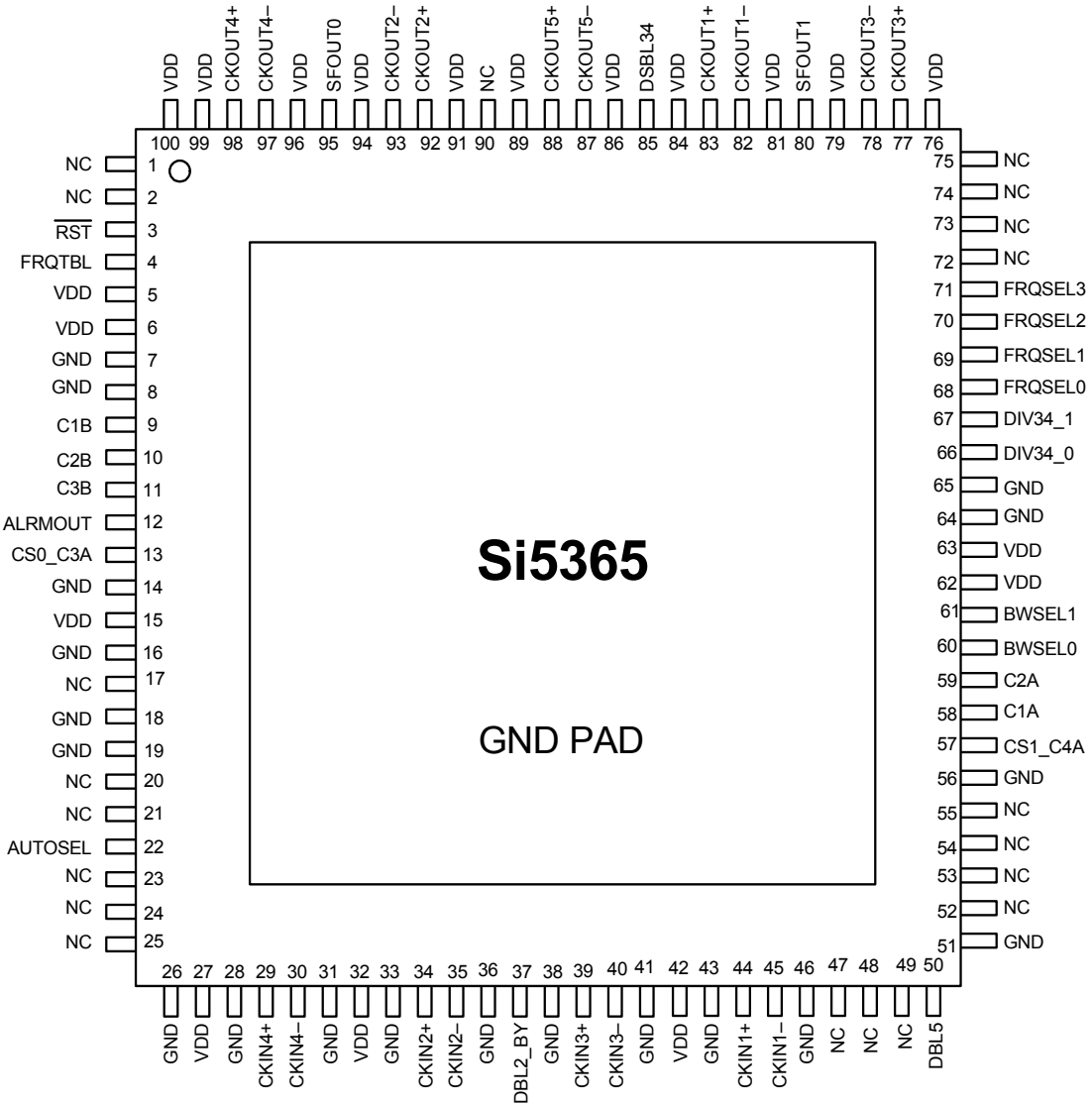


Table 3. Si5365 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1, 2, 17, 20, 21, 23, 24, 25, 47, 48, 49, 52, 53, 54, 55, 72, 73, 74, 75, 90	NC			**No Connect.** These pins must be left unconnected for normal operation.

Table 3. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
3	$\overline{RST}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. After rising edge of $\overline{RST}$ signal, the device will perform an internal self-calibration. This pin has a weak pull-up.
4	FRQTBL	I	3-Level	**Frequency Table Select.** This pin selects SONET/SDH, datacom, or SONET/SDH to datacom frequency translation table. L = SONET/SDH. M = Datacom. H = SONET/SDH to Datacom. This pin has a weak pull-down.
5, 6, 15, 27, 32, 42, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100	V_{DD}	V_{DD}	Supply	**V_{DD}.** The device operates from a 1.8 or 2.5 V supply. Bypass capacitors should be associated with the following V_{DD} pins: Pins — Bypass Cap 5, 6 — 0.1 µF 15 — 0.1 µF 27 — 0.1 µF 62, 63 — 0.1 µF 76, 79 — 1.0 µF 81, 84 — 0.1 µF 86, 89 — 0.1 µF 91, 94 — 0.1 µF 96, 99, 100 — 0.1 µF
7, 8, 14, 16, 18, 19, 26, 28, 31, 33, 36, 38, 41, 43, 46, 51, 56, 64, 65	GND	GND	Supply	**Ground.** These pins must be connected to system ground. Minimize the ground path impedance for optimal performance.
9	C1B	O	LVCMOS	**CKIN1 Invalid Indicator.** This pin is an active high alarm output associated with CKIN1. Once triggered, the alarm will remain high until CKIN1 is validated. 0 = No alarm on CKIN1. 1 = Alarm on CKIN1.
10	C2B	O	LVCMOS	**CKIN2 Invalid Indicator.** This pin is an active high alarm output associated with CKIN2. Once triggered, the alarm will remain high until CKIN2 is validated. 0 = No alarm on CKIN2. 1 = Alarm on CKIN2.
11	C3B	O	LVCMOS	**CKIN3 Invalid Indicator.** This pin is an active high alarm output associated with CKIN3. 0 = No alarm on CKIN3. 1 = Alarm on CKIN3.

Table 3. Si5365 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>12</td><td>ALRMOUT</td><td>O</td><td>LVCMOS</td><td>Alarm Output Indicator.
This pin is an active high alarm output associated with CKIN4 or the frame sync alignment alarm.
0 = ALRMOUT not active.
1 = ALRMOUT active.</td></tr>
<tr><td>13
57</td><td>CS0_C3A
CS1_C4A</td><td>I/O</td><td>LVCMOS</td><td>Input Clock Select/CKINn Active Clock Indicator.
If manual clock selection mode is chosen (AUTOSEL = 1), the CS[1:0] pins function as the manual input clock selector control.
<table>
<tr><th>CS[1:0]</th><th>Active Input Clock</th></tr>
<tr><td>00</td><td>CKIN1</td></tr>
<tr><td>01</td><td>CKIN2</td></tr>
<tr><td>10</td><td>CKIN3</td></tr>
<tr><td>11</td><td>CKIN4</td></tr>
</table>
These inputs are internally deglitched to prevent inadvertent clock switching during changes in the CSn input state.
If automatic clock detection is chosen (AUTOSEL = M or H), these pins function as the CKINn active clock indicator output.
0 = CKINn is not the active input clock.
1 = CKINn is currently the active input clock to the PLL.
This pin has a weak pull-down.</td></tr>
<tr><td>22</td><td>AUTOSEL</td><td>I</td><td>3-Level</td><td>Manual/Automatic Clock Selection.
Three level input that selects the method of input clock selection to be used.
L = Manual.
M = Automatic non-revertive.
H = Automatic revertive.</td></tr>
<tr><td>29
30</td><td>CKIN4+
CKIN4–</td><td>I</td><td>MULTI</td><td>Clock Input 4.
Differential clock input. This input can also be driven with a single-ended signal.</td></tr>
<tr><td>34
35</td><td>CKIN2+
CKIN2–</td><td>I</td><td>MULTI</td><td>Clock Input 2.
Differential input clock. This input can also be driven with a single-ended signal.</td></tr>
<tr><td>37</td><td>DBL2_BY</td><td>I</td><td>3-Level</td><td>CKOUT2 Disable/PLL Bypass Mode Control.
Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode.
L = CKOUT2 Enabled.
M = CKOUT2 Disabled.
H = BYPASS Mode with CKOUT2 enabled.</td></tr>
<tr><td>39
40</td><td>CKIN3+
CKIN3–</td><td>I</td><td>MULTI</td><td>Clock Input 3.
Differential clock input. This input can also be driven with a single-ended signal.</td></tr>
<tr><td>44
45</td><td>CKIN1+
CKIN1–</td><td>I</td><td>MULTI</td><td>Clock Input 1.
Differential clock input. This input can also be driven with a single-ended signal.</td></tr>
</table>

Table 3. Si5365 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
50	DBL5	I	3-Level	**CKOUT5 Disable.** This pin performs the following functions: L = Normal operation. Output path is active and signal format is determined by SFOUT inputs. M = CMOS signal format. Overrides SFOUT signal format to allow CKOUT5 to operate in CMOS format while the clock outputs operate in a differential output format. H = Powerdown. Entire CKOUT5 divider and output buffer path is powered down. CKOUT5 output will be in tristate mode during powerdown.
58	C1A	O	LVCMOS	**CKIN1 Active Clock Indicator.** This pin serves as the CKIN1 active clock indicator. 0 = CKIN1 is not the active input clock. 1 = CKIN1 is currently the active input clock to the PLL.
59	C2A	O	LVCMOS	**CKIN2 Active Clock Indicator.** This pin serves as the CKIN2 active clock indicator. 0 = CKIN2 is not the active input clock. 1 = CKIN2 is currently the active input clock to the PLL.
60 61	BWSEL0 BWSEL1	I	3-Level	**Bandwidth Select.** These pins are three level inputs that select the DSPLL closed loop bandwidth according to the Any-Rate Precision Clock Family Reference Manual.
66 67	DIV34_0 DIV34_1	I	3-Level	**CKOUT3 and CKOUT4 Divider Control.** These pins control the division of CKOUT3 and CKOUT4 relative to the CKOUT2 output frequency. Detailed operations and timing characteristics for these pins may be found in the Any-Rate Precision Clock Family Reference Manual.
68 69 70 71	FRQSEL0 FRQSEL1 FRQSEL2 FRQSEL3	I	3-Level	**Multiplier Select.** These pins are three level inputs that select the input clock and clock multiplication setting according to the Any-Rate Precision Clock Family Reference Manual, depending on the FRQTBL setting.
77 78	CKOUT3+ CKOUT3–	O	MULTI	**Clock Output 3.** Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.

Table 3. Si5365 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>80
95</td><td>SFOUT1
SFOUT0</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for all of the clock outputs and CKOUT5.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>Reserved</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Tristate/Sleep</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>82
83</td><td>CKOUT1–
CKOUT1+</td><td>O</td><td>MULTI</td><td>Clock Output 1.
Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>85</td><td>DBL34</td><td>I</td><td>LVCMOS</td><td>Output 3 and 4 Disable.
Active high input. When active, entire CKOUT3 and CKOUT4 divider and output buffer path is powered down. CKOUT3 and CKOUT4 outputs will be in tristate mode during powerdown.
This pin has a weak pull-down.</td></tr>
<tr><td>87
88</td><td>CKOUT5–
CKOUT5+</td><td>O</td><td>MULTI</td><td>Clock Output 5.
Fifth high-speed clock output with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>92
93</td><td>CKOUT2+
CKOUT2–</td><td>O</td><td>MULTI</td><td>Clock Output 2.
Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>97
98</td><td>CKOUT4–
CKOUT4+</td><td>O</td><td>MULTI</td><td>Clock Output 4.
Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>GND PAD</td><td>GND PAD</td><td>GND</td><td>Supply</td><td>Ground Pad.
The ground pad must provide a low thermal and electrical impedance to a ground plane.</td></tr>
</table>

3. Ordering Guide

Ordering Part Number	Package	Temperature Range
Si5365-B-GQ	100-Pin 14 x 14 mm TQFP	–40 to 85 °C

4. Package Outline: 100-Pin TQFP

Figure 3 illustrates the package details for the Si5365. Table 4 lists the values for the dimensions shown in the illustration.

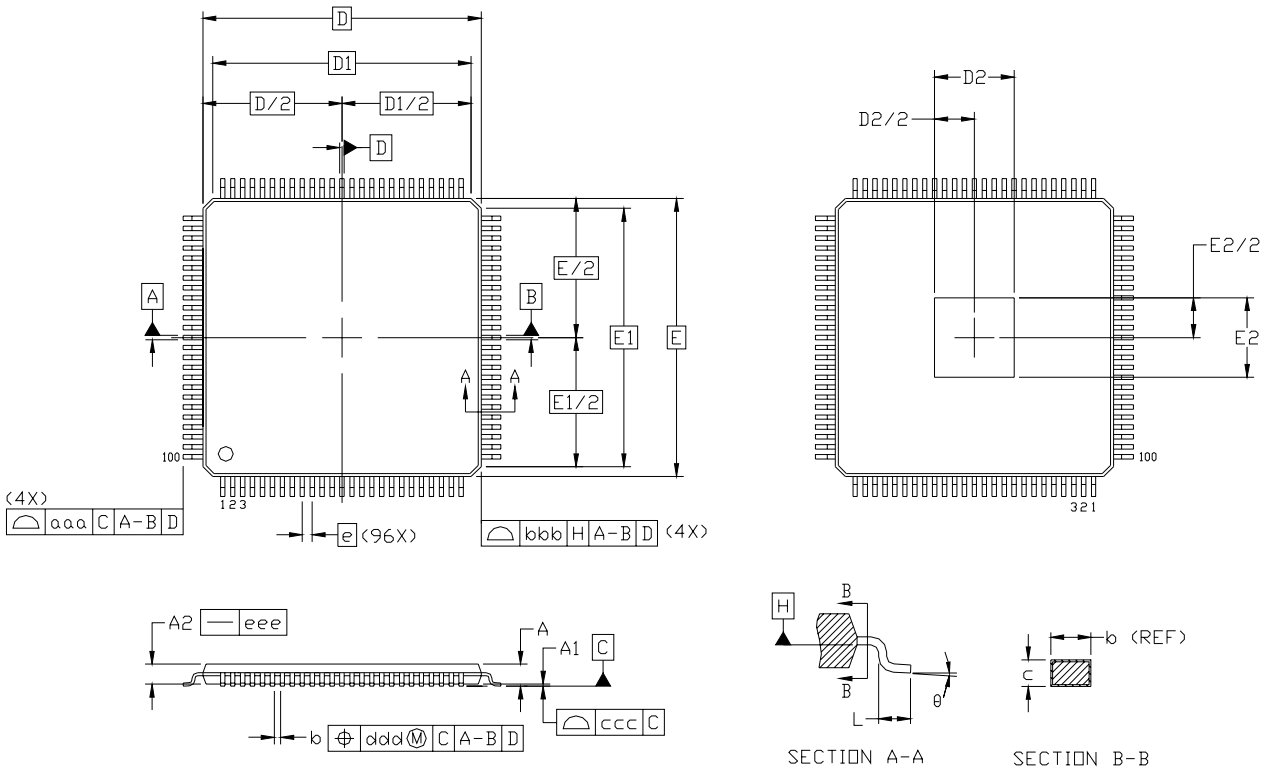


Figure 3. 100-Pin Thin Quad Flat Package (TQFP)

Table 4. 100-Pin Package Diagram Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.20	E	16.00 BSC.		
A1	0.05	—	0.15	E1	14.00 BSC.		
A2	0.95	1.00	1.05	E2	3.85	4.00	4.15
b	0.17	0.22	0.27	L	0.45	0.60	0.75
c	0.09	—	0.20	aaa	—	—	0.20
D	16.00 BSC.			bbb	—	—	0.20
D1	14.00 BSC.			ccc	—	—	0.08
D2	3.85	4.00	4.15	ddd	—	—	0.08
e	0.50 BSC.			Θ	0º	3.5º	7º

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. Recommended PCB Layout

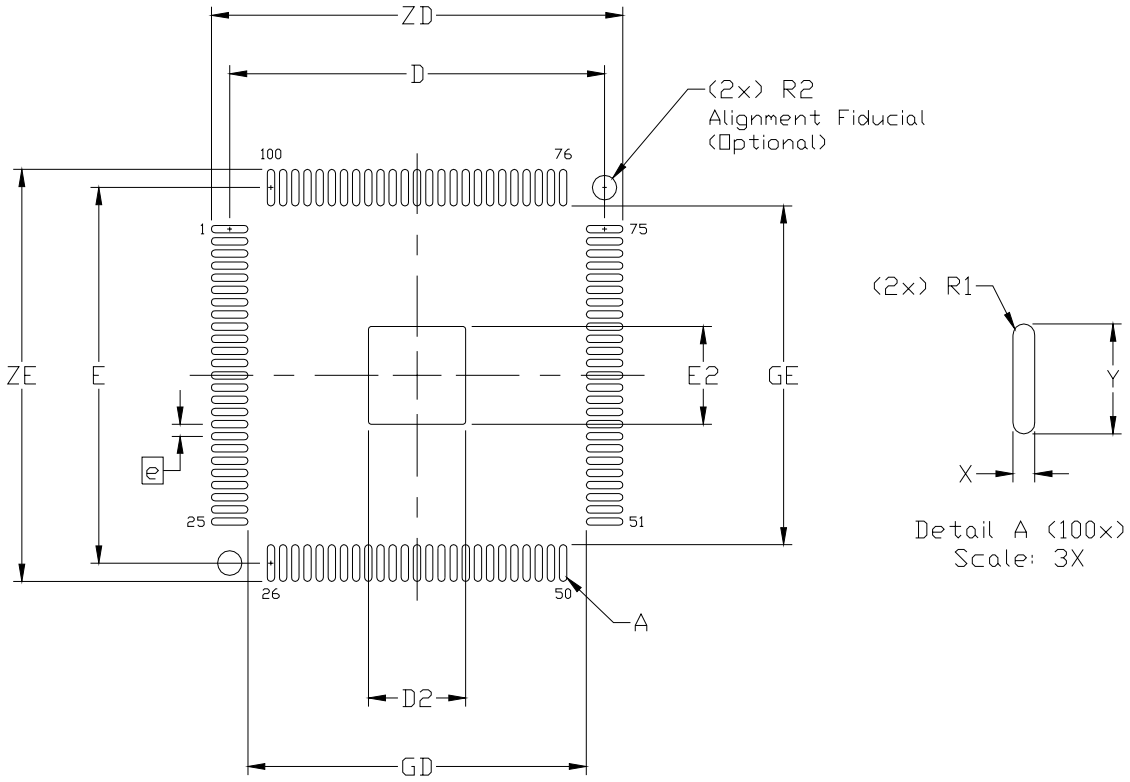


Figure 4. PCB Land Pattern Diagram

Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	15.40 REF.	
D	15.40 REF.	
E2	3.90	4.10
D2	3.90	4.10
GE	13.90	—
GD	13.90	—
X	—	0.30
Y	1.50 REF.	
ZE	—	16.90
ZD	—	16.90
R1	0.15 REF	
R2	—	1.00

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.32 to Revision 0.33

- Condensed format.

Revision 0.33 to Revision 0.34

- Removed references to latency control, INC, and DEC pins.
- Updated Table 1, “Performance Specifications,” on page 2.
- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 3.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated Figure 2, “Si5365 Typical Application Circuit”.
- Updated “2. Pin Descriptions: Si5365”.
- Updated "3. Ordering Guide" on page 12.
- Added “5. Recommended PCB Layout”.

NOTES:

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