

IMAGE SENSOR

CCD area image sensor

S8658-01

Front-illuminated FFT-CCD for X-ray imaging



S8658-01 is a FFT-CCD area image sensor specifically developed for X-ray imaging. Since a FOS (Fiber Optic plate with Scintillator) to convert X-rays into visible light is mounted on the CCD chip, X-ray images can be captured in fine detail. Three CCD chips are linearly arranged in close proximity to form a long and narrow sensor format. Effective size of each active area is $73.728\text{ (H)} \times 6.144\text{ (V)}\text{ mm}^2$, so the overall active area length of the three chips is up to 220 mm in length. Each CCD chip has 1536×128 pixels and the pixel size is $48 \times 48\text{ }\mu\text{m}$.

When used in TDI operation mode which is a special feature of this CCD image sensor, even X-ray images of a moving object can be clearly acquired, making S8658-01 ideal for non-destructive inspection of products carried on a belt conveyor, etc. S8658-01 is pin compatible with S8658: (Operating condition is a little bit changed from S8658)

Features

- FFT-CCD coupled with FOS for X-ray imaging
- $1536\text{ (H)} \times 128\text{ (V)}$ pixel format
- Pixel size: $48 \times 48\text{ }\mu\text{m}$
- Slit-like image of 220 mm long by aligning 3 CCD chips together
- Coupled with FOS for X-ray imaging
- TDI (Time Delay Integration) operation
- 100 % fill factor
- Wide dynamic range
- Low dark current
- MPP operation

Applications

- General X-ray imaging
- Non-destructive inspection
- Dental panorama, cephalo

Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm(V)]
S8658-01	Non-cooled	1536×128	1536×128	73.728×6.144

Note) As an input window, FOS is suited to S8658-01.

General ratings

Parameter	Specification
CCD structure	Full frame transfer or TDI
X-ray sensitive area	$220 \times 6\text{ mm}$
Fill factor	100 %
Number of active pixels	$1536\text{ (H)} \times 128\text{ (V)}^{*1}$
Pixel size	$48\text{ (H)} \times 48\text{ (V)}\text{ }\mu\text{m}$
CCD active area	$73.728\text{ (H)} \times 6.144\text{ (V)}\text{ mm}^{*1}$
Vertical clock phase	2 phase and 2 line
Horizontal clock phase	2 phase and 2 line
Output circuit	Two-stage MOSFET source follower with load resistance
X-ray resolution	4 to 6 Lp/mm at 60 kVp, 10 m Roentgen
Reliability	100,000 shots at 60 kVp, 10 m Roentgen
Package	60 pin ceramic package
Window	FOS (Fiber Optic plate with Scintillator)

*1: Number of active pixels per chip. Three chips are used.

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	-20	-	+70	°C
Operating temperature	Topr	0	-	+40	°C
OD voltage	VOD	-0.5	-	+20	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
IGV voltage	VIGV	-15	-	+15	V
IGH voltage	VIGH	-15	-	+15	V
SG voltage	VSG	-15	-	+15	V
OG voltage	VOG	-15	-	+15	V
RG voltage	VRG	-15	-	+15	V
TG voltage	VTG	-15	-	+15	V
Vertical clock voltage	VP1AV, VP2AV VP1BV, VP2BV	-15	-	+15	V
Horizontal clock voltage	VP1AH, VP2AH VP1BH, VP2BH	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	12	15	18	V
Reset drain voltage		VRD	12	13	14	V
Output gate voltage		VOG	-0.5	2	5	V
Output transistor ground voltage		VSSA	-	0	-	V
Substrate voltage		VSSD	-5	0	-	V
Test point	Vertical input source	VISV	-	VRD	-	V
	Vertical input gate	VIGV	-8	0	-	
	Horizontal input gate	VIGH	-8	0	-	
Vertical shift register clock voltage	High	VP1AVH, VP2AVH VP1BVH, VP2BVH	0	3	6	V
	Low	VP1AVL, VP2AVL VP1BVL, VP2BVL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1AHH, VP2AHH VP1BHH, VP2BHH	0	3	6	V
	Low	VP1AHL, VP2AHL VP1BHL, VP2BHL	-9	-8	-7	
Summing gate voltage	High	VSGH	0	3	6	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	0	3	6	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	0	3	6	V
	Low	VTGL	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc		-	2	4	MHz
Reset clock frequency	frg		-	2	4	MHz
Vertical shift register capacitance	CP1AV, CP2AV CP1BV, CP2BV		-	15000	-	pF
Horizontal shift register capacitance	CP1AH, CP2AH CP1BH, CP2BH		-	500	-	pF
Summing gate capacitance	CSG		-	15	-	pF
Reset gate capacitance	CRG		-	10	-	pF
Transfer gate capacitance	CTG		-	500	-	pF
Transfer efficiency	CTE	*2	0.99995	0.99999	-	
DC output level	Vout	*3	5	8	11	V
Output impedance	Zo	*3	-	500	-	Ω
Power dissipation	P	*3, *4	-	60	-	mW

*2: Measured at half of the full well capacity. CTE is defined per pixel.

*3: VOD=15 V.

*4: Power dissipation of the on-chip amplifier (each chip).

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter			Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat		-	Fw × Sv	-	V
Full well capacity	Vertical		Fw		600	1200	-	ke ⁻
	Horizontal				600	1200	-	
	Summing				600	1200	-	
CCD node sensitivity			Sv	*5	0.45	0.6	-	μV/e ⁻
Dark current (MPP mode)			DS	*6	-	8	24	ke ⁻ /pixel/s
Readout noise			Nr	*7	-	60	120	e ⁻ rms
Dynamic range			DR	*8	5000	20000	-	
X-ray response non-uniformity			XRNU	*9, *10	-	±10	±30	%
Blemish	Point defects *11	White spots	-		-	-	10	-
		Black spots			-	-	10	
	Cluster defects			*12	-	-	0	
	Column defects			*13	-	-	0	
X-ray resolution			ΔR		4	6	-	Lp/mm

*5: V_{OD}=15 V.

*6: Dark current doubles for every 5 to 7 °C.

*7: -40 °C, operating frequency is 2 MHz.

*8: Dynamic range = Full well capacity / Readout noise

*9: X-ray irradiation of 60 kVp, measured at half of the full well capacity.

*10: XRNU (%) = Noise / Signal × 100

Noise: Fixed pattern noise (peak to peak)

Measuring region that is within 220.0 mm (H) × 6.0 mm (V) (refer to dimensional outline)

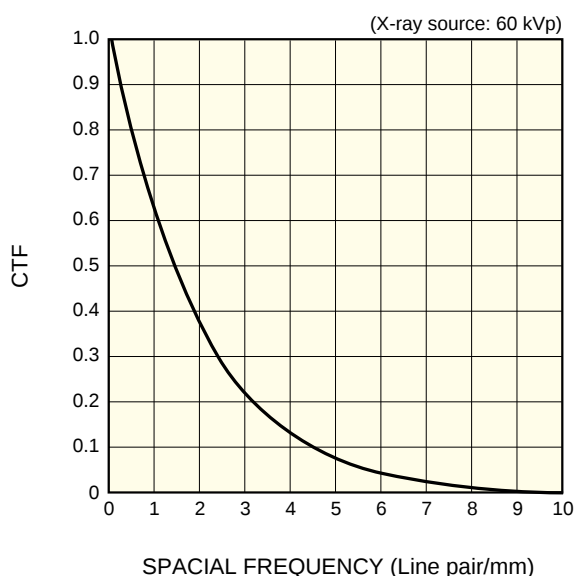
*11: White spots > 20 times of typ. dark signal (8 ke⁻/pixel/s).

Black spots > 50 % reduction in response relative to adjacent pixels, measured at half of the full well capacity.

*12: continuous 2 to 9 point defects.

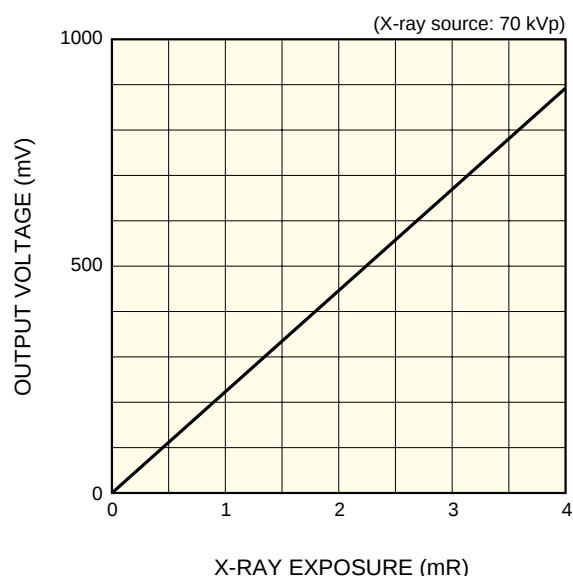
*13: continuous >10 point defects.

■ Resolution



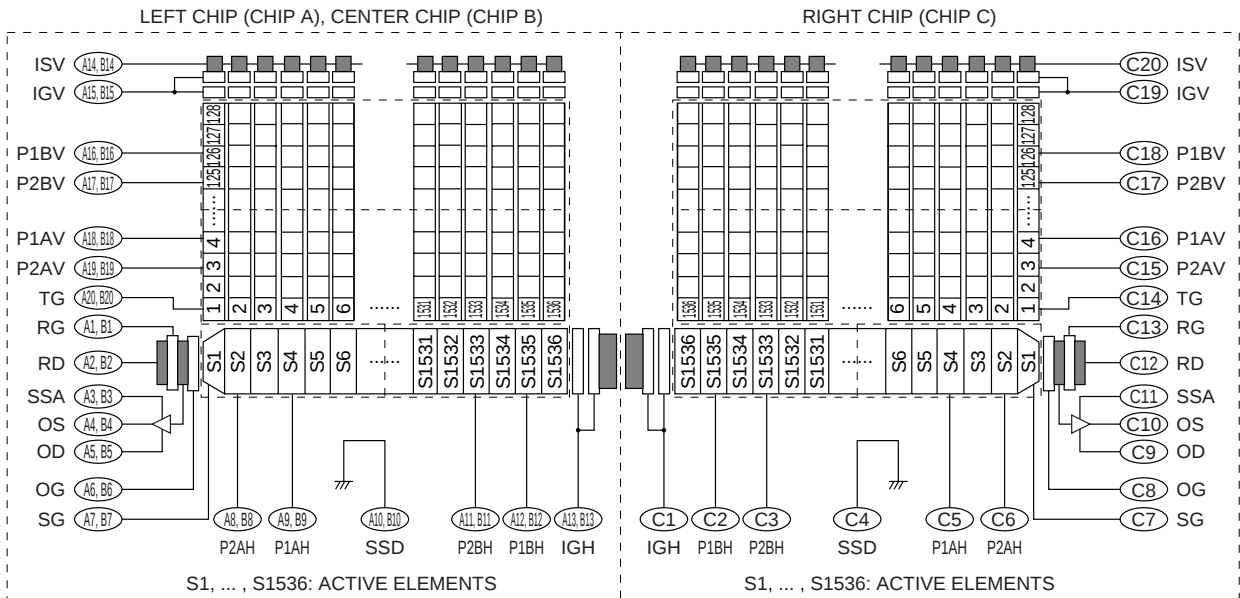
KMPDB0248EA

■ Response



KMPDB0248EA

■ Device structure



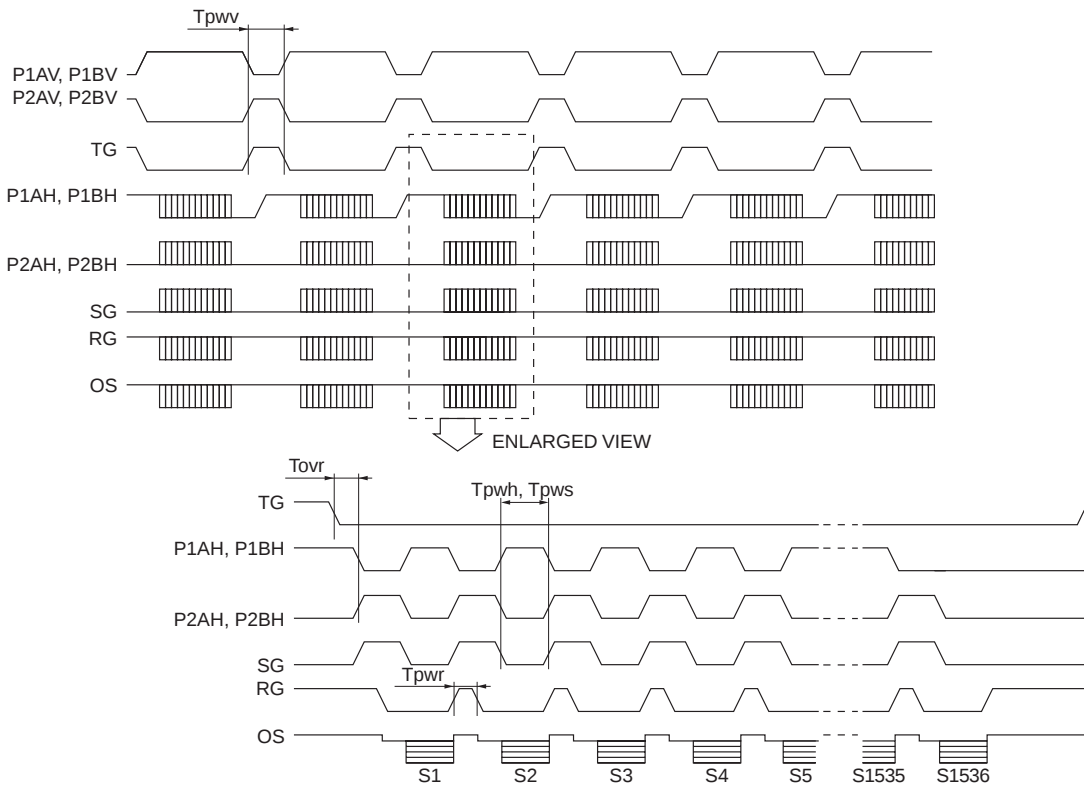
KMPDC0143EA

■ Pixel format

← Left Horizontal Direction → Right						
Blank	Optical black	Isolation	Effective	Isolation	Optical black	Blank
0	0	0	1536	0	0	0

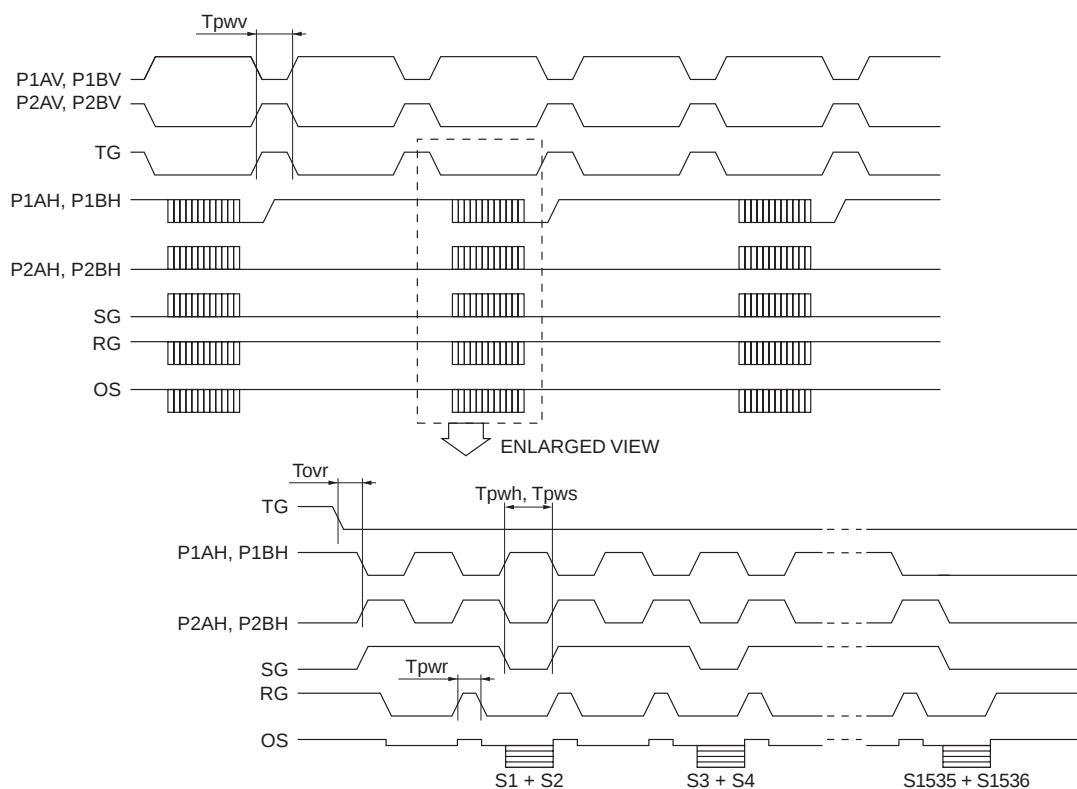
Top ← Vertical direction → Bottom		
Isolation	Effective	Isolation
0	128	0

■ Timing chart (TDI operation)



KMPDC0142EB

■ Timing chart (TDI operation, 2 × 2 pixel binning)



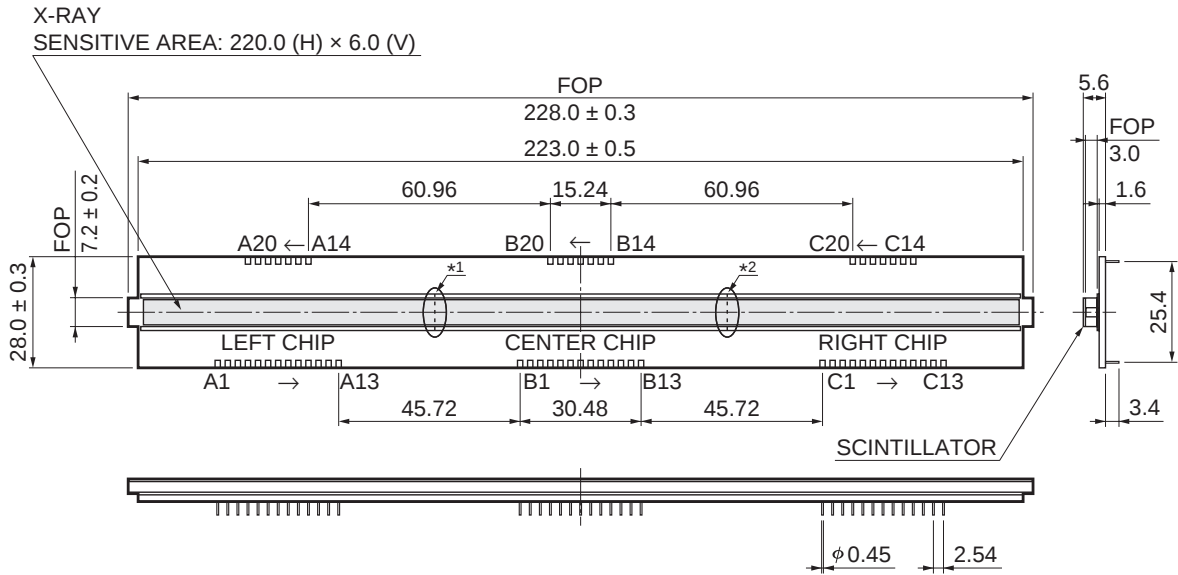
KMPDC0111EC

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1AV, P1BV, P2AV, P2BV, TG	Pulse width	tpwv	*14, *15	30	60	-	μs
	Rise and fall time	tprv, tpfv		200	-	-	ns
P1AH, P1BH, P2AH, P2BH	Pulse width	tpwh	*15	125	250	-	ns
	Rise and fall time	tprh, tpfh		10	-	-	ns
	Duty ratio			-	50	-	%
SG	Pulse width	tpws		125	250	-	ns
	Rise and fall time	tprs, tpfs		10	-	-	ns
	Duty ratio			-	50	-	%
RG	Pulse width	tpwr		10	50	-	ns
	Rise and fall time	tpr, tpf		5	-	-	ns
TG-P1AH, P1BH	Overlap time	tovr		10	20	-	μs

*14: TG terminal can be short-circuited to P2AV terminal.

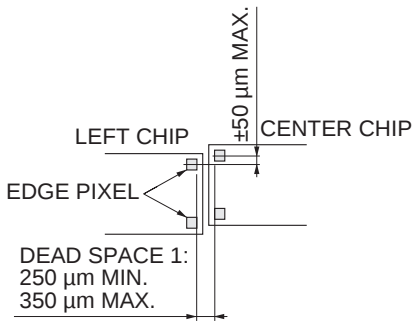
*15: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■ Dimensional outline (unit: mm)

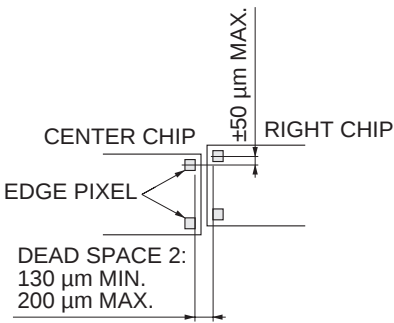


KMPDA0149EC

*1 Details



*2 Details



■ Pin connections

Pin No.	Symbol	Description	Remark
A1, B1	RG	Reset gate	
A2, B2	RD	Reset drain	
A3, B3	SSA	Analog ground	
A4, B4	OS	Output transistor source	
A5, B5	OD	Output transistor drain	
A6, B6	OG	Output gate	
A7, B7	SG	Summing gate	
A8, B8	P2AH	CCD horizontal register clock A-2	
A9, B9	P1AH	CCD horizontal register clock A-1	
A10, B10	SSD	Digital ground	
A11, B11	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
A12, B12	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
A13, B13	IGH	Test point (Horizontal input gate)	
A14, B14	ISV	Test point (Vertical input source)	Shorted to RD
A15, B15	IGV	Test point (Vertical input gate)	
A16, B16	P1BV	CCD vertical register clock B-1	Same timing as P1AV
A17, B17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
A18, B18	P1AV	CCD vertical register clock A-1	
A19, B19	P2AV	CCD vertical register clock A-2	
A20, B20	TG	Transfer gate	
C1	IGH	Test point (Horizontal input gate)	
C2	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
C3	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
C4	SSD	Digital ground	
C5	P1AH	CCD horizontal register clock A-1	
C6	P2AH	CCD horizontal register clock A-2	
C7	SG	Summing gate	
C8	OG	Output gate	
C9	OD	Output transistor drain	
C10	OS	Output transistor source	
C11	SSA	Analog ground	
C12	RD	Reset drain	
C13	RG	Reset gate	
C14	TG	Transfer gate	
C15	P2AV	CCD vertical register clock A-2	
C16	P1AV	CCD vertical register clock A-1	
C17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
C18	P1BV	CCD vertical register clock B-1	Same timing as P1AV
C19	IGV	Test point (Vertical input gate)	
C20	ISV	Test Point (Vertical input source)	Shorted to RD

■ Precautions for use (Electrostatic countermeasures)

- * Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- * Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- * Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- * Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.