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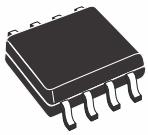
STS4DNF30L

Dual N-channel 30V - 0.039Ω - 4A SO-8 STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS4DNF30L	30V	<0.050Ω	4A

- Standard outline for easy automated surface mount assembly
- Low threshold drive

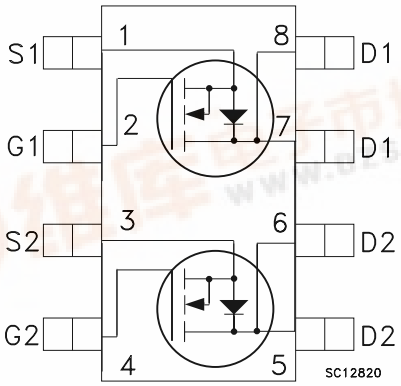


S0-8

Description

This Power MOSFET is the second generation of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STS4DNF30L	S4DNF30L	SO-8	Tape & reel

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Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (v_{gs} = 0)	30	V
V_{GS}	Gate- source voltage	±16	V
I_D	Drain current (continuos) at T_C = 25°C	4	A
I_D	Drain current (continuos) at T_C = 100°C	2.5	A
I_{DM} (1)	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at T_C = 25°C dual operating	2	W

1. Pulse width limited by safe operating area

Table 2. Thermal data

$R_{thj\text{-}a}$	(1)Thermal resistance junction-ambient Max	62.5	°C/W
T_J	Junction temperature	-55 to 150	°C
T_{stg}	Storage temperature range	150	°C

1. Mounted on FR-4 board (t≤10sec)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS}=Max rating, T_C=125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 2A V_{GS} = 4.5V, I_D = 2A		0.039 0.046	0.050 0.060	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D= 4 A	1	3		S
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		330		pF
C_{oss}	Output capacitance			90		pF
C_{rss}	Reverse transfer capacitance			40		pF
Q_g	Total gate charge	V_{DD} = 24V, I_D = 4A, V_{GS} = 10V		6.5	9	nC
Q_{gs}	Gate-source charge			3.6		nC
Q_{gd}	Gate-drain charge			2		nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=15 V, I_D=2A, R_G=4.7Ω, V_{GS}= 4.5V (see Figure 12)		11 100		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=15 V, I_D=2A, R_G=4.7Ω, V_{GS}= 4.5V (see Figure 12)		25 22		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				4	A
I_{SDM} (1)	Source-drain current (pulsed)				16	A
V_{SD} (2)	Forward on voltage	I_{SD} = 4A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4A, V_{DD} = 20V di/dt = 100A/µs, T_j = 150°C (see Figure 14)		30 18 1.2		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

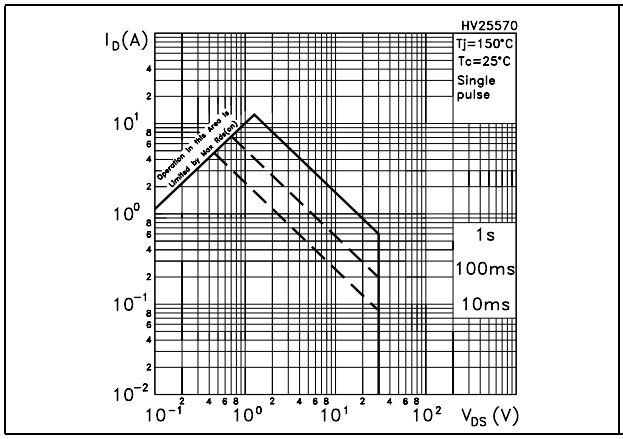


Figure 2. Thermal impedance

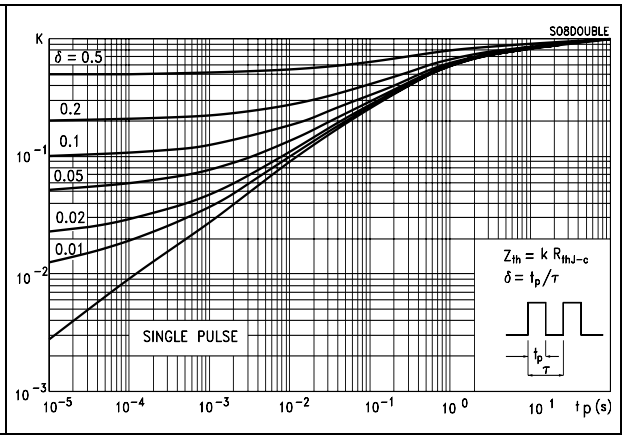


Figure 3. Output characterisics

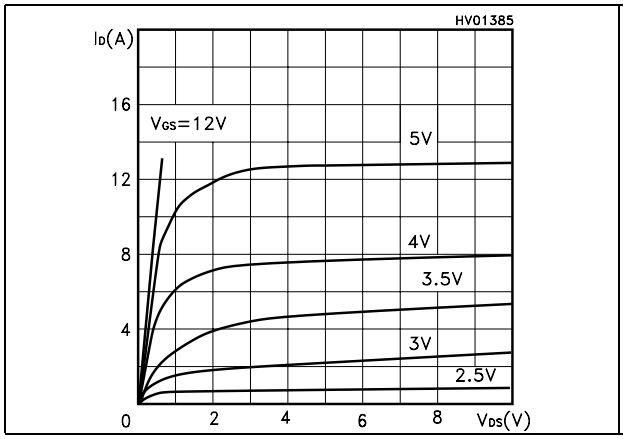


Figure 4. Transfer characteristics

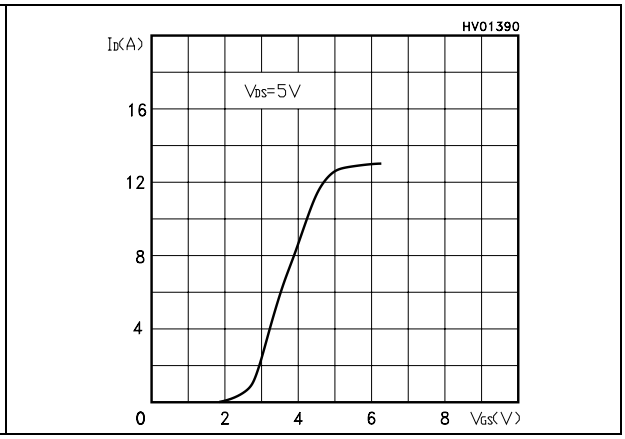


Figure 5. Transconductance

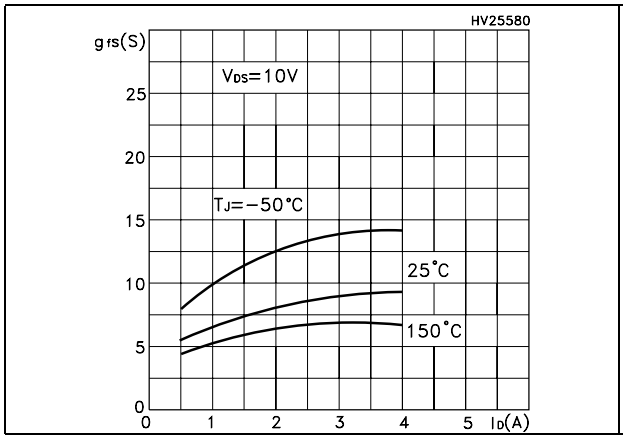


Figure 6. Static drain-source on resistance

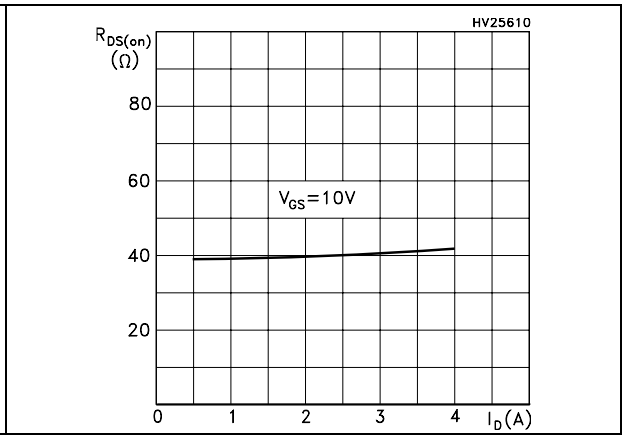


Figure 7. Gate charge vs gate-source voltage

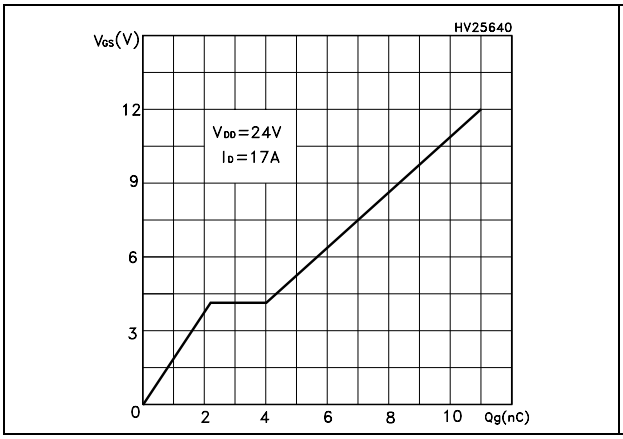


Figure 8. Capacitance variations

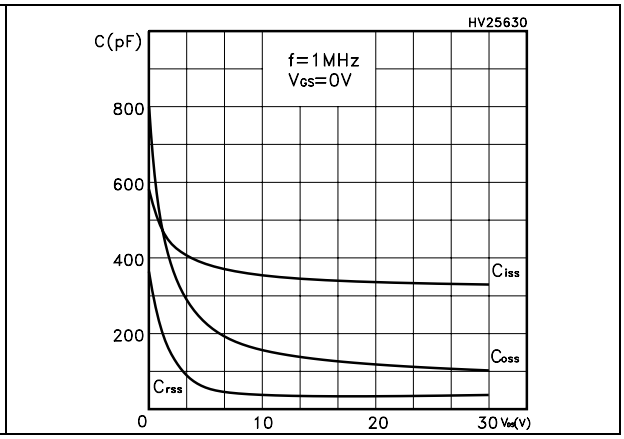


Figure 9. Normalized gate threshold voltage vs temperature

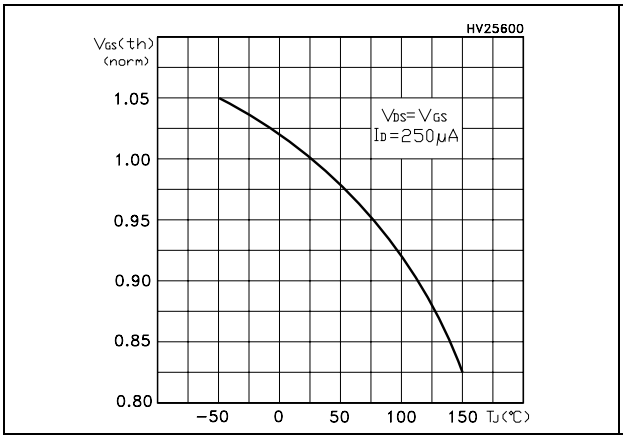


Figure 10. Normalized on resistance vs temperature

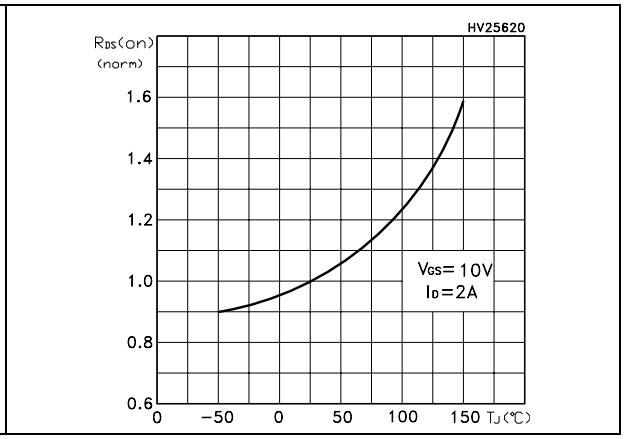
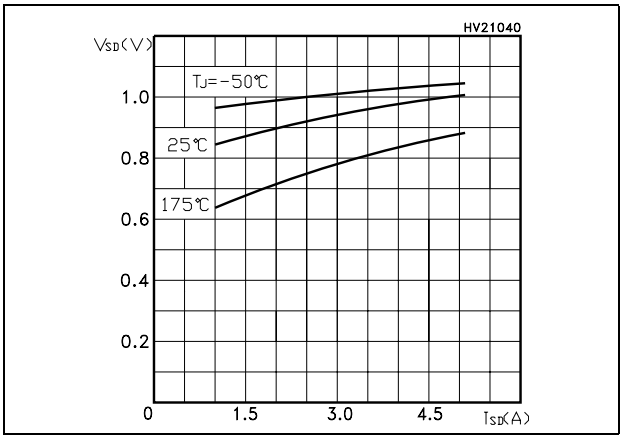


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

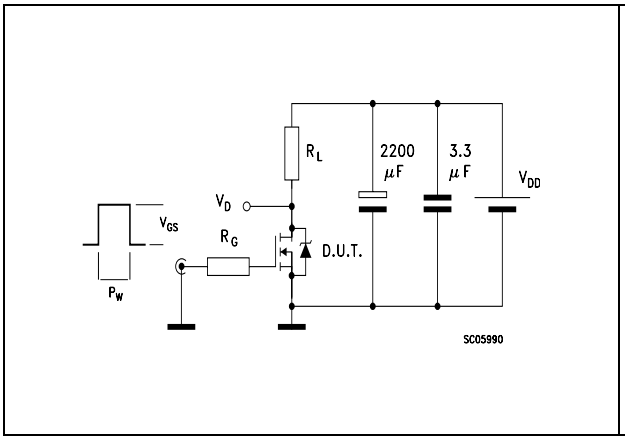


Figure 13. Gate charge test circuit

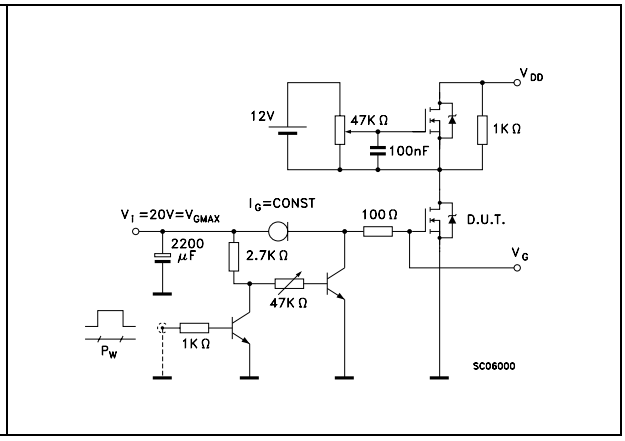


Figure 14. Test circuit for inductive load switching and diode recovery times

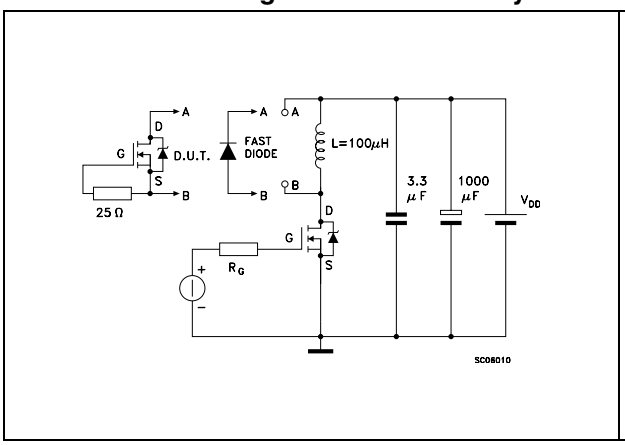


Figure 15. Unclamped Inductive load test circuit

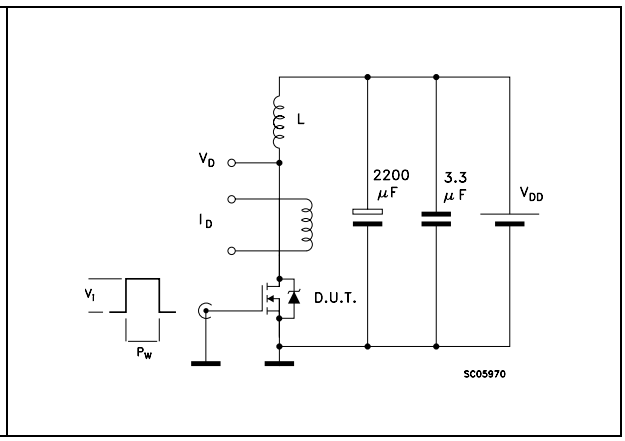


Figure 16. Unclamped inductive waveform

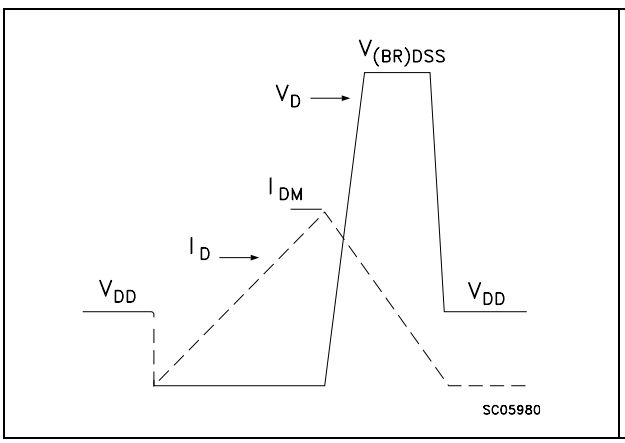
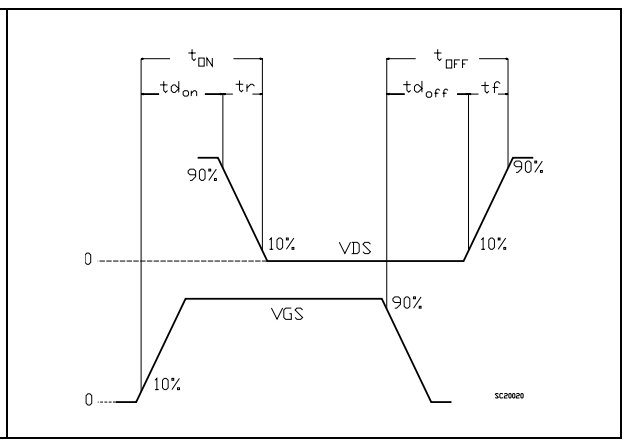


Figure 17. Switching time waveform

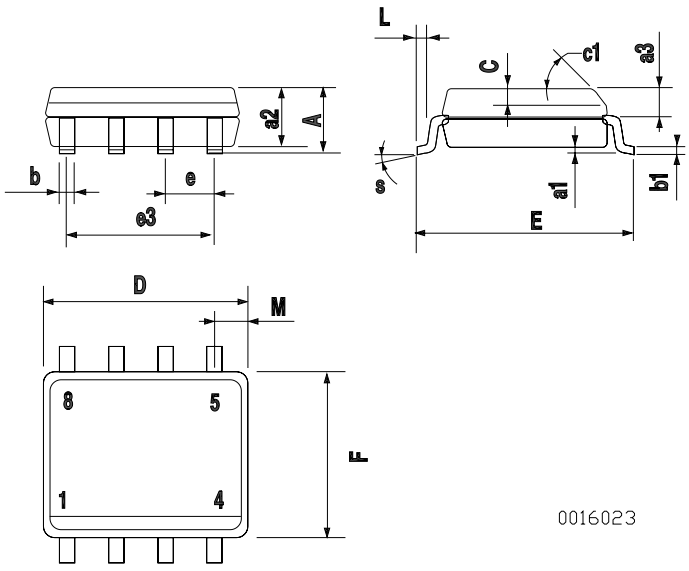


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
11-Sep-2006	1	First version
15-Nov-2006	2	The document has been reformated

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