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requested by a CPU. It provides connection with a CPU via two
and has two systems of interrupt/alarm and clock output feat
allowing the alleviation of software treatment on the side of a
It also works on lower power with the oscillating circuit operated
constant voltage. Its package uses an extremely small and thin ty
eight-pin SSOP.

■ Features

- Low power consumption : 0.7 µA typ. (V_{DD}=3.0 V)
- Wide area of operating voltage : 1.7 to 5.5 V
- BCD input/output of year, month, day, day of a week, hour, minute and second
- CPU interface via two wires (I^2C- BUS)
- Auto calender till the year of 2,099 (automatic leap year arithmetic feature included)
- Built-in power voltage detecting circuit
- Built-in constant voltage circuit
- Built-in flag generating circuit on power on/off
- Built-in alarm interrupter
- Steady-state interrupt frequency/duty setting feature
- Built-in 32 KHz crystal oscillating circuit (Internal Cd, External Cg)
- 8-pin SSOP package (terminal pitch: 0.65 mm)

(*) I^2C-BUS is a trademark of PHILLIPS ELECTRONICS N.V.

■ Applications

- Cellular phone
- PHS
- A variety of pagers
- TV set and VCR
- Camera

■ Block Diagram

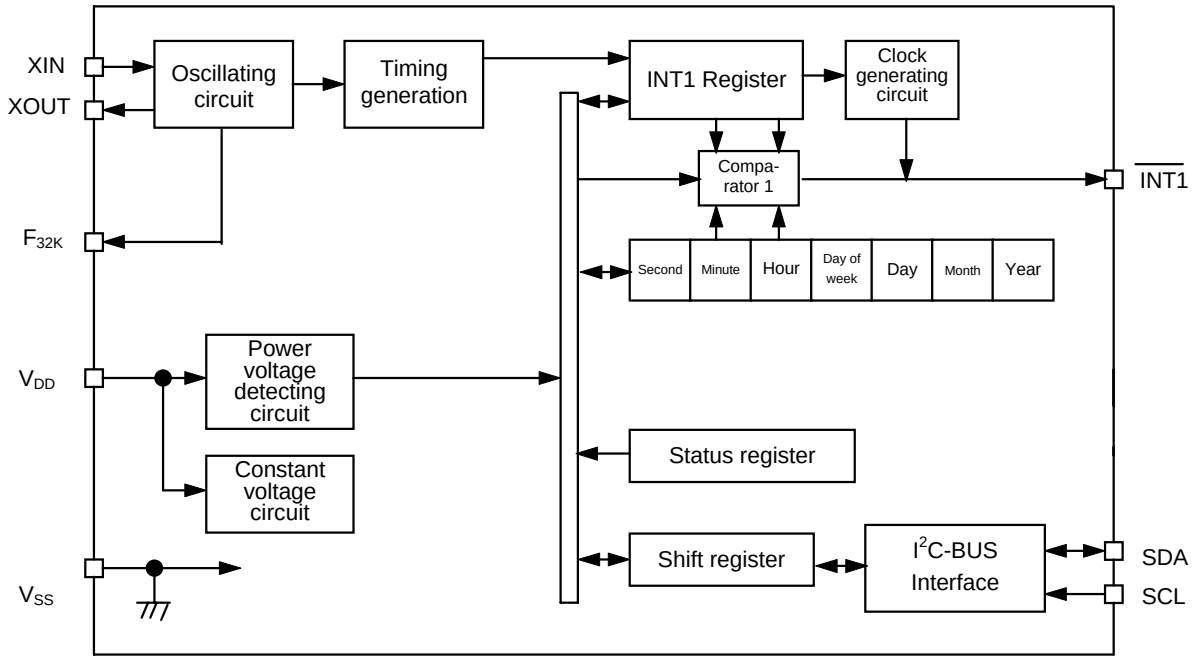


Figure 1 Block diagram

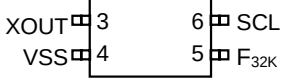


Figure 2 Pin assignment

■ Description of Terminals

Terminal Num.	Abbreviation	Description	Configuration
1	$\overline{\text{INT1}}$	Alarm interrupt 1 output terminal. Depending on the mode set by the $\overline{\text{INT1}}$ register and status register, it outputs low or Clock when time is reached. It is disabled by rewriting the status register.	N-channel open drain output (No protective diode on the side of VDD)
2	XIN	Crystal oscillator connect terminal (32,768 Hz) (Internal Cd, External Cg)	—
3	XOUT		
4	VSS	Negative power supply terminal (GND)	—
5	F_{32K}	32,768 Hz clock output terminal. This clock is always being output and cannot be controlled by command.	N-channel open drain output (No protective diode on the side of VDD)
6	SCL	Serial clock input terminal. Follow the specification with great care to the rising/falling time of the SCL signal because the signal is treated at its rising/falling edge.	CMOS input (No protective diode on the side of VDD)
7	SDA	Serial data input/output terminal. It is normally used with pulled up to VDD charge via resistance and wired or connected to other devices with open drain or open collector output	N-channel open drain output (No protective diode on the side of VDD) CMOS input
8	VDD	Positive power supply terminal.	—

Table 1 Description of terminals

1-1. Start condition

When the SCL line is on the “H” level, the line changes from “H” to “L” so that the start condition is obtained. A operations begin at the start condition.

1-2. Stop condition

When the SCL line is on the “H” level, the line changes from “L” to “H” so that the stop condition is reached. D a read sequence, any read operation is stopped and a device enters its stand-by mode when a stop condi received.

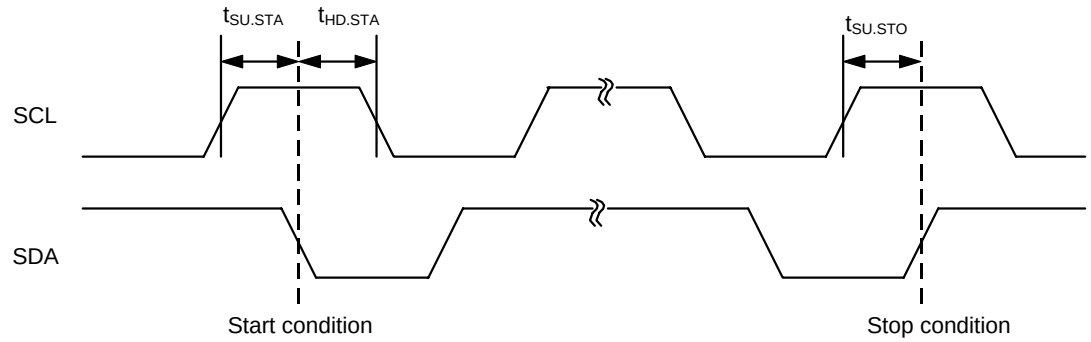


Figure 3 Start/Stop condition

1-3. Data transfer

When the SDA line is changed while it is on “L”, data transfer is performed.
When the SDA line is changed while it is on “H”, a start or stop condition is recognized.

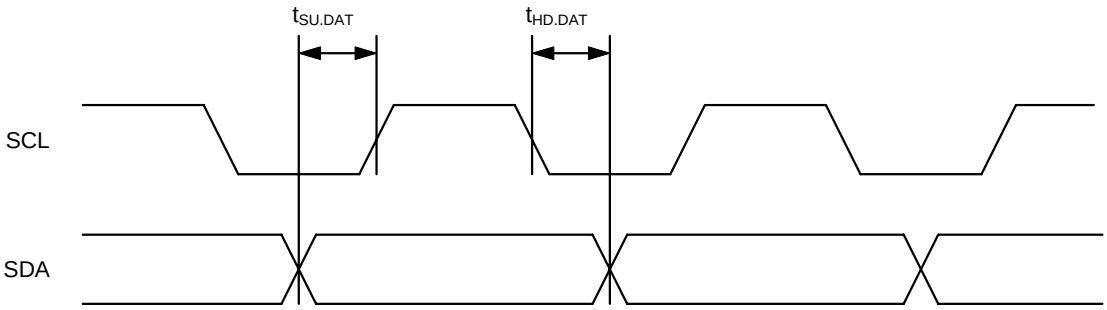


Figure 4 Data transfer timing

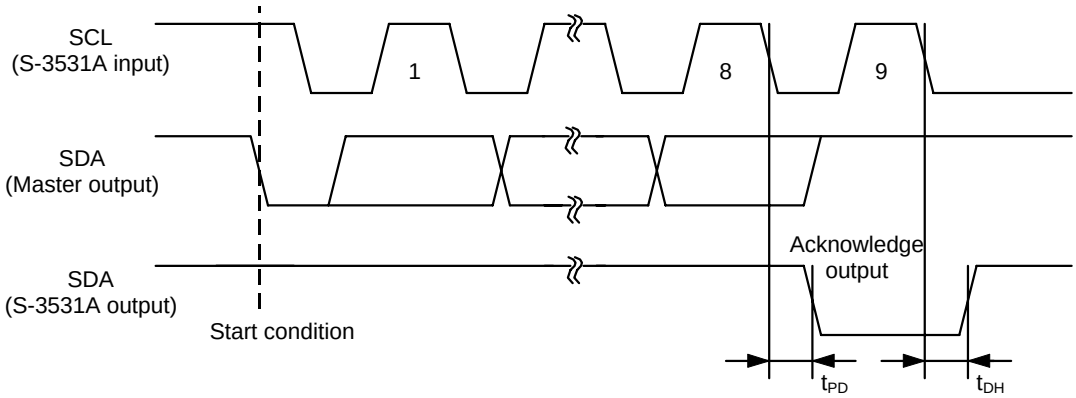


Figure 5 Acknowledge output timing

1-5. Device addressing

The master device on the system generates a start condition to its slave device to make communication. It continuously issues the device address of a four-bit length, the command of a three-bit length and the read/write command of a one-bit length over the SDA bus.

The upper four bits, called a device code, represent a device address and are fixed at “0110”.

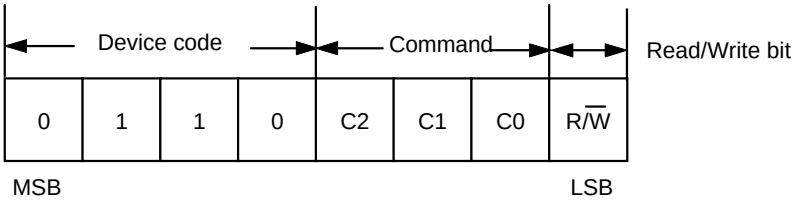
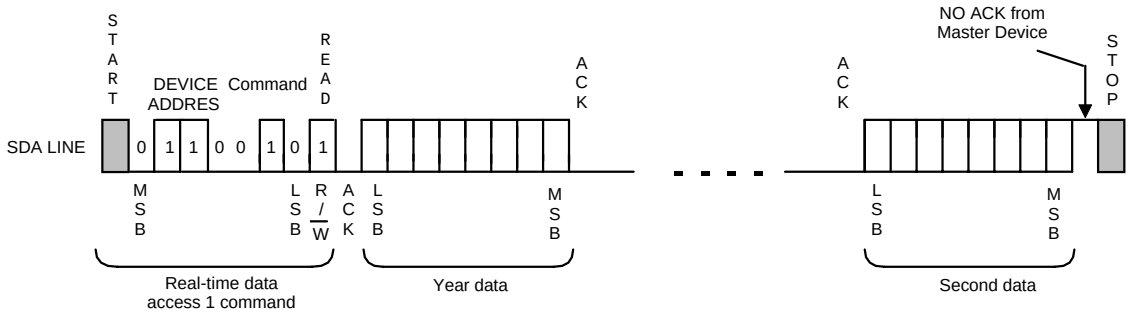
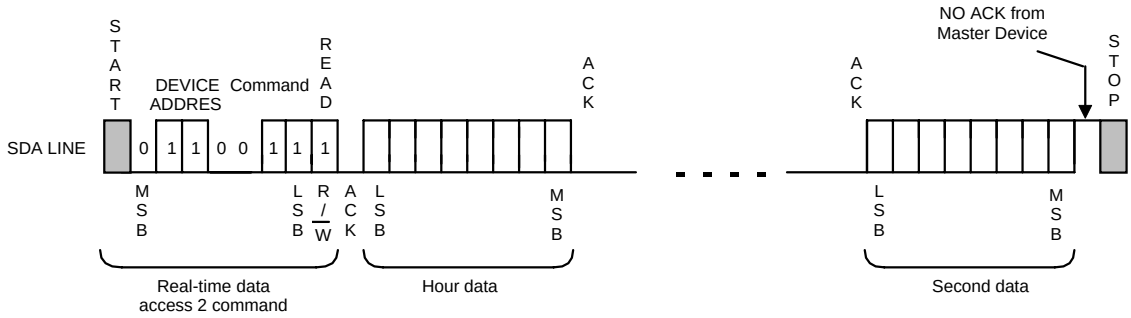


Figure 6 Communication data

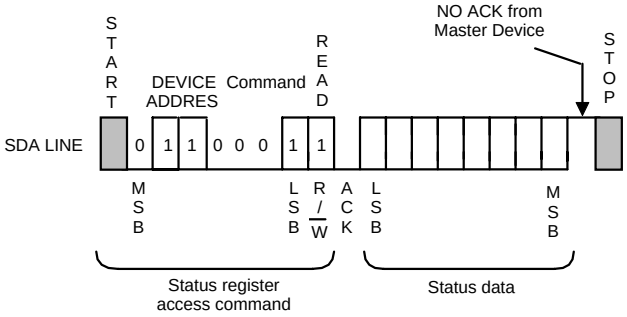
(1)Real-time data reading 1



(2)Real-time data reading 2



(3)Status register reading

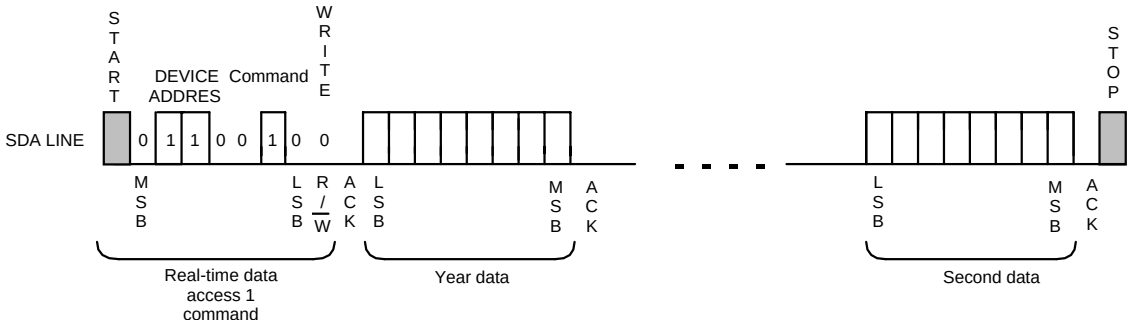


«NOTE»
ACK Top:Generate from master device
Bottom:Generate from S-3531A

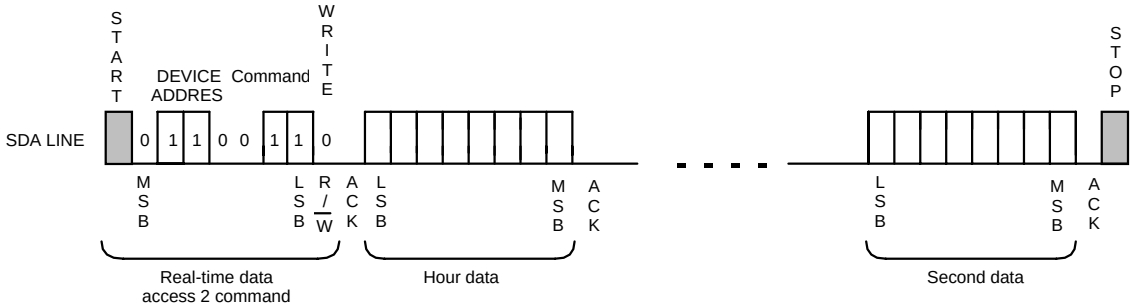
Figure 7 Read communication

writing command, and any update operation is disabled. After a minute data is received, the end of a month is corrected while a second data is imported. Then, the count is started when the ACK signal rises after the second data is received.

(1)Real-time data writing 1



(2)Real-time data writing 2



(3)Status register writing

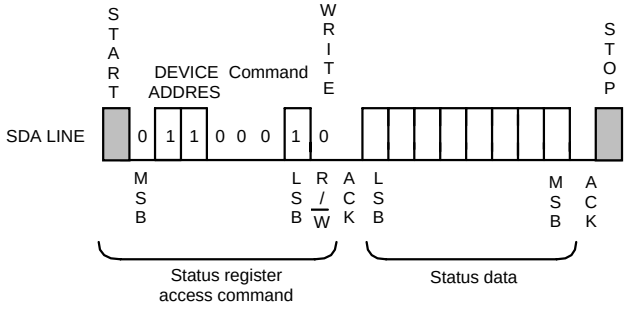
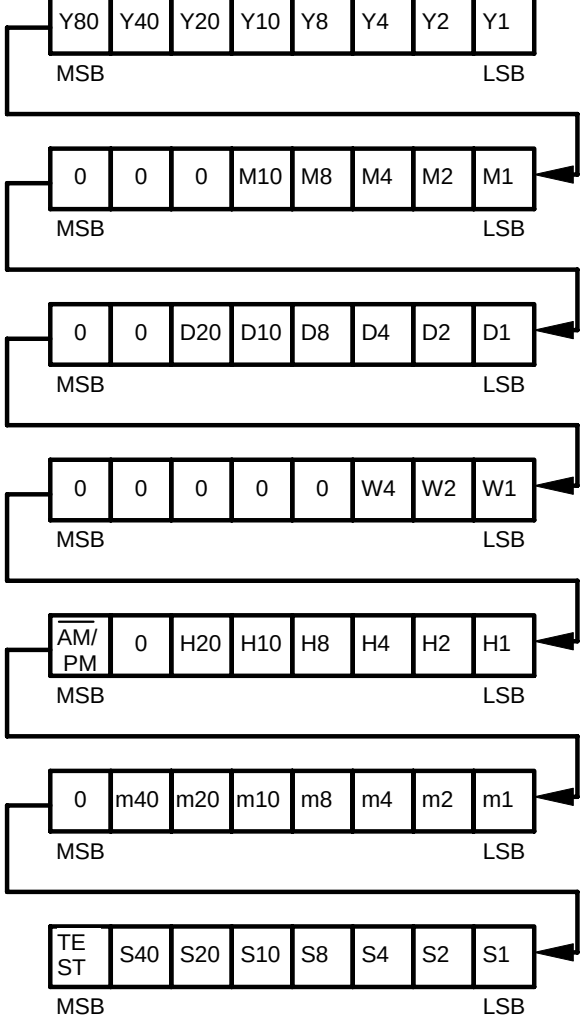


Figure 8 Write communication

C2	C1	C0	Description	Number of ACK
0	0	0	Reset (00 (year), 01 (month), 01 (day), 0 (day of week), 00 (minute), 00 (second)) (*1)	1
0	0	1	Status register access	2
0	1	0	Real-time data access 1 (year data to)	8
0	1	1	Real-time data access 2 (hour data to)	4
1	0	0	Alarm time/frequency duty setting 1 (for $\overline{\text{INT1}}$ terminal)	3
1	1	0	Test mode start (*2)	1
1	1	1	Test mode end (*2)	1

(*1) Don't care the R/W bit of this command.
(*2) This command is access-disabled due to specific use for the $\overline{\text{IC}}$ test.

Table 2 Command list



Year data (00 to 99)

Sets the lower two digits of the Christian era (00 to 99) and links together with the auto calender feature till 2,099.

Month data (01 to 12)

The count value is automatically changed by the auto calender feature:

1, 3, 5, 7, 8, 10, 12: 1 to 31
4, 6, 9, 11: 1 to 30
2 (leap year): 1 to 29
2 (common year): 1 to 28

Day data (01 to 31)

Day of week data (00 to 06)
A septenary counter. Set it so that it corresponds to the day of the week.

Hour data (00 to 23 or 00 to 11)

$\overline{\text{AM}}$/PM : For 12-hour expression, 0:AM and 1:PM. For 24-hour expression, this flag has no meaning but either 0 or 1 must be written.

Minute data (00 to 59)

Second data (00 to 59) and test flag

TEST : Turns to “1” during the test mode.

Figure 9 Real-time data register

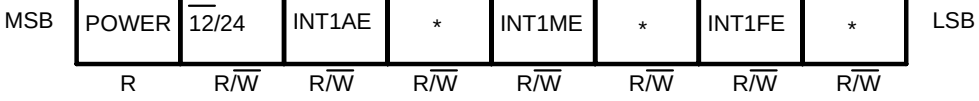


Figure 10 Status register

B7:POWER This flag turns to "1" if the power voltage detecting circuit operates during power-on or ch in power voltage (below VDET). Once turning to "1," this flag does not turns back to "0" when the power voltage reaches or exceeds the detected voltage. When the flag is "1 must send the reset command and turn it to "0." It is a read-only flag.

B6:12/24 This flag is used to set 12-hour or 24-hour expression.

0 : 12-hour expression
1 : 24-hour expression

B5:INT1AE

This flag is used to choose the state of INT1 terminal output with interrupt output set. E this flag after setting alarm time that forms a meeting condition in the INT1 register:

0 : Alarm interrupt output is disabled.
1 : Alarm interrupt output is enabled.

B3:INT1ME

This flag is used to make the output of the INT1 terminal per-minute edge interrupt or per-m steady interrupt. To make the output per-minute steady interrupt, set "1" at INT1ME and IN .

0 : Alarm interrupt or selected frequency steady interrupt output
1 : Per-minute edge interrupt or per-minute steady interrupt output

B1:INT1FE

This flag is used to make the output of the INT1 terminal per-minute steady interrupt out period of one minute, 50% of duty) or selected frequency steady interrupt. Note that the register is considered as the data of frequency/duty if selected frequency steady interr chosen.

0 : Alarm interrupt or selected frequency steady interrupt output
1 : Per-minute edge interrupt or per-minute steady interrupt output

B4,B2,B0: * Non-used bits; They are ignored during the data writing. Indefinite data ("0" or "1") is during the data reading.

rightly then set hour data is not met to alarm data. The alarm time/frequency duty setting register is a write-only register.

(1) When INT1AE = 1

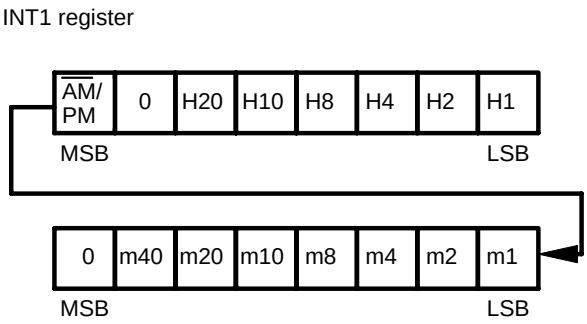
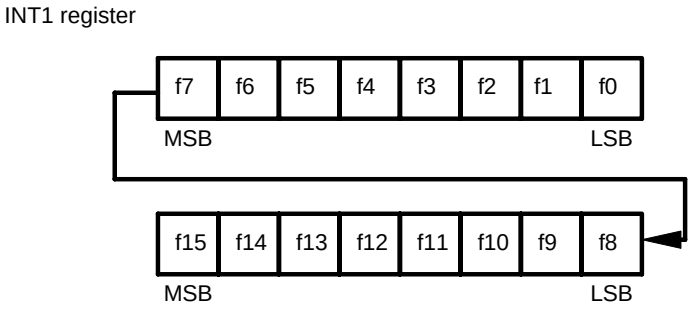


Figure 11 INT1 register (alarm)

INT1 register is considered as alarm time data. Having the same configuration as the time and minutes registers of real-time register configuration, they represent hours and minutes with BCD codes. When setting them, do not set any none-existent day. Data to be set must be in accordance with 12-hour or 24-hour expression that is set at the status register.

(2) When INT1FE = 1

INT1 register is considered as frequency duty data. By turning each bit of the registers to "1," a frequency corresponding to each bit is chosen in an ANDed form.



f0	32768 Hz	f4	2048 Hz	f8	128 Hz	f12	8 Hz
f1	16384 Hz	f5	1024 Hz	f9	64 Hz	f13	4 Hz
f2	8192 Hz	f6	512 Hz	f10	32 Hz	f14	2 Hz
f3	4096 Hz	f7	256 Hz	f11	16 Hz	f15	1 Hz

Figure 12 INT1 register (frequency duty)

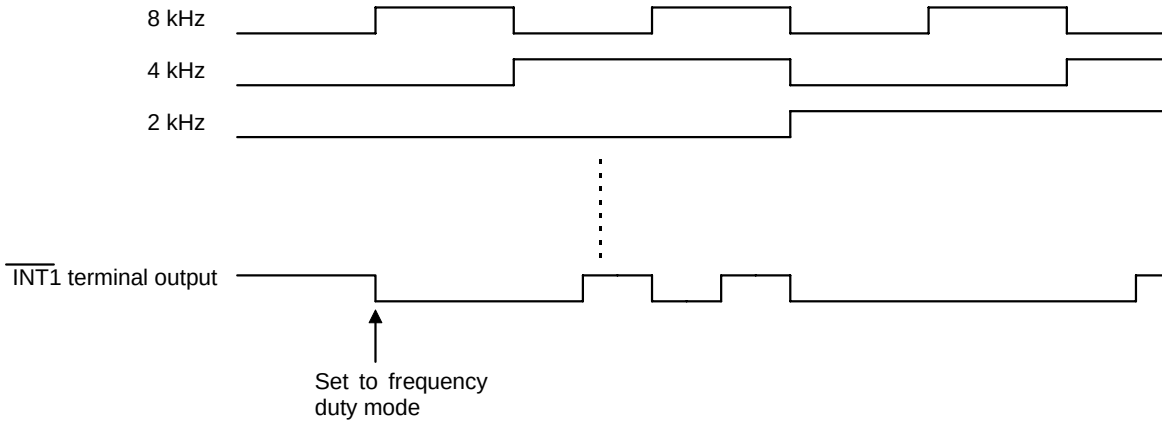


Figure 13 Clock output

2-4. Test flag

The test flag is a one-bit register which is assigned to MSB of the second data of the real-time data re
If a transferred data is considered as the test mode starting data due to the receiving of the test mode s
data or noises, "1" is set. When "1" is set, you must send the test mode ending command or reset comman

3. Initialization

Note that S-3531A has different initializing operations, depending on states.

3-1. When power is turned on

When power is turned on, the status register is set to "82h" and the INT1 register to "8000h" by the pow
detecting circuit. In other words, "1" is sets at the bit 7 (POWER flag) of the status register and the clock o
is output from the $\overline{\text{INT1}}$ terminal. This is provided to adjust oscillating frequencies. In normal use, the
command must be sent when power is turned on.

Real-time data register : 00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register : "82h"
INT1 register : "8000h"

3-2.When the power voltage detecting circuits operates

The power voltage detecting circuit included in S-3531A operates and sets "1" at the bit 7 (POWER fl
the internal status register when power is turned on or power voltage is reduced. Once "1" is set, it is held
after the power voltage gets equal to or higher than the detected power voltage. When the flag has "1", you
send the reset command from CPU and initialize the flag. At this point, other registers does not ch
However, if the POWER flag has "0" during the power-on reset of CPU (S-3531A does not reach any ind
area during backup), you do not have to send the reset command.

3-3. When the reset command is received

When the reset command is received, each register turns as follows:

Real-time data register : 00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register : "00h"
INT1 register : "0000h"

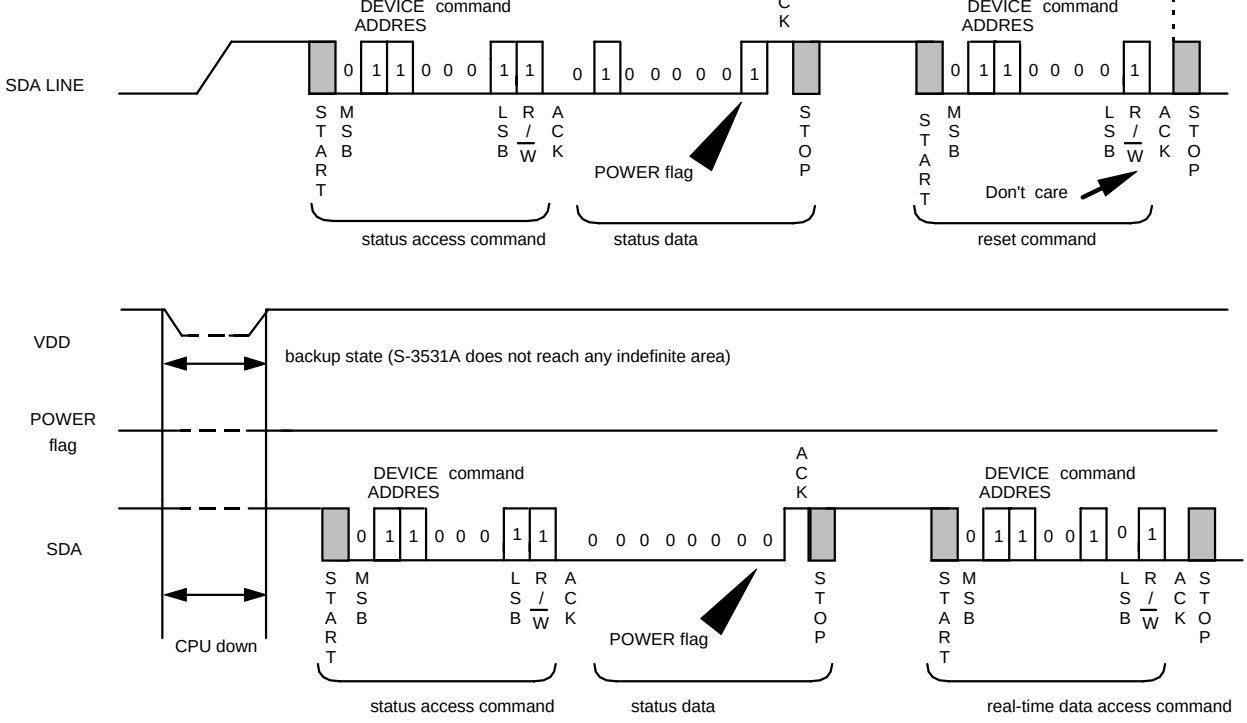


Figure 14 Initializing

4. Processing of none-existent data and end-of-month

When writing real-time data, validate it and treat any invalid data and end-of-month correction.

[None-existent data processing] Table 3 None-existent data processing

Register	Normal data	Error data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XA to XF	01
Day data	01 to 31	00, 32 to 39, XA to XF	01
Day of week data	0 to 6	7	0
Hour data (24-hour) (*) (12-hour)	0 to 23 0 to 11	24 to 29, 3X, XA to XF 12 to 19, XA to XF	00 00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data (**)	00 to 59	60 to 79, XA to XF	00

(*) For 12-hour expression, write the $\overline{\text{AM}}$/PM flag.
The $\overline{\text{AM}}$/PM flag is ignored in 24-hour expression, but "0" for 0 to 11 o'clock and "1" for 12 to 23 o'clock are read in a read operation.

(**) None-existent data processing for second data is performed by a carry pulse one second after the end of writing. At this point, the carry pulse is sent to the minute

[End-of-month correction]

Any none-existent day is corrected to the first day of the next month. For example, February 30 is changed to March 1. Leap-year correction is also performed here.

(1) Alarm interrupt output

Alarm interrupt is enabled by setting hour and minute data to the INT1 register and turning the status register's IN to "1" and INT1ME and INT1FE to "0" . When set hour data is met, low is output from the $\overline{INT1}$ terminal. Sinc output is held, rewrite INT1AE of the status register to "0" through serial communication to turn the output to high state). When you perform DISABLE or ENABLE communication while the corresponding signal is being retaine one minute), "Low" signal is output from the $\overline{INT1}$ terminal again.

(2) Selected frequency steady interrupt output

When you set frequency/duty data to the INT1 register and turn the status register's INT1ME to "0" and INT1FE clock set at the INT1 register is output from the $\overline{INT1}$ terminal.

(3) Per-minute edge interrupt output

When a first minute carry is performed after the status register's INT1ME is set with "1" and INT1FE with "0" , output from the $\overline{INT1}$ terminal . Since the output is held, rewrite INT1AE, INT1ME and INT1FE of the status regis "0" through serial communication to turn the output to high (OFF state). When you perform DISABLE or EN communication while the minute carry processing signal is being retained (for 10 msec), "Low" signal is output fro $\overline{INT1}$ terminal again.

(4) Per-minute steady interrupt output

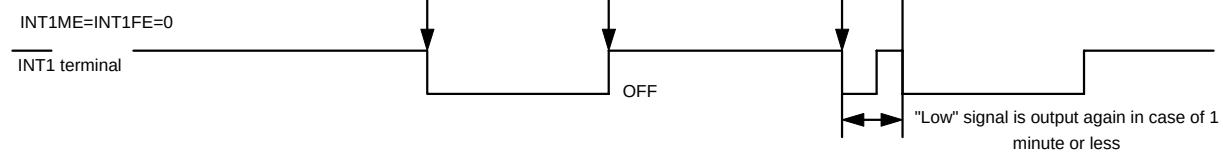
When a first carry is performed after the status register's INT1ME and INT1FE are set with "1" , clock is output fro $\overline{INT1}$ terminal with a period of one minute (50% duty). When you perform DISABLE or ENABLE communication the $\overline{INT1}$ terminal is at "L," "Low" signal is output from the $\overline{INT1}$ terminal again.

Note 1 : If changing an output mode, give care to the state of the INT1 register and output.
Note 2 : If per-minute edge interrupt output or per-minute steady interrupt output is chosen, the INT1 register h meaning.

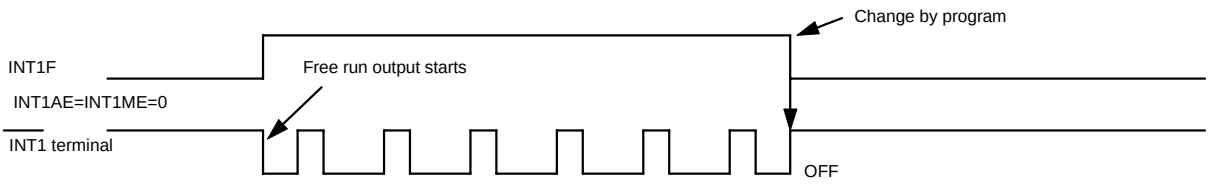
Table 4 Interrupt description

NO.	INT1AE	INT1ME	INT1FE	Description
0	0	0	0	Output disabled (No interrupt output)
1	*	0	1	Selected frequency steady interrupt output
2	*	1	0	Per-minute edge interrupt output
3	*	1	1	Per-minute steady interrupt output
4	1	0	0	Per-minute alarm interrupt output

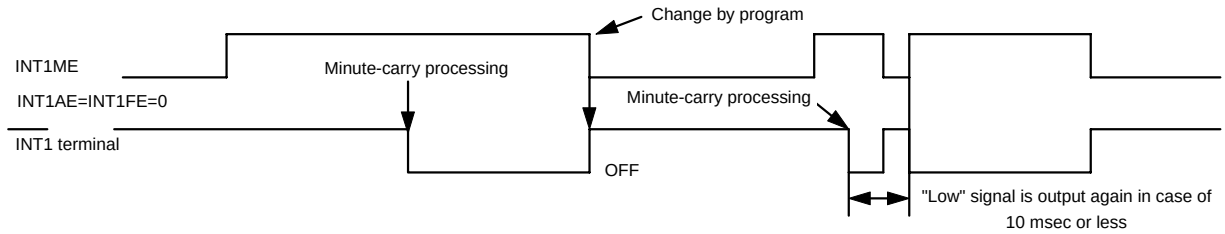
Note * : Don't care.



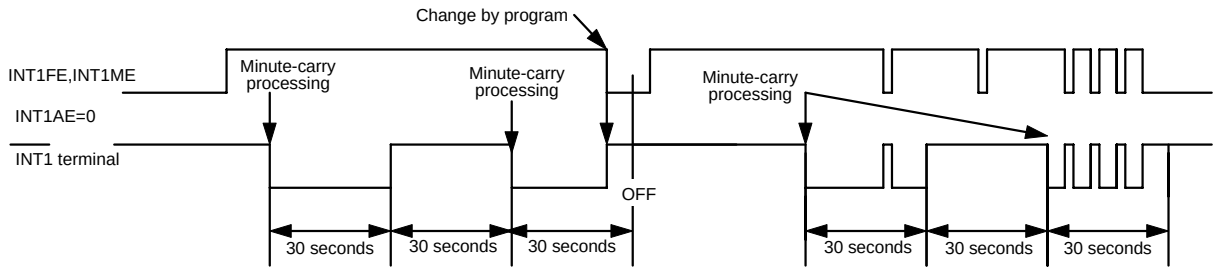
(2) Selected frequency steady interrupt output



(3) Per-minute edge interrupt output



(4) Per-minute steady interrupt output



(5) During power-on detecting circuit operation

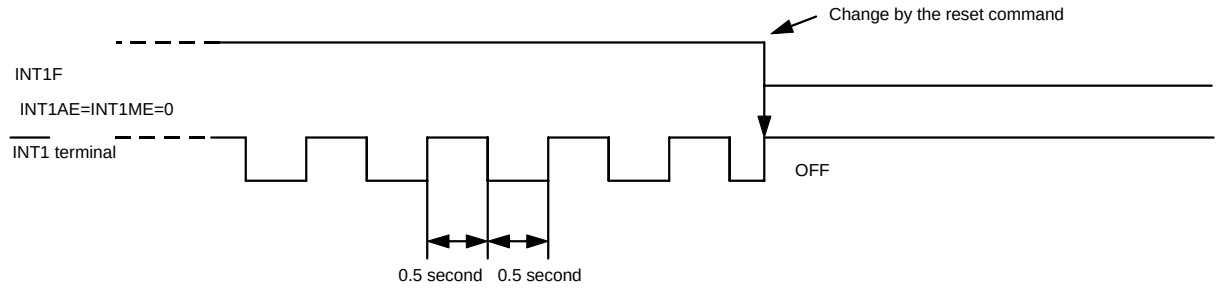


Figure 15 Output mode

Decrease in power voltage can be monitored by reading the POWER flag.

That is to say, once decrease in power voltage is detected, any detecting operation is not performed and "H" is held unl you perform initialization or send the status read command.

[Note]

When power voltage is increased and the first read operation is performed after decrease in power voltage occurs a latch circuit latches "H", "1" can be read on the POWER flag. However, if the next read operation is performed aft sampling of the detecting circuit, the POWER flag is reset since sampling is subsequently allowed. See the timing di below.

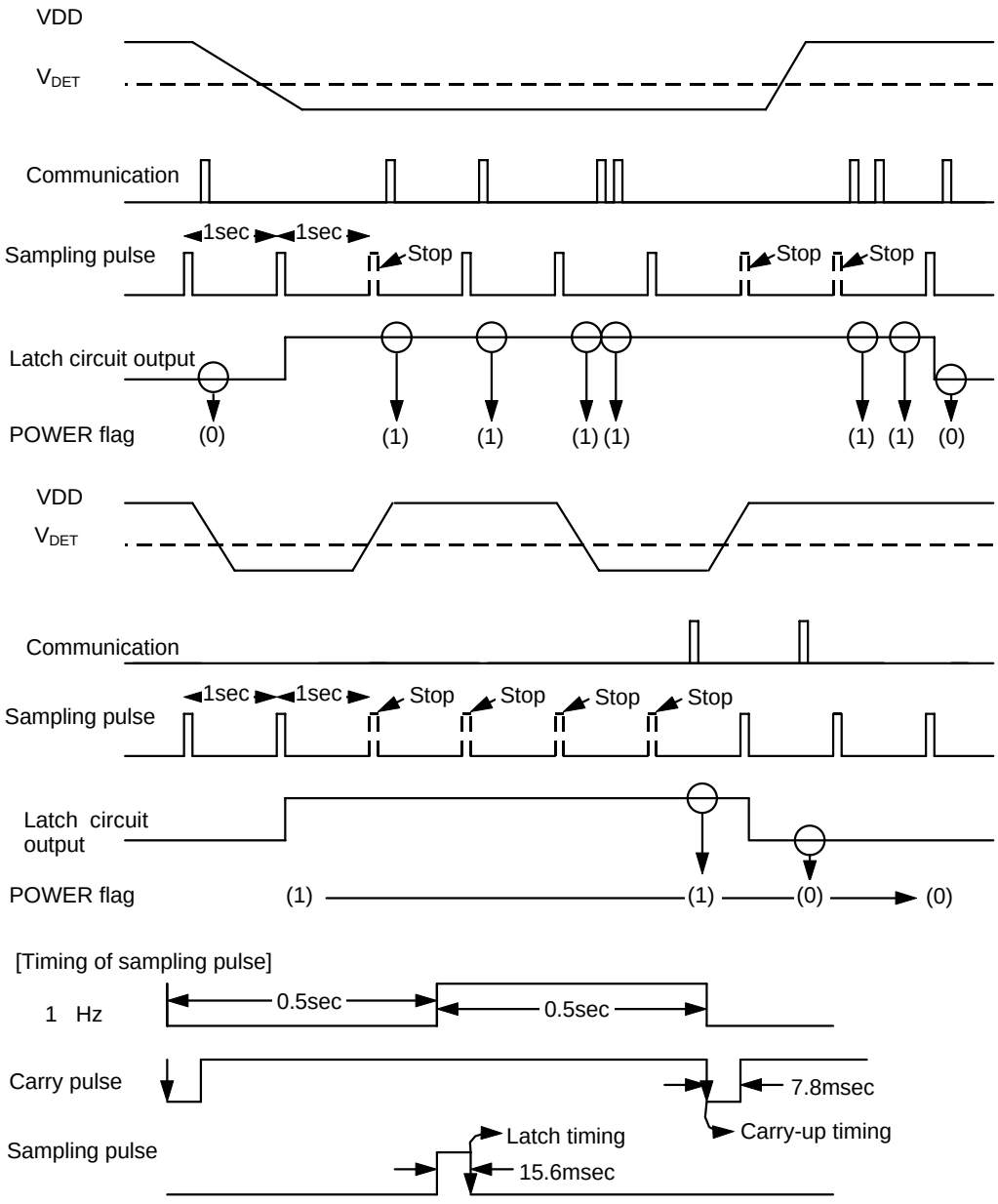
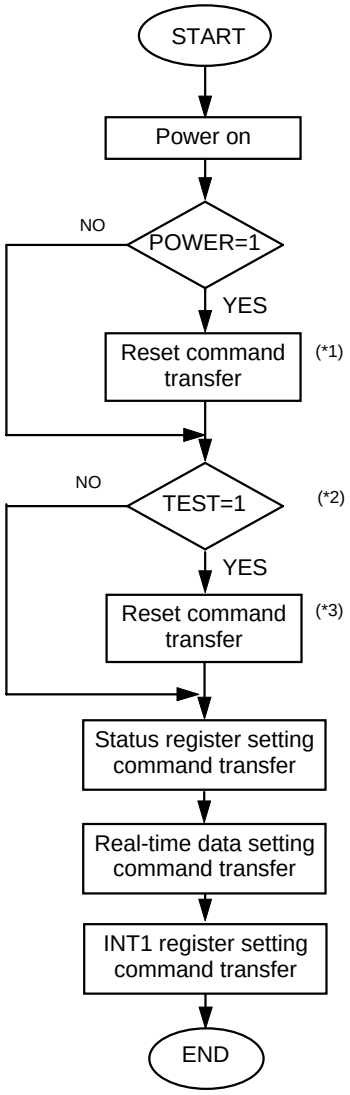


Figure 16 Timing of the power voltage detecting circuit

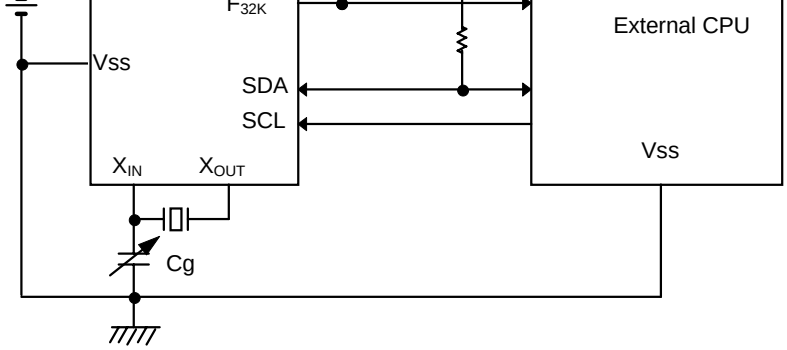


(*1) If S-3531 is back-up and power is turned on only on the CPU side, the reset command does not need transferring.

(*2) If conditions are no good (e.g., noise) and probable changes in commands occurs via serial communications, it is recommended to make sure the TEST flag.

(*3) The test ending command may be used alternately

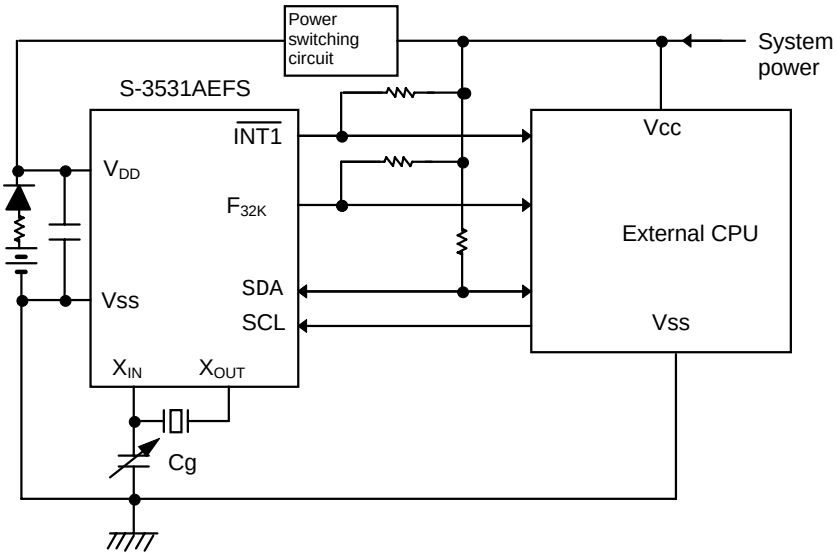
Figure 17 Initialization flow



Due to the I/O terminal with no protective diode on the VDD side, the relation of VCC≥VDD has no problem. But give great care to the standard.

Make communications after the system power is turned on and a stable state is obtained.

Figure 18 Applied circuit 1



Make communications after the system power is turned on and a stable state is obtained.

Figure 19 Applied circuit 2

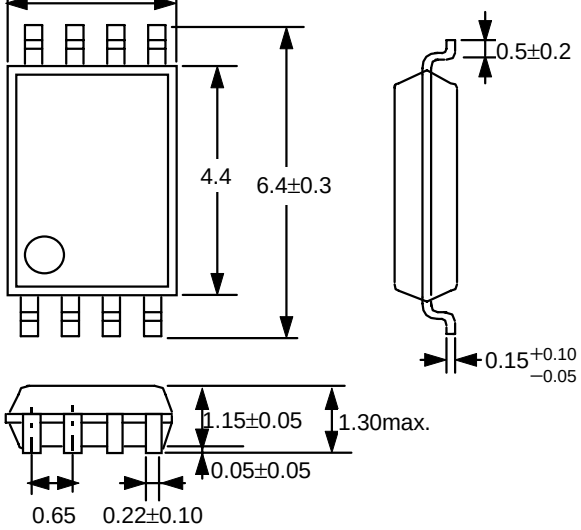


Figure 20 Dimensional outline

■ Order Specification

S-3531AE FS

Package (fixed) : Eight-pin SSOP

Description (fixed)

Since crystal oscillation is sensitive to external noises (clock accuracy is affected), the following measures must be ta
configuring the oscillating circuit:

(1) S-3531A, crystal oscillator and external capacitor (Cg) are placed as close to each other as possible.

(2) Make high the insulation resistance between terminals and the board between XIN and XOUT.

(3) Do not place any signal or power lines close to the oscillating circuit.

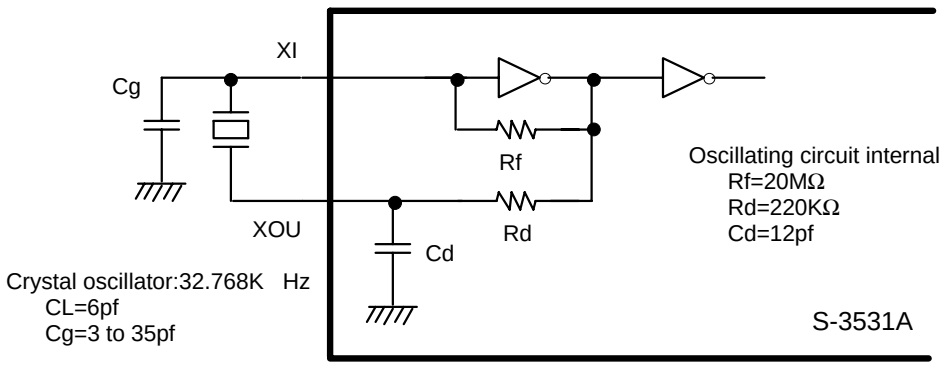
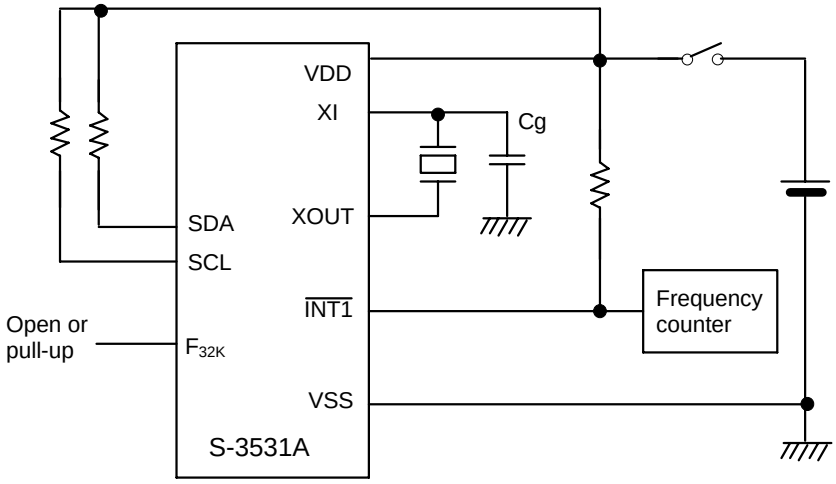


Figure 21 Connection

2.Measurement of oscillating frequencies

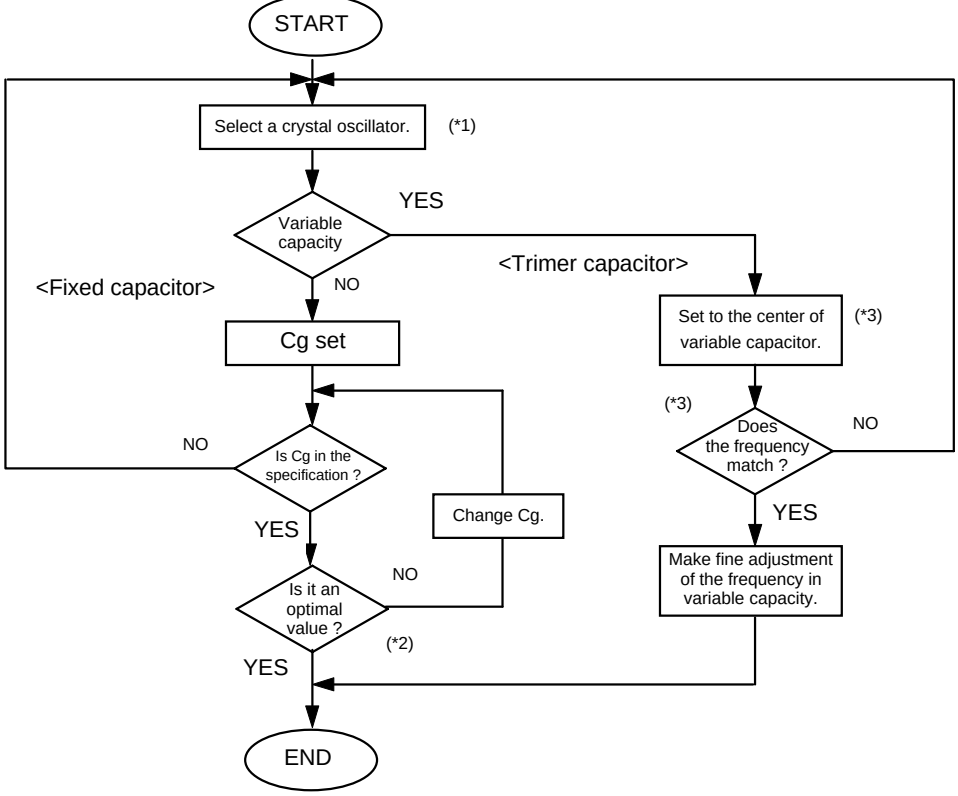
When power is turned on, S-3531A has the internal power-on detecting circuit operating and outputs a signal of 1 Hz fro
$\overline{\text{INT1}}$ terminal to select the crystal oscillator and optimize the Cg value. Turn power on and measure the signal w
frequency counter following the circuit configuration shown in Figure 22. Refer to 11 and 14 pages in this document for fu
information.

(*) If the error range is ±1ppm in relation to 1 Hz, time is shifted by approximately 2.6 seconds a month:
10^{-6} (1ppm) ×60 seconds ×60 minutes ×24 hours × 30 days = 2.592 seconds



Note 1: Use a high-accuracy frequency counter (1ppm order).
Note 2: Since the 1 Hz signal continues to be output, yo must send the reset comm in normal operation.
Note 3: Determine Cg with its frequency slow/fast range property referred.

Figure 22 Connection diagram



(*1) For making matching adjustment of the IC with a crystal, contact an appropriate crystal maker to determine the CL value (load capacity) and RI value (equivalent serial capacity). The CL value = 6 pf and RI value = 30 kΩ TYP. are recommended values.

(*2) Cg value selection must be performed on the actual PCB since suspended capacity affects it. Select the Cg value in a range from 3 pf to 35 pf. If the frequency does not match, change the CL value of the crystal.

(*3) Adjust the rotation angle of the variable capacity so that the capacity value is somewhat smaller than the center, and confirm the oscillating frequency and the center value of the variable capacity. This is done in order to make the capacity of the center value smaller than one half of the actual capacity value because a smaller capacity value makes a greater quantity of changes in a frequency. If the frequency does not match, change the CL value of the crystal.

Note 1 : Oscillating frequencies are changed by ambient temperature and power voltage. Refer to property samples.

Note 2 : The 32 kHz crystal oscillator operates slower at higher or lower ambient temperature than 20 to 25°C. Therefore, it is recommended to adjust or set the oscillator to operate somewhat faster at normal temperature.

Output voltage	V_{OUT}	-0.3 to +6.5	V	SDA,$\overline{INT1}$, F_{32K}
Operating temperature	T_{opr}	-40 to +85	°C	VDD=3.0V
Retention temperature	T_{stg}	-55 to +125	°C	—

■ Recommended Operating Conditions

Table 6 Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	VDD	—	1.7	3.0	5.5	V
Operating temperature	T_{opr}	—	-20	+25	+70	°C

■ Oscillation Characteristics

Table 7 Oscillation characteristics

(Ta=25°C, VDD=3V, DS-VT-200 (crystal oscillator, CL=6pF, 32,768HZ) manufactured by Seiko Electronic Part Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within ten seconds	1.7	—	5.5	V
Oscillation start time	T_{STA}	—	—	—	1	SEC
IC-to-IC frequency diversity	δIC	—	-10	—	+10	ppm
Frequency voltage diversity	δV	VDD=1.7 to 5.5V	-3	—	+3	ppm/V
Input capacity	Cg	Applied to the XIN terminal	3	—	35	pF
Output capacity	Cd	Applied to the XOUT terminal	—	12	—	pF

Range of operating voltage	VDD	Ta=-20 to +70°C	1.7	3.0	5.5	V	—
Drain current 1	I_{DD1}	During no communications	—	0.7	1.5	µA	—
Drain current 2	I_{DD2}	During communications (SCL=100KHZ)	—	12	20	µA	—
Input leak current 1	I_{ILL1}	V_{IN}= VDD	-0.5	—	0.5	µA	SCL,SDA
Input leak current 2	I_{ILL2}	V_{IN}= VSS	-0.5	—	0.5	µA	SCL,SDA
Output leak current1	I_{OZH}	V_{OUT}=VDD	-0.5	—	0.5	µA	$\overline{INT1}$, F_{32K} SDA
Output leak current2	I_{OZL}	V_{OUT}=VSS	-0.5	—	0.5	µA	$\overline{INT1}$,F_{32K} SDA
Input voltage 1	V_{IH}	—	0.8xVDD	—	—	V	SDA,SCL
Input voltage 2	V_{IL}	—	—	—	0.2xVDD	V	SDA,SCL
Output current 1	I_{OL1}	V_{OUT}=0.4V	1.5	2.5	—	mA	$\overline{INT1}$,F_{32K}
Output current 2	I_{OL2}	V_{OUT}=0.4V	5	10	—	mA	SDA
Power voltage detecting voltage 1	V_{DET1}	Ta=+25°C	1.8	2.0	2.2	V	—
Power voltage detecting voltage 2	V_{DET2}	Ta=-20 to+70°C	1.72	—	2.3	V	—

voltage							
Drain current 1	I_{DD1}	During no communications	—	1.6	3.0	µA	—
Drain current 2	I_{DD2}	During communications (SCL=100KHZ)	—	26	40	µA	—
Input leak current 1	I_{ILL1}	V_{IN}= VDD	-0.5	—	0.5	µA	SCL,SDA
Input leak current 2	I_{ILL2}	V_{IN}= VSS	-0.5	—	0.5	µA	SCL,SDA
Output leak current1	I_{OZH}	V_{OUT}=VDD	-0.5	—	0.5	µA	$\overline{INT1}$,F_{32K} SDA
Output leak current2	I_{OZL}	V_{OUT}=VSS	-0.5	—	0.5	µA	$\overline{INT1}$,F_{32K} SDA
Input voltage 1	V_{IH}	—	0.8xVDD	—	—	V	SDA,SCL
Input voltage 2	V_{IL}	—	—	—	0.2xVDD	V	SDA,SCL
Output current 1	I_{OL1}	V_{OUT}=0.4V	2.0	3.5	—	mA	$\overline{INT1}$,F_{32K}
Output current 2	I_{OL2}	V_{OUT}=0.4V	6	12	—	mA	SDA
Power voltage detecting voltage 1	V_{DET1}	Ta=+25°C	1.8	2.0	2.2	V	—
Power voltage detecting voltage 2	V_{DET2}	Ta=-20 to+70°C	1.72	—	2.3	V	—

Table 10 Measurement conditions

Input pulse voltage	0.1×VDD to 0.9×VDD
Input pulse rising/falling time	20ns
Output judgment voltage	0.5×VDD
Output load	100pF+pull-up resistance 1.0kΩ

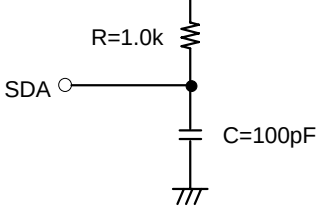


Figure Output load circuit

Table 11 AC properties

Item	Symbol	VDD=1.7V to 5.5V			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	—	100	kHz
SCL clock “L” time	t_{LOW}	4.7	—	—	µs
SCL clock “H” time	t_{HIGH}	4.0	—	—	µs
SDA output delay time	t_{PD}	—	—	3.5	µs
Start condition setup time	$t_{SU.STA}$	4.7	—	—	µs
Start condition holding time	$t_{HD.STA}$	4.0	—	—	µs
Data input setup time	$t_{SU.DAT}$	250	—	—	ns
Data input holding time	$t_{HD.DAT}$	150	—	—	ns
Stop condition setup time	$t_{SU.STO}$	4.7	—	—	µs
SCL-SDA rising time	t_R	—	—	1.0	µs
SCL-SDA falling time	t_F	—	—	0.3	µs
Bus release time	t_{BUF}	4.7	—	—	µs
Noise suppression time	t_I	—	—	100	ns

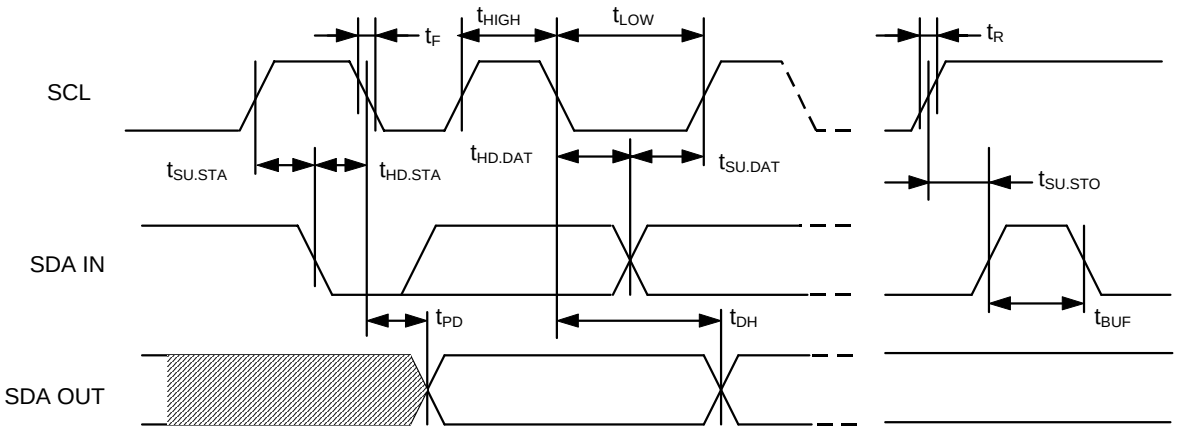
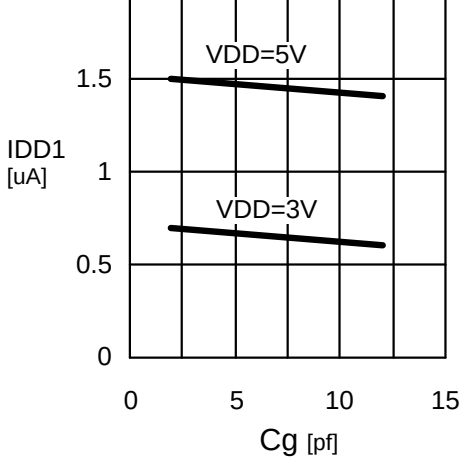
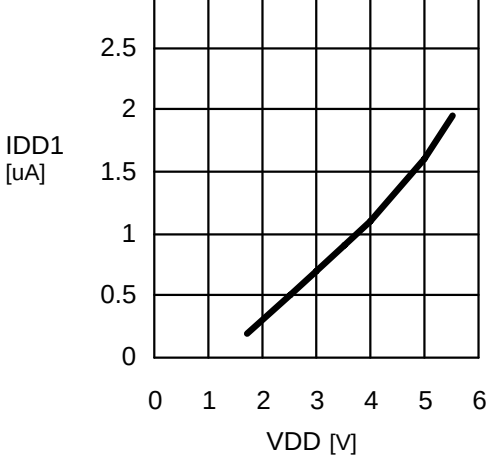
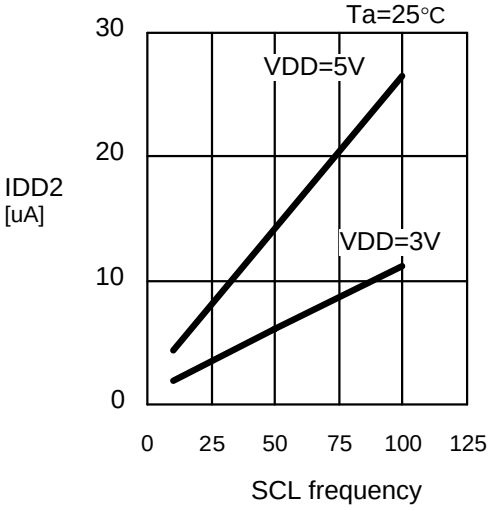


Figure 22 Bus timing

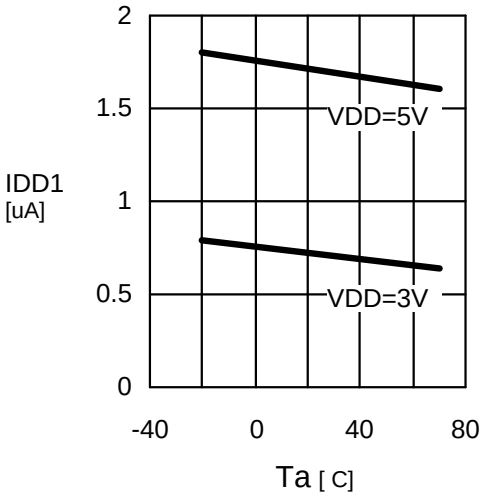




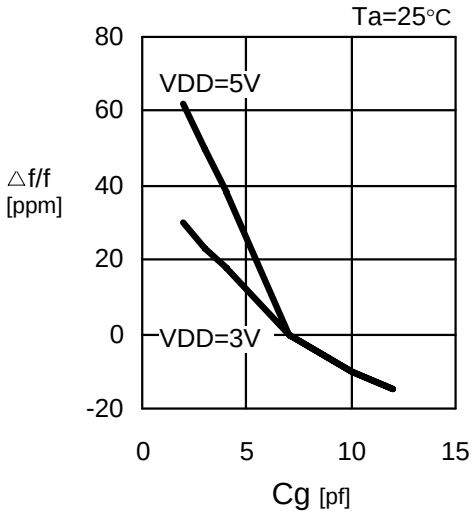
(3) Operating drain current versus Input clock



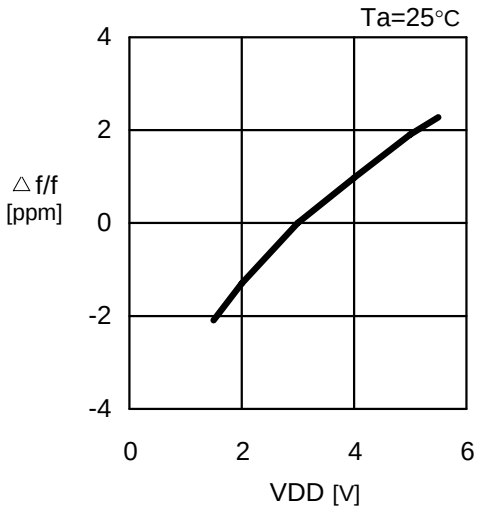
(4) Standby current versus temperature

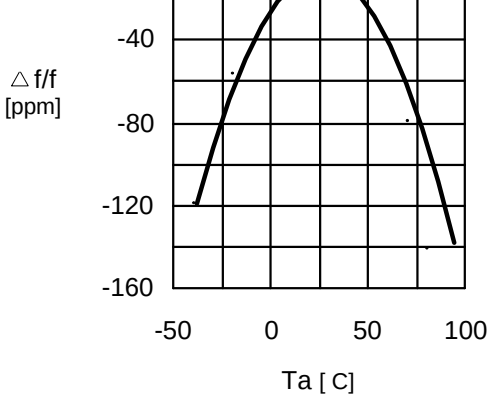


(5) Oscillating frequency versus Cg

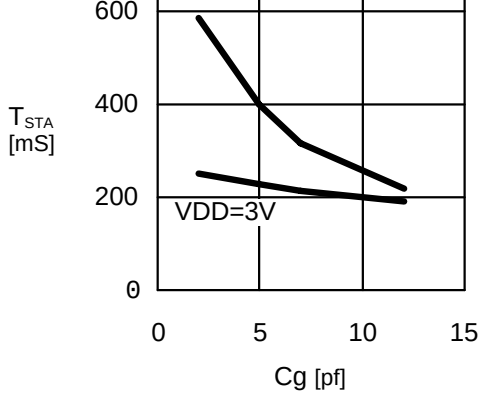


(6) Oscillating frequency versus VDD

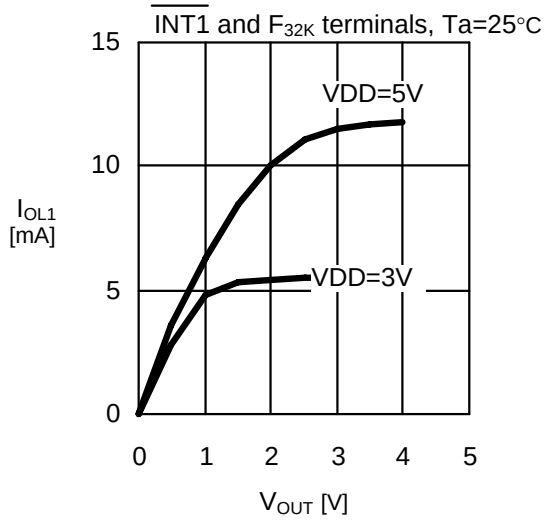


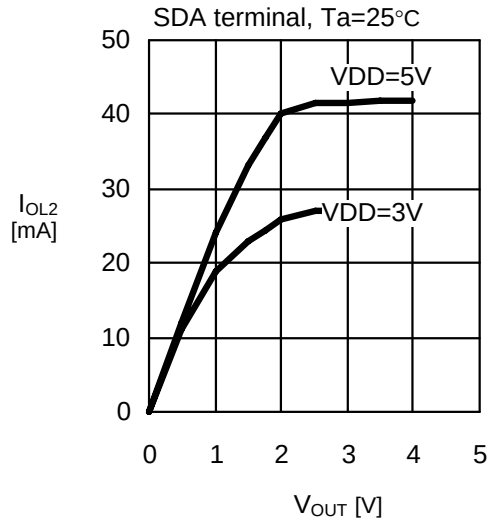


(9) Output current 1 (V_{OUT} versus I_{OL1})



(10) Output current 2 (V_{OUT} versus I_{OL2})





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Collection of Product FAQs

Author: Shirai Masaaki Date: 99/04/16 (Friday) 18:20 (modified: 99/04/16(Friday))

<Information level>

A: Public (Printing O.K.)

Index: B: General

<Product>

Division name: 01 IC

Category 1: 17 ASSP

Category 2: 2. Real-Time Clock

Product name: Overall

Related documents:

Question:

What are the notes for time settings (S3511/S3530/S3531)?

Answer:

If time data is rewritten in a product with an alarm interrupt (S-3511/S-3530/S-3531), be sure to disable the alarm interrupt before the time is set.

Reason: When data is written using real-time data access 2, registers for hours, minutes, and seconds are reset (all “0”’s), and arbitrary hours, minutes, and seconds are then set. If the alarm is set for 0:00 a.m. and the alarm interrupt is enabled, when the time data is rewritten the registers are reset (all “0”’s) to 0:00 a.m., the set alarm time, thereby causing an interrupt (INT).

<Remarks>

FAQ No.: 17S35004

Collection of Product FAQs

Author: Shirai Masaaki Date: 99/04/14 (Wednesday) 11:34 (modified: 99/05/18)

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 17 ASSP

Category 2: 2. Real-Time Clock

Cal No.: Overall

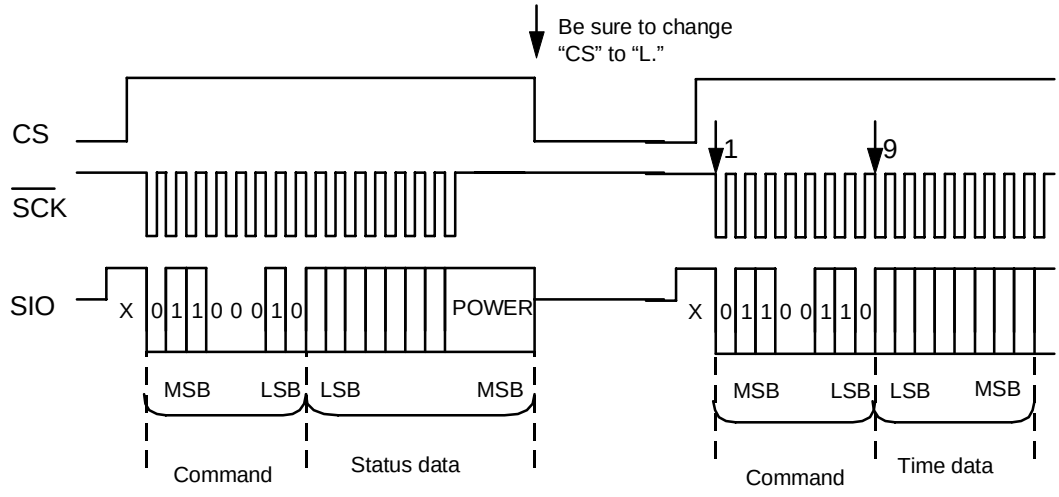
Related documents:

Question:

What about the write/read errors (notes)?

Answer:

To continuously write or read data in a 3-wire RTC (S-3511/S-3513/S-35L12/S-3510), be sure to change “CS” to “L” after the first command has been executed and before the next command is executed. If commands are continuously executed without changing “CS” to “L,” the second command is disregarded.



<Remarks>

FAQ No.: 17S35003

Collection of Product FAQs

Author: Shirai Masaaki Date: 99/04/13 (Tuesday) 15:40 (modified: 99/05/18)

<Information level>

A: Public (Printing O.K.)

Index: A: General

<Product>

Division name: 01 IC

Category 1: 17 ASSP

Category 2: 2. Real-Time Clock

Cal No.: Overall

Related documents:

Question:

What about the Y2K problem?

Answer:

Our Real-Time Clock outputs information consisting of the last two digits of the year. The S-35L12/L32 can use the register bits in its RTC to determine whether the year is 1900 or 2000 when the last two digits change from 99 to 00. Most other RTCs, however, cannot determine whether the year is 1900 or 2000 when the last two digits change from 99 to 00. Thus, when this microcomputer is used, the user must load year information for the RTC in a microcomputer to determine whether the year is 1900 or 2000. Accordingly, when the year reaches 2000, our RTC allows year information to operate normally and be output as “00,” thereby preventing malfunctions.

There is no problem with the operation of the IC. If, however, peripheral circuits and software developed by a client manage year information using the last two digits of the year, they may malfunction. Thus, such devices should be checked.

<reference>

http://www.sii.co.jp/sii2000.htm

<Remarks>

FAQ No.: 17S35002

Collection of Product FAQs

Author: Shirai Masaaki Date: 99/04/13 (Tuesday) 14:26 (modified: 99/04/13)

<Information level>

A: Public (Printing O.K.)

Index: A: General

<Product>

Division name: 01 IC

Category 1: 17 ASSP

Category 2: 2. Real-Time Clock

Cal No.: Overall

Related documents:

Question:

Why is an auto calendar available through the year 2099?

Answer:

The SII's RTC denotes the year using its last two digits. These digits are then divided by four, and if they are divisible the year is determined to be a leap year (the auto calendar determines both 1996 and 2000 to be leap years). The actual calendar, however, does not treat a year with "00" as its last two digits as a leap year (except for the year 2000; see the following). Accordingly, although 2100 is not a leap year, the RTC treats it as one. Therefore, this auto calendar is available through 2099.

(Note) A year is defined as a leap year when its last two digits are "00" and its first two digits are divisible by four.

<Remarks>

FAQ No.: 17S35001