S3155

SONET/SDH/ATM OC-48 Transceiver With CDR

Product Brief

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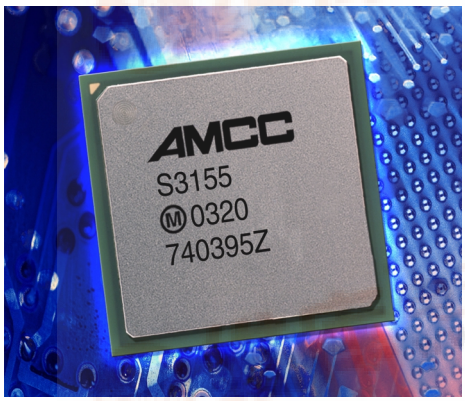

Description

The S3155 SONET/SDH transceiver chip is a fully integrated serialization/ deserialization SONET OC-48 (2.488 - 2.67 Gbps) interface device. The S3155 receives an OC-48 scrambled Non-Return to Zero (NRZ) signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based WDM applications. The figure below shows a typical network application.

On-chip clock synthesis is performed by the high-frequency Phase-Locked Loop (PLL) on the S3155 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 or 166.63 MHz reference clock in support of existing system clocking schemes.

The low jitter LVPECL interface is compliant with the bit-error rate requirements of the Telecodia and ITU-T standards. The S3155 is packaged in a 196 PBGA, offering designers a small package outline.

Overview

The S3155 transceiver implements SONET/SDH serialization/deserialization, and transmission functions. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The S3155 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. 16-bit parallel output

– At a Glance –

Features

- 650 mW typical power
- Integrated clock data recovery
- On-chip high-frequency PLL for clock generation and clock recovery
- Supports OC-48 (2.488 Gbps) with FEC
- Reference frequency of 155.52 to 166.63 MHz
- RX and TX reference selectable
- Interface to LVCMOS/LVTTL logic
- Internal input termination option built-in
- 16-bit differential LVPECL/ LVDS data path or single-ended LVPECL option
- 196 PBGA package
- Diagnostic and line loopback mode
- Support serial loop timing mode
- Lock detect
- Signal detect input with polarity select
- Low Jitter LVPECL/LVDS interface
- Internal FIFO to decouple transmit clocks

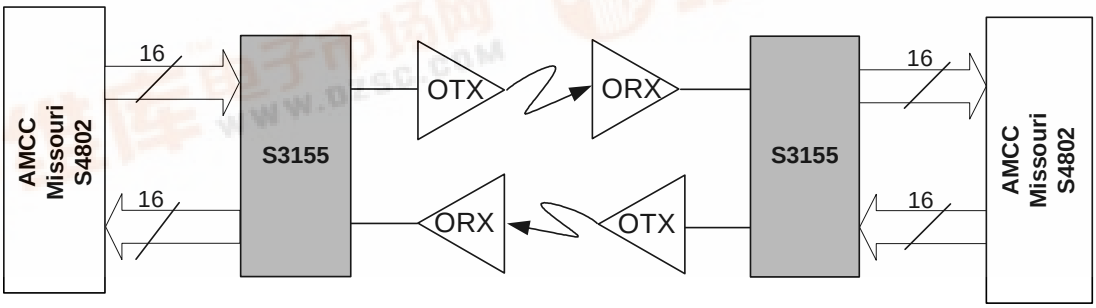

Figure 1. System Block Diagram

AMCC Suggested Interface Device

AMCC S4801 Amazon	STS-48c POS/ATM SONET Mapper
AMCC S4802 Missouri	SONET/SDH STS-48/STM-16 Framer/ Pointer Processor
AMCC S4804 Rhine	STS-48 SONET/SDH Framer and POS/ATM Mapper
AMCC S4805 Danube	SONET/SDH STS-48/STM-16 Framer/ Pointer Processor
AMCC S19201 Indus	STS-192 SONET/SDH Interleaver/ Disinterleaver

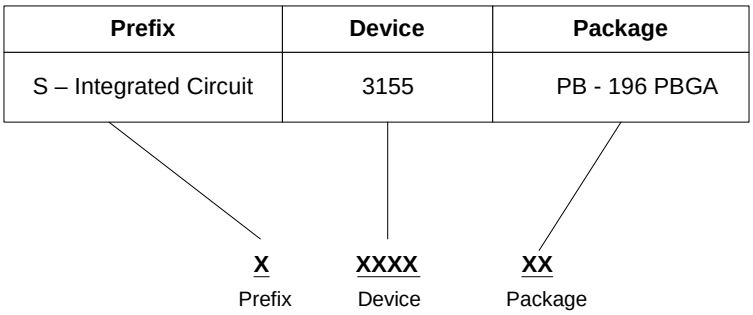

Figure 2. S3155 Ordering Information

- Dual 1.2 V and 3.3 V/2.5 V supply
- Complies with Telcordia and ITU-T specifications
- Built-in self test

Applications

- Wavelength Division Multiplexing (WDM) equipment
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment