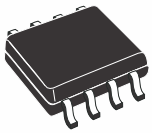
STS17NF3LL

N-channel 30V - 0.0045Ω - 17A - SO-8
STripFET™ II Power MOSFET for DC-DC conversion

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS17NF3LL	30V	<0.0055Ω	17A

- Optimal $R_{DS(on)}$ x Q_g trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced

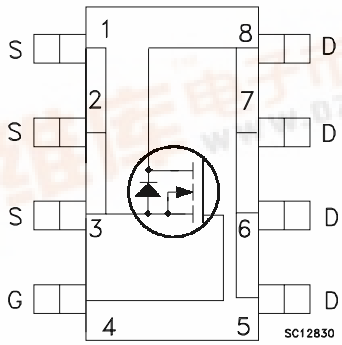


SO-8

Description

This application specific Power MOSFET is the second generation of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. Such features make it the best choice in high efficiency DC-DC converters for Telecom and computer industries.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STS17NF3LL	S17NF3LL	SO-8	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	±18	V
I_D	Drain current (continuous) at T_C = 25°C	17	A
I_D	Drain current (continuous) at T_C = 100°C	12	A
I_{DM} (1)	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at T_C = 25°C	3.2	W

1. Pulse width limited by safe operating area

Table 2. Thermal data

Rthj-amb	Thermal resistance junction-ambient max (1)	47	°C/W
Rthj-lead	Thermal resistance junction-leads max	16	°C/W
T_j	Maximum operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature	-55 to175	°C

1. When mounted on FR-4 board of 1in², 2oz Cu. t<10sec

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = max rating V_{DS} =max rating, T_C = 125°C				1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 18V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 8.5A V_{GS} = 4.5V, I_D = 8.5A		0.0045 0.0055	0.0055 0.007	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10V, I_D = 8.5A		37		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		2160 614 98		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 15V, I_D = 8.5A R_G = 4.7Ω V_{GS} = 4.5V (see *Figure 13*)		23.5 39 47.5 37		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 24V, I_D = 12.5A, V_{GS} = 4.5V, R_G = 4.7Ω (see *Figure 14*)		26 7 12	35	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				17 68	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 17A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17A, di/dt = 100A/µs, V_{DD} = 15V; T_j = 150°C (see *Figure 15*)		39 45 2.3		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

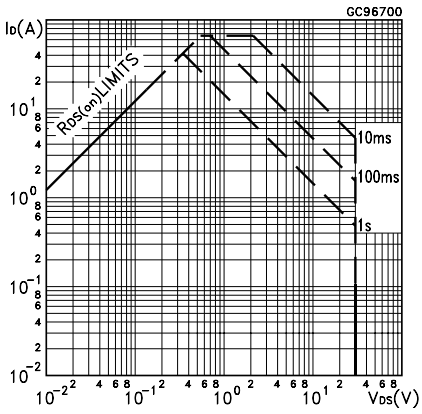


Figure 2. Thermal impedance

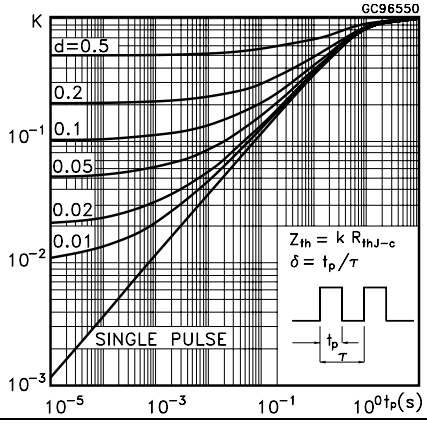


Figure 3. Output characterisics

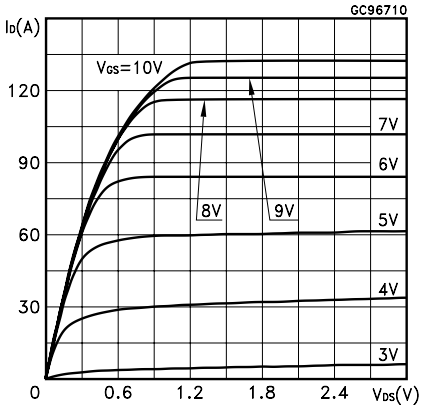


Figure 4. Transfer characteristics

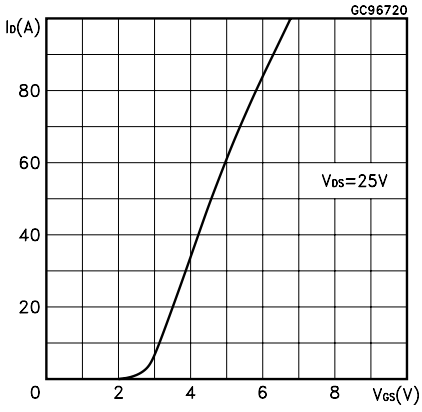


Figure 5. Transconductance

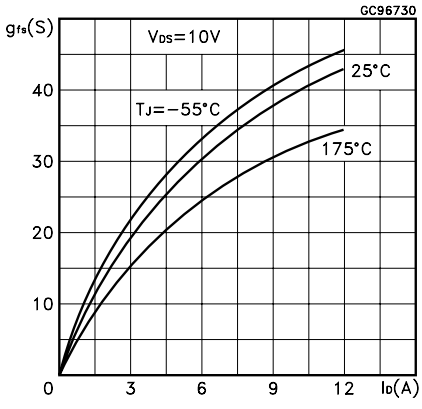


Figure 6. Static drain-source on resistance

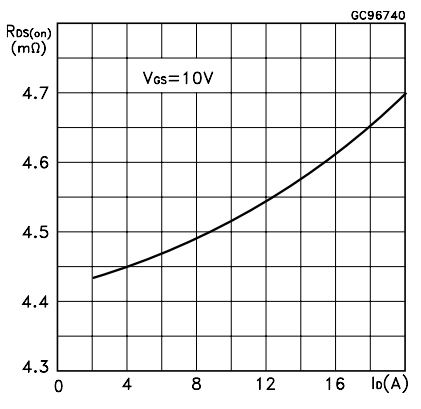


Figure 7. Gate charge vs gate-source voltage

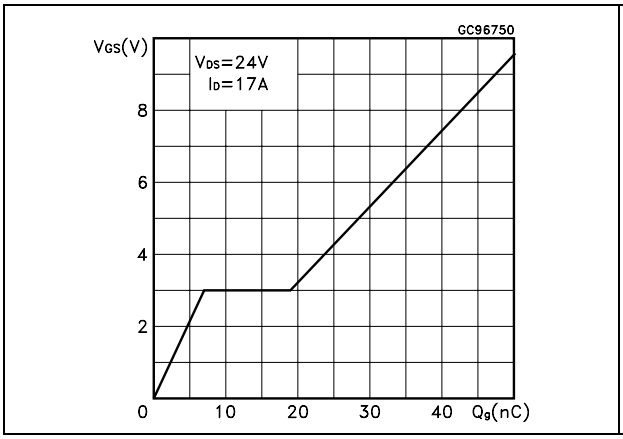


Figure 8. Capacitance variations

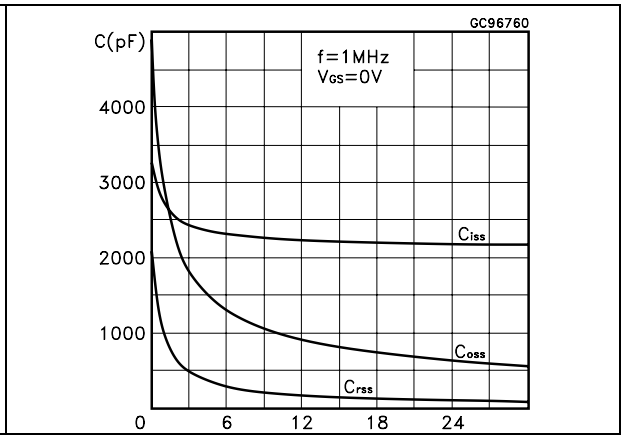


Figure 9. Normalized gate threshold voltage vs temperature

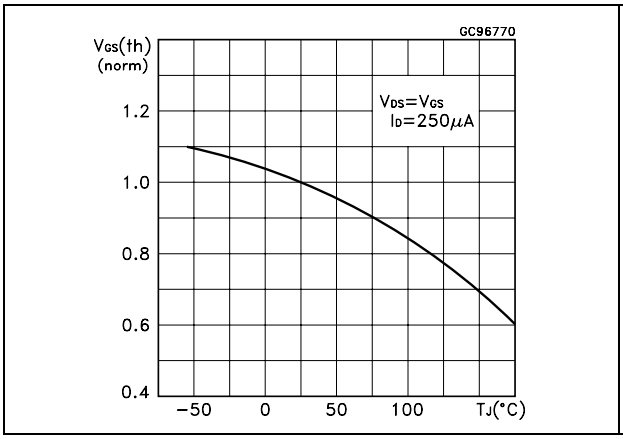


Figure 10. Normalized on resistance vs temperature

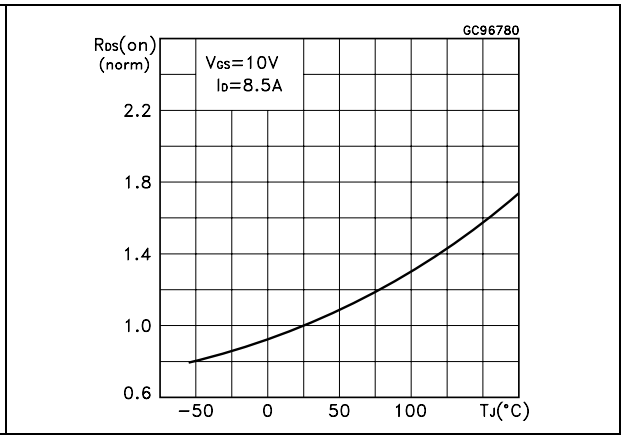


Figure 11. Source-drain diode forward characteristics

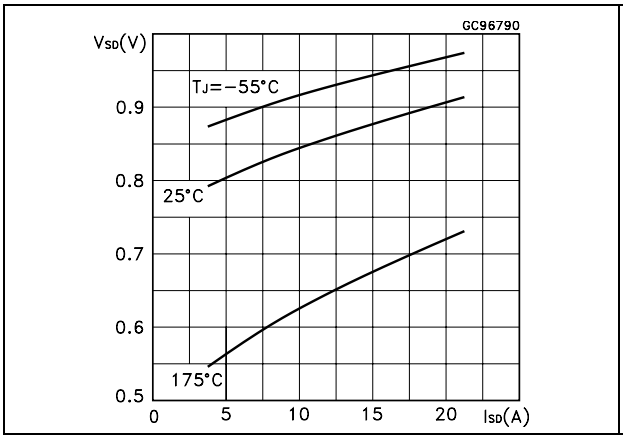
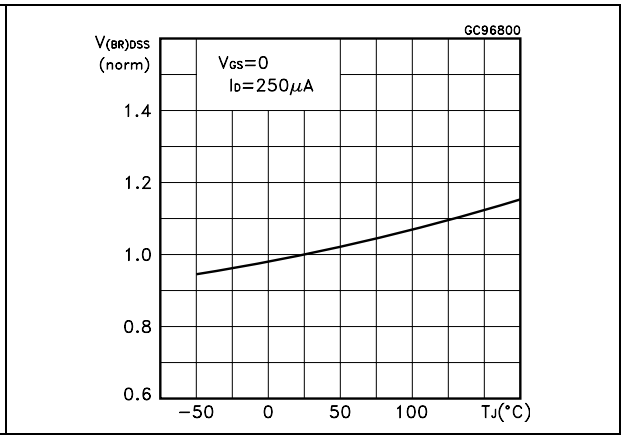


Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

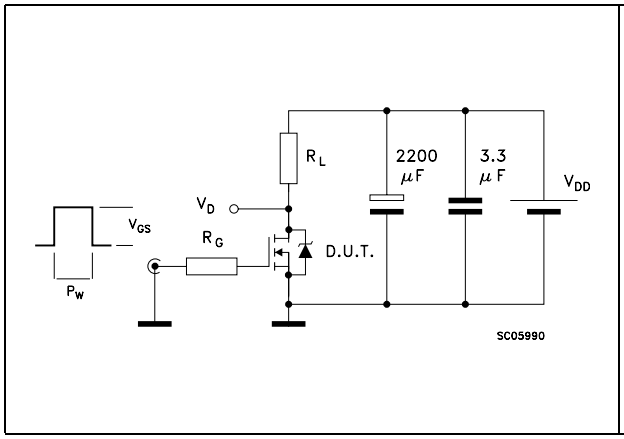


Figure 14. Gate charge test circuit

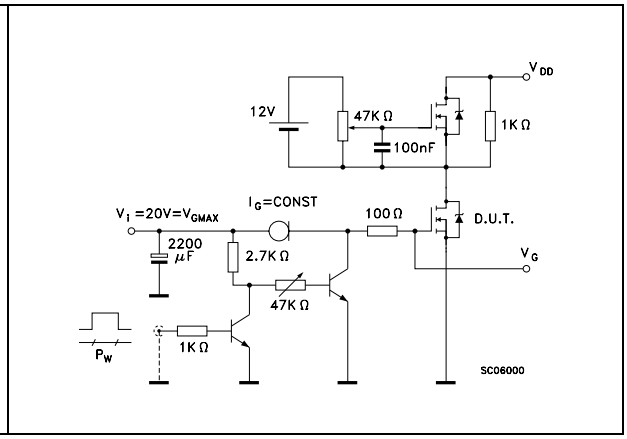


Figure 15. Test circuit for inductive load switching and diode recovery times

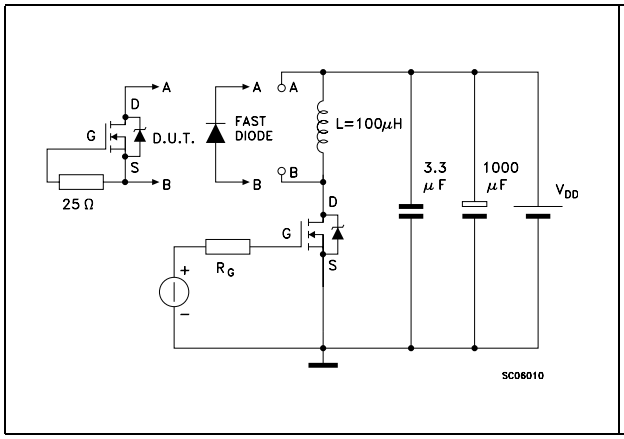


Figure 16. Unclamped Inductive load test circuit

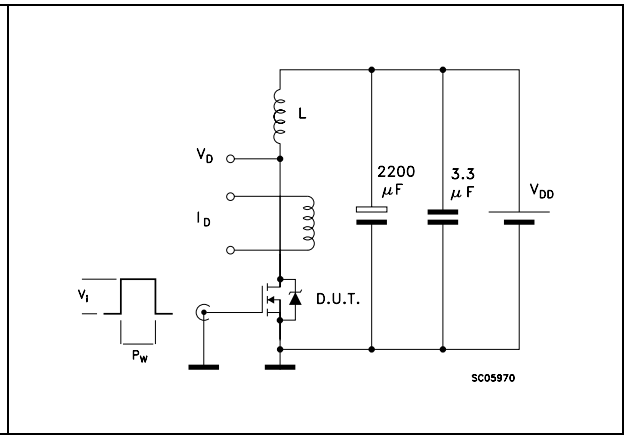


Figure 17. Unclamped inductive waveform

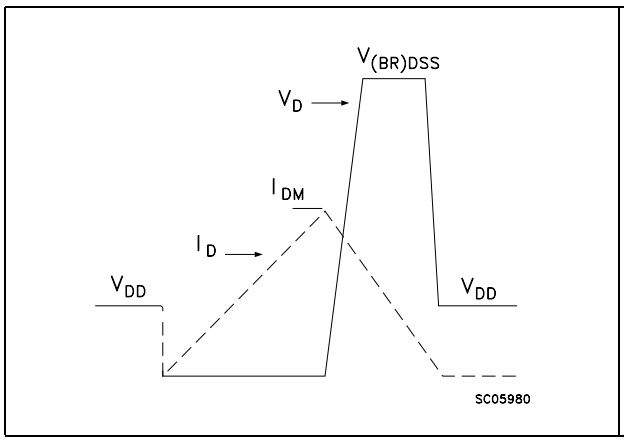
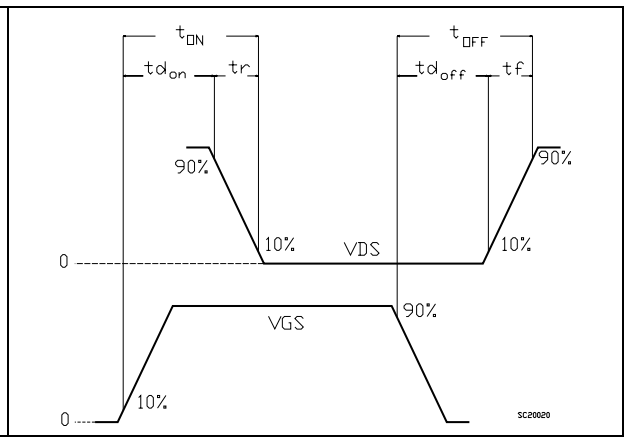


Figure 18. Switching time waveform

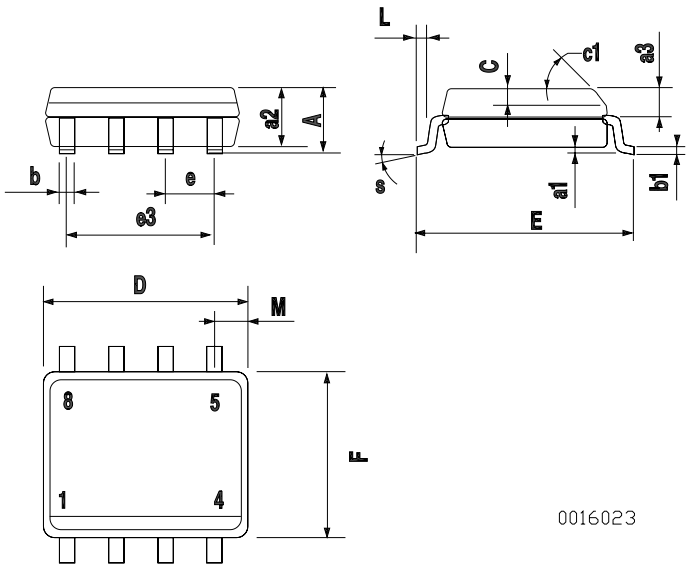


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2004	4	Complete document
04-Oct-2006	5	New template, no content change

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