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# RV4140A

## Low Power Two-Wire Ground Fault Interrupter Controller

### Features

- Powered from the AC line
- Built-in bridge rectifier
- Direct interface to SCR
- 350 µA quiescent current
- Adjustable trip current
- Adjustable time delay
- Minimum external components
- Meets UL 943 requirements
- Specifically for two-wire systems
- For use with 110V or 220V systems

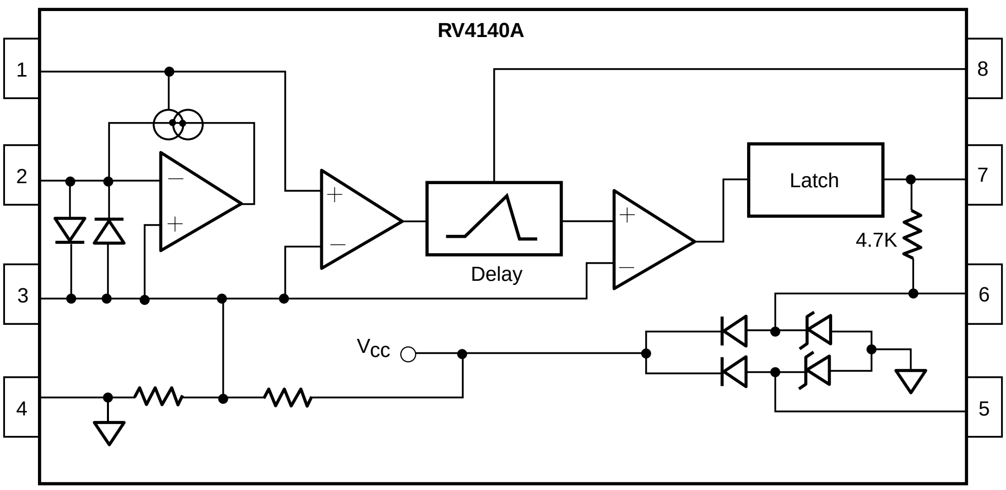
### Description

The RV4140A is a low power controller for AC outlet appliance leakage circuit interrupters. These devices detect hazardous current paths to ground such as an appliance falling into water. The interrupter then open circuits the line before a harmful or lethal shock occurs.

Internally, the RV4140A has a diode bridge rectifier, zener shunt regulator, op amp, current reference, time delay circuit, latch and SCR driver.

An external sense transformer, SCR, relay, two resistors and three capacitors complete the design of the circuit interrupter. The simple layout and minimum component count ensure ease of application and long term reliability.

### Block Diagram




65-4140A-01

## Functional Description

(Refer to Block Diagram and Figure 1 )

The shunt regulator generated by a 6.5V zener diode is built into the internal bridge rectifier. It is divided to create an internal reference voltage of 2.9V connected to pin 3. The secondary of the sense transformer is AC coupled to the inverting input of the sense amplifier at pin 2; the non-inverting input is referenced to pin 3. A current feedback loop around the sense amplifier ensures a virtual ground will be presented to the secondary of the sense transformer. In this manner it acts as a current transformer instead of a voltage transformer. In this mode, the transformer's characteristics are very predictable and circuit adjustments are not necessary in production.

The sense transformer has a toroidal core made of laminated steel rings or solid ferrite material. The secondary of the transformer is 500 to 1000 turns of #40 wire wound through the toroid. The primary's one turn made by passing the AC hot and neutral wires through the center of the toroid. When a ground fault exists, a difference exists between the current flowing in hot and neutral wires. The difference primary current, divided by the number of secondary turns, flows through the secondary wire of the transformer.

The AC coupled transformer secondary current then flows through the sense amplifier's feedback loop, creating a full wave rectified version of the secondary fault current. This current passes through $R_{SET}$ at pin 1, generating a voltage equal to $R_{SET}$ times the peak fault current divided by the sense transformer turns ratio. This voltage is compared with the reference voltage at pin 3.

If the voltage at pin 1 is greater than pin 3, a comparator will charge C2 through a 29 μA current source at pin 8. If the voltage at pin 1 exceeds pin 3 for longer than the delay time, a 400 μA current will pulse between pins 7 and 6 which will trigger the gate of the SCR.

If the voltage at pin 1 exceeds pin 3 for less than the delay time, the SCR will not trigger.

The fault current at which the controller triggers the SCR is dependent on the value of $R_{SET}$ and the time delay determined by C2.

UL 943 requires the circuit interrupter trip when the ground fault exceeds 6 mA and not trip when the fault current is less than 4 mA.

### Supply Current Requirements

The RV4140A has a built-in diode bridge rectifier that provides power to the chip independent of the polarity of the AC line. This eliminates the external rectifier required for previous GFCI controllers.

$R_{LINE}$ limits the shunt regulator current to 2 mA. The recommended value is 47K to 91K for 110V systems and 91K to 150K for 220V systems. The recommended maximum peak line current through $R_{LINE}$ is 7 mA.

**DO NOT** connect a filter capacitor between pins 5 and 6 in an attempt to filter the supply voltage at the RV4140A. Proper operaton of the RV4140A requires the internal supply voltage to be unfiltered.

### SCR Driver

The SCR must have a high dV/dt rating to ensure that line noise (generated by electrically noisy appliances) does not falsely trigger the SCR. Also, the SCR must have a gate drive requirement less than 200 μA. C3 is a noise filter that prevents high frequency line pulses from triggering the SCR.

The relay solenoid used should have a 3 ms or less response time to meet the UL 943 timing requirement.

### Supplier of Sense Transformers and Cores

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842, supplies a full line of ring cores and transformers designed specifically for GFCI and related applications.

### Determining the Values of RSET and C2

Determine the ground fault trip current requirement. This will be typically 5 mA in North America (117 VAC) and 10 mA in the UK and Europe.

Determine the minimum amount of time delay required to prevent nuisance tripping. This will typically be 1 to 2 ms.

The value of C2 required to provide the desired delay time is:

$$C2 = 10 \times T$$

where C2 is in nF, and T is the desired delay time in ms.

The value of $R_{SET}$ to meet nominal ground fault tip current specification is:

$$R_{SET} = \frac{2.05 \times N}{I_{FAULT} \times \mathrm{COS}\ 180(T/P)}$$

Where:

- $R_{SET}$ is in kΩ
- T is the time delay in ms
- P is the period of the line frequency in ms
- $I_{FAULT}$ is the desired ground fault trip current in mA RMS.
- N is the number of sense transformer secondary turns.

This formula assumes an ideal sense transformer is used. The calculated value of $R_{SET}$ may have to be changed up to 30% when using a non-ideal transformer.

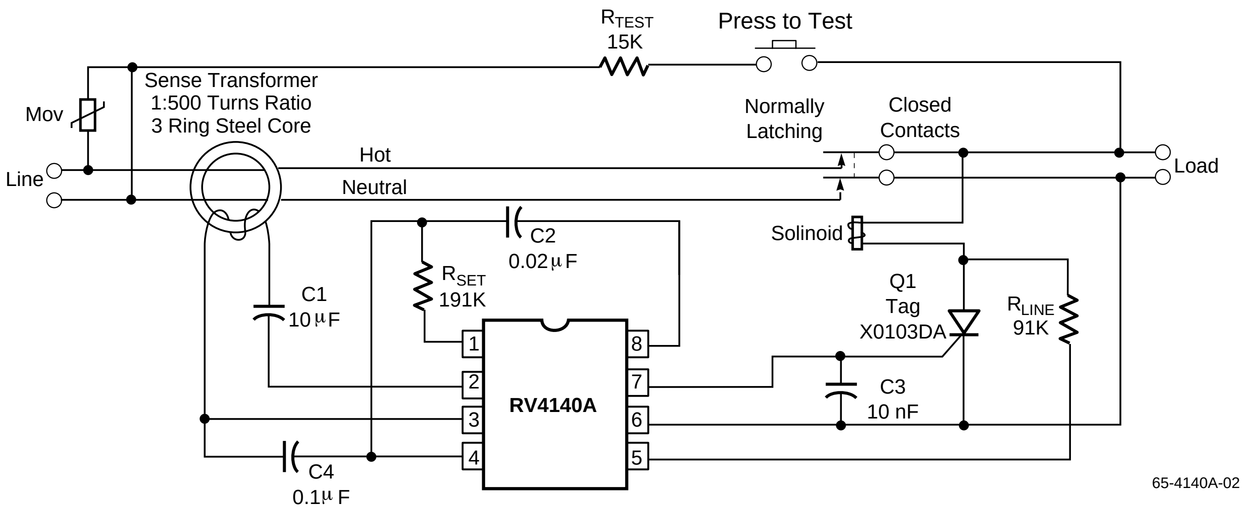
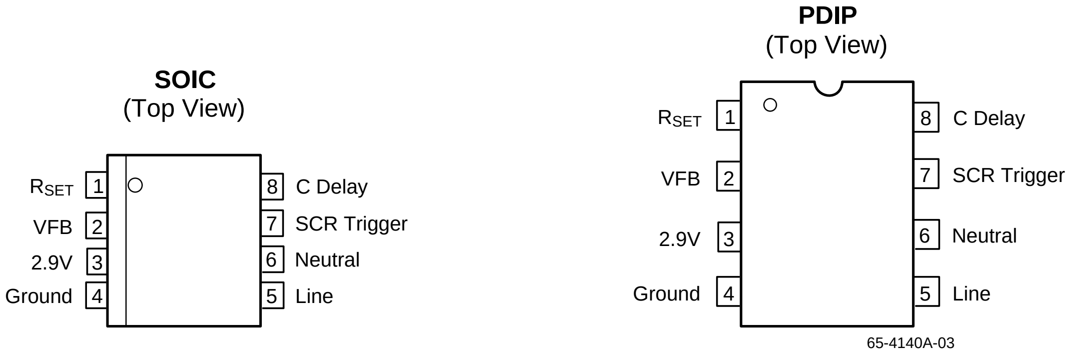



**Figure 1. Appliance Leakage Detector Circuit Application**

## Pin Assignments




## Absolute Maximum Ratings

| Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Supply Current | | | | 7 | mA |
| Internal Power Dissipation | | | | 500 | mW |
| Storage Temperature Range | | -65 | | +150 | °C |
| Operating Temperature Range | | -35 | | +80 | °C |
| Lead Soldering Temperature | 60 Seconds, DIP | | | +300 | °C |
| | 10 Seconds, SOIC | | | +260 | °C |

## Thermal Characteristics

| Parameter | 8 Lead Plastic SOIC | 8 Lead Plastic DIP |
|---|---|---|
| Maximum Junction Temperature | +125°C | +125°C |
| Maximum $P_D T_A$<50°C | 300 mW | 468 mW |
| Thermal Resistance, $\theta_{JA}$ | 240°C/W | 160°C/W |
| For $T_A$ > 50°C Derate at | 4.1 mW/°C | 6.25 mW/°C |

## Electrical Characteristics

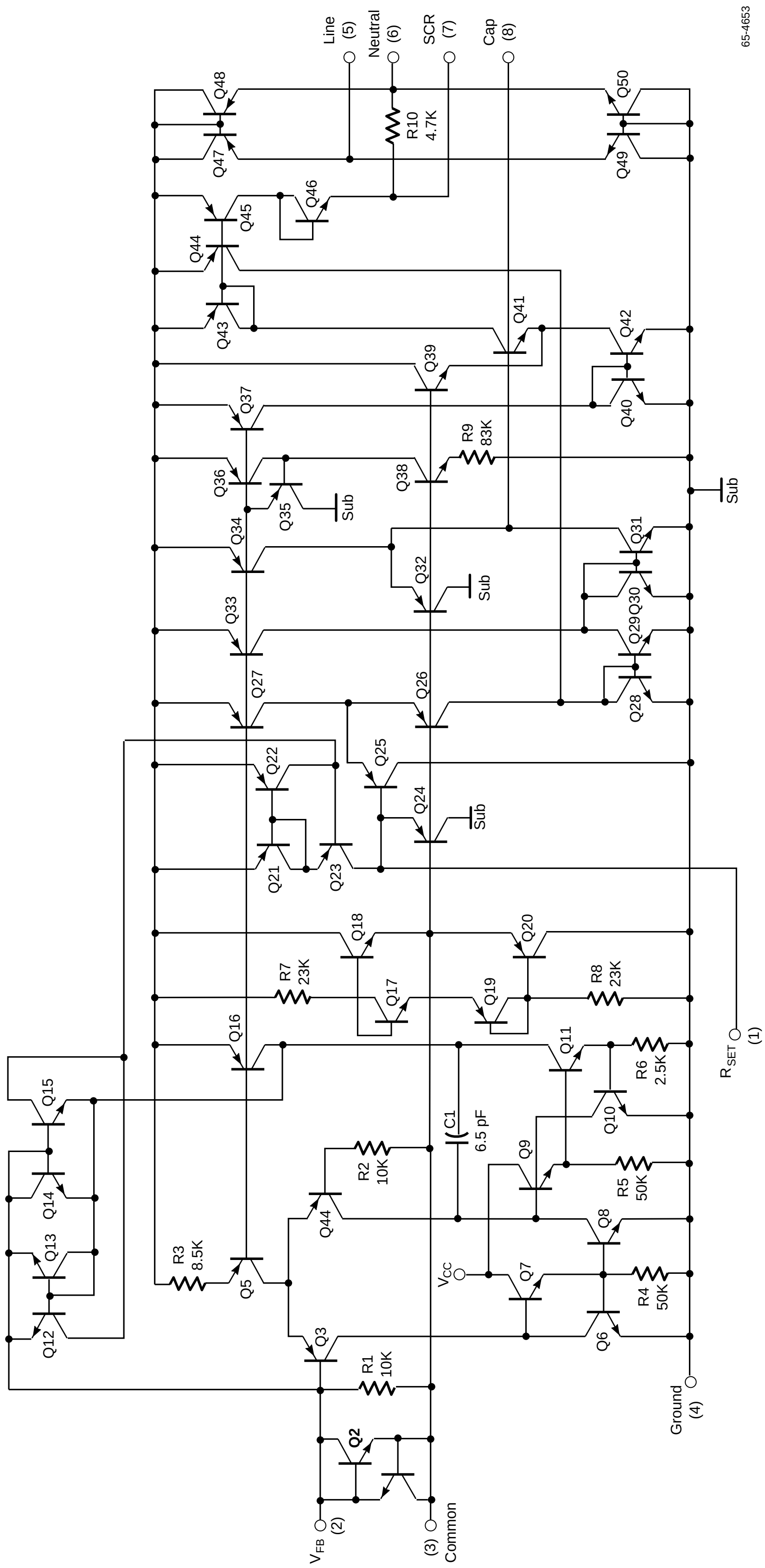
$I_{LINE}$ = 1.2mA and $T_A$ = +25°C, $R_{SET}$ = 290kΩ

| Parameters | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Shunt Regulator (Pins 5 to 4)** | | | | | |
| Regulated Voltage | $I_{2-3}$ = 11µA | 6.8 | 7.2 | 7.6 | V |
| Regulated Voltage | $I_{LINE}$ = 700 µA, $I_{2-3}$ = 9µA | 6.8 | 7.2 | 7.6 | V |
| **Sense Amplifier (Pins 2 to 3)** | | | | | |
| Offset Voltage | Design Value | -3.0 | 0 | 3.0 | mV |
| Gain Bandwidth | Design Value | | 2.0 | | MHz |
| Input Bias Current | Design Value | | 30 | 100 | nA |
| **SCR Trigger (Pins 7 to 6)** | | | | | |
| Output Resistance | $V_{5-6}$ = open, $I_{2-3}$ = 0µA | 4.0 | 4.7 | 5.4 | kΩ |
| Output Voltage | $I_{2-3}$ = 9µA | 0 | 0.1 | 10 | mV |
| Output Voltage | $I_{2-3}$ = 11µA | 1.4 | 2.0 | 2.6 | V |
| Output Current | $V_{7-6}$ = 0V, $I_{2-3}$ = 11µA | 300 | 420 | 600 | µA |
| **Reference Voltage (Pins 3 to 4)** | | | | | |
| Reference Voltage | $I_{LINE}$ = 700 µA | 2.6 | 2.9 | 3.2 | V |
| **Delay Timer (Pins 8 to 4)** | | | | | |
| Delay Time[1] | $C_{8-4}$ = 20nF | — | 2.0 | — | ms |
| Delay Current | $I_{2-3}$ = 11µA | 23 | 29 | 35 | µA |

**Note:**

1. Delay time is defined as starting when the instantaneous sense current ($I_{2-3}$) exceeds 2.9V/$R_{SET}$ and ending when the SCR trigger voltage $V_{7-6}$ goes high.

# Schematic Diagram



## Notes:

## Notes:

## Notes:

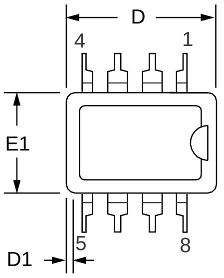
# Mechanical Dimensions

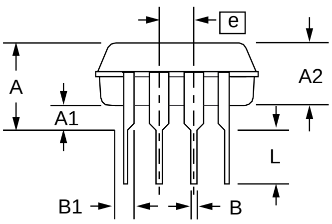
## 8-Lead Plastic DIP Package

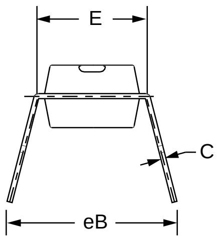
| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | — | .210 | — | 5.33 | |
| A1 | .015 | — | .38 | — | |
| A2 | .115 | .195 | 2.93 | 4.95 | |
| B | .014 | .022 | .36 | .56 | |
| B1 | .045 | .070 | 1.14 | 1.78 | |
| C | .008 | .015 | .20 | .38 | 4 |
| D | .348 | .430 | 8.84 | 10.92 | 2 |
| D1 | .005 | — | .13 | — | |
| E | .300 | .325 | 7.62 | 8.26 | |
| E1 | .240 | .280 | 6.10 | 7.11 | 2 |
| e | .100 BSC | | 2.54 BSC | | |
| eB | — | .430 | — | 10.92 | |
| L | .115 | .160 | 2.92 | 4.06 | |
| N | 8° | | 8° | | 5 |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



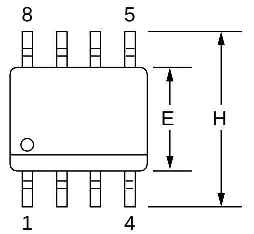
# Mechanical Dimensions (continued)

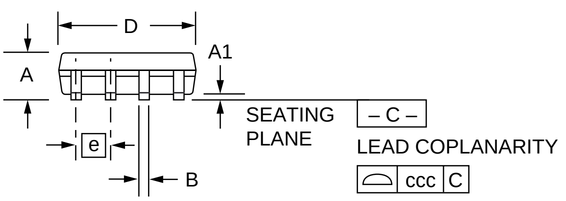
## 8-Lead SOIC Package

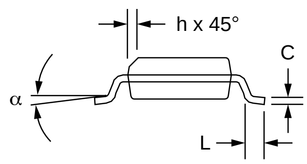
| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | |
| C | .008 | .010 | 0.20 | 0.25 | 5 |
| D | .189 | .197 | 4.80 | 5.00 | 2 |
| E | .150 | .158 | 3.81 | 4.01 | 2 |
| e | .050 BSC | | 1.27 BSC | | |
| H | .228 | .244 | 5.79 | 6.20 | |
| h | .010 | .020 | 0.25 | 0.50 | |
| L | .016 | .050 | 0.40 | 1.27 | 3 |
| N | 8 | | 8 | | 6 |
| α | 0° | 8° | 0° | 8° | |
| ccc | — | .004 | — | 0.10 | |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



## Ordering Information

| Part Number | Package | Operating Temperature Range |
|---|---|---|
| RV4140AN | 8-Lead Plastic DIP | -35°C to +80°C |
| RV4140AM | 8-Lead Plastic SOIC | -35°C to +80°C |

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# RV4141A

## Low Power Ground Fault Interrupter

### Features

- Powered from the AC line
- Built-in rectifier
- Direct interface to SCR
- 500 µA quiescent current
- Precision sense amplifier
- Adjustable time delay
- Minimum external components
- Meets UL 943 requirements
- For use with 110V or 220V systems
- Available in 8 pin DIP or SOIC package

### Description

The RV4141A is a low power controller for AC receptacle ground fault circuit interrupters. These devices detect hazardous current paths to ground and ground to neutral faults. The circuit interrupter then disconnects the load from the line before a harmful or lethal shock occurs.

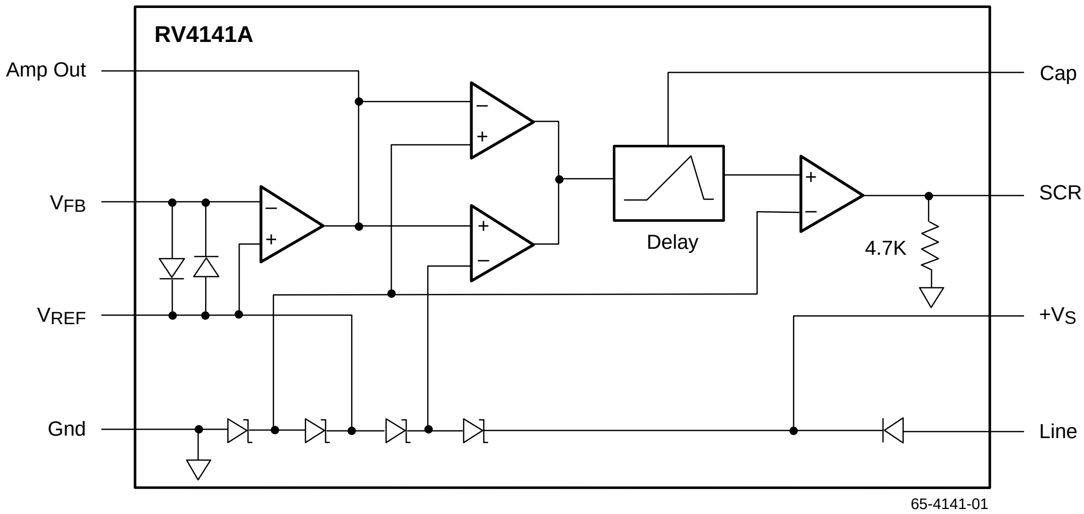
Internally, the RV4141A contains a diode rectifier, shunt regulator, precision sense amplifier, current reference, time delay circuit, and SCR driver.

Two sense transformers, SCR, solenoid, three resistors and four capacitors complete the design of the basic circuit interrupter. The simple layout and minimum component count insure ease of application and long term reliability.

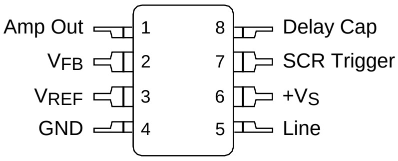
Features not found in other GFCI controllers include a low offset voltage sense amplifier eliminating the need for a coupling capacitor between the sense transformer and sense amplifier, and an internal rectifier to eliminate high voltage rectifying diodes.

The RV4141A is powered only during the positive half period of the line voltage, but can sense current faults independent of its phase relative to the line voltage. The gate of the SCR is driven only during the positive half cycle of the line voltage.

### Block Diagram



## Pin Assignments




65-4141A-02

## Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Current | | | | 10 | mA |
| Internal Power Dissipation | | | | 500 | mW |
| Storage Temperature Range | | -65 | | +150 | °C |
| Operating Temperature Range | | -35 | | +80 | °C |
| Junction Temperature | | | | 125°C | |
| Lead Soldering Temperature | 60 Sec, DIP | | | 300 | °C |
| | 10 Sec, SOIC | | | 260 | °C |

**Notes:**

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

## Thermal Characteristics

| Parameter | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal resistance | SOIC | | 240 | | °C/W |
| | | PDIP | | 160 | | °C/W |

## Electrical Characteristics ($I_{LINE}$ = 1.5mA and $T_A$ = +25°C, $R_{SET}$ = 650kΩ)

| Parameters | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Shunt Regulator (Pins 5 to 4)** | | | | | |
| Regulated Voltage | $I_{2-3}$ = 11µA | 25.0 | 27.0 | 29.0 | V |
| Regulated Voltage | $I_{LINE}$ = 750 µA, $I_{2-3}$ = 9µA | 25.0 | 27.0 | 29.0 | V |
| Quiescent Current | $V_{5-4}$ = 24V | — | 500 | — | µA |
| **Sense Amplifier (Pins 2 to 3)** | | | | | |
| Offset Voltage | | -200 | 0 | 200 | µV |
| Gain Bandwidth | (Design Value) | — | 1.5 | — | MHz |
| Input Bias Current | (Design Value) | | 30 | 100 | nA |
| **SCR Trigger (Pins 7 to 4)** | | | | | |
| Output Resistance | $V_{7-4}$ = Open, $I_{2-3}$ = µA | 3.8 | 4.7 | 5.6 | kΩ |
| Output Voltage | $I_{2-3}$ = 9µA | 0 | 0.1 | 10 | mV |
| Output Voltage | $I_{2-3}$ = 11µA | 2.4 | 3.0 | 3.6 | V |
| Output Current | $V_{7-4}$ = 0V, $I_{2-3}$ = 11µA | 400 | 600 | | µA |
| **Reference Voltage (Pins 3 to 4)** | | | | | |
| Reference Voltage | $I_{LINE}$ = 750 µA | 12.0 | 13.0 | 14.0 | V |
| **Delay Timer (Pins 8 to 4)** | | | | | |
| Delay Time (Note 1) | $C_{8-4}$ = 12nF | — | 2.0 | — | ms |
| Delay Current | $I_{2-3}$ = 11µA | 30 | 40 | 50 | µA |

**Note:**

1. Delay time is defined as starting when the instantaneous sense current ($I_{2-3}$) exceeds 6.5 V/$R_{SET}$ and ending when the SCR trigger voltage $V_{7-6}$ goes high.

## Circuit Operation

(Refer to Block Diagram and Figure 1)

The precision op amp connected to Pins 1 through 3 senses the fault current flowing in the secondary of the sense transformer, converting it to a voltage at Pin 1. The ratio of secondary current to output voltage is directly proportional to feedback resistor, $R_{SET}$.

$R_{SET}$ converts the sense transformer secondary current to a voltage at Pin 1. Due to the virtual ground created at the sense amplifier input by its negative feedback loop, the sense transformer's burden is equal to the value of $R_{IN}$. From the transformer's point of view, the ideal value for $R_{IN}$ is 0Ω. This will cause it to operate as a true current transformer with minimal error. However, making $R_{IN}$ equal to zero creates a large offset voltage at Pin 1 due to the sense amplifier's very high DC gain. $R_{IN}$ should be selected as high as possible consistent with preserving the transformer's operation as a true current mode transformer. A typical value for $R_{IN}$ is between 200 and 1000Ω.

As seen by the equation below, maximizing $R_{IN}$ minimizes the DC offset error at the sense amplifiers output. The DC offset voltage at Pin 1 contributes directly to the trip current error. The offset voltage at Pin 1 is:

$$V_{OS} \times R_{SET}/(R_{IN} + R_{SEC})$$

Where:
$V_{OS}$ = Input offset voltage of sense amplifier
$R_{SET}$ = Feedback resistor
$R_{IN}$ = Input resistor
$R_{SEC}$ = Transformer secondary winding resistance

The sense amplifier has a specified maximum offset voltage of 200 μV to minimize trip current errors.

Two comparators connected to the sense amplifier output are configured as a window detector, whose references are -6.5 volts and +6.5 volts referred to Pin 3. When the sense transformer secondary RMS current exceeds 4.6/$R_{SET}$ the output of the window detector starts the delay circuit. If the secondary current exceeds the predetermined trip current for longer than the delay time a current pulse appears at Pin 7, triggering the SCR.

The SCR anode is directly connected to a solenoid or relay coil. The SCR can be tripped only when its anode is more positive than its cathode.

### Supply Current Requirements

The RV4141A is powered directly from the line through a series limiting resistor called $R_{LINE}$, its value is between 24 kΩ and 91 kΩ. The controller IC has a built-in diode rectifier eliminating the need for external power diodes.

The recommended value for $R_{LINE}$ is 24 kΩ to 47 kΩ for 110V systems and 47 kΩ to 91 kΩ for 220V systems. When $R_{LINE}$ is 47 kΩ the shunt regulator current is limited to 3.6 mA. The recommended maximum peak line current through $R_{LINE}$ is 10 mA.

### GFCI Application (Refer to Figure 1)

The GFCI detects a ground fault by sensing a difference current in the line and neutral wires. The difference current is assumed to be a fault current creating a potentially hazardous path from iine to ground. Since the line and neutral wires pass through the center of the sense transformer, only the differential primary current is transferred to the secondary. Assuming the turns ratio is 1:1000 the secondary current is 1/1000th the fault current. The RV4141A's sense amplifier converts the secondary current to a voltage which is compared with either of the two window detector reference voltages. If the fault current exceeds the design value for the duration of the programmed time delay, the RV4141A will send a current pulse to the gate of the SCR.

Detecting ground to neutral faults is more difficult. $R_B$ represents a normal ground fault resistance, $R_N$ is the wire resistance of the electrical circuit between load/ neutral and earth ground. $R_G$ represents the ground to neutral fault condition. According to UL 943, the GFCI must trip when $R_N$ = 0.4Ω, $R_G$ = 1.6Ω and the normal ground fault is 6 mA.

Assuming the ground fault to be 5 mA, 1 mA and 4 mA will go through $R_G$ and $R_N$, respectively, causing an effective 1 mA fault current. This current is detected by the sense transformer and amplified by the sense amplifier. The ground/ neutral and sense transformers are now mutually coupled by $R_G$, $R_N$ and the neutral wire ground loop, producing a positive feedback loop around the sense amplifier. The newly created feedback loop causes the sense amplifier to oscillate at a frequency determined by ground/neutral transformer secondary inductance and C4. Typically it occurs at 8 KHz.

C2 is used to program the time required for the fault to be present before the SCR is triggered. Refer to the equation below for calculating the value of C2. Its typical value is 12 nF for a 2 ms delay.

$R_{SET}$ is used to set the fault current at which the GFCI trips. When used with a 1:1000 sense transformer, its typical value is 1 MΩ for a GFCI designed to trip at 5 mA.

$R_{IN}$ should be the highest value possible which insures a predictable secondary current from the sense transformer. If $R_{IN}$ is set too high, normal production variations in the transformer permeability will cause unit to unit variations in the secondary current. If it is too low, a large offset voltage error at Pin 1 will be present. This error voltage in turn creates a trip current error proportional to the input offset voltage of the sense amplifier. As an example, if $R_{IN}$ is 500Ω,

$R_{SET}$ is 1 MΩ, $R_{SEC}$ is 45Ω and the $V_{OS}$ of the sense amplifier is its maximum of 200 μV, the trip current error is ±5.6%.

The SCR anode is directly connected to a solenoid or relay coil. It can be tripped only when its anode is more positive than its cathode. It must have a high dV/dt rating to ensure that line noise (generated by electrically noisy appliances) does not falsely trigger it. Also the SCR must have a gate drive requirement less than 200 μA. C3 is a noise filter that prevents high frequency line pulses from triggering the SCR.

The relay solenoid used should have a response time of 3 ms or less to meet the UL 943 timing requirement.

## Sense Transformers and Cores

The sense and ground/neutral transformer cores are usually fabricated using high permeability laminated steel rings. Their single turn primary is created by passing the line and neutral wires through the center of its core. The secondary is usually from 200 to 1500 turns.

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842 and Magnetics, 900 E. Butler Road, P.O. Box 391, Butler, PA 16003, (412) 282-8282 are full-line suppliers of ring cores and transformers designed specifically for GFCI and related applications.

## Calculating The Values Of $R_{SET}$ and C2

Determine the nominal ground fault trip current requirement. This will be typically 5 mA in North America (117V AC) and 22 mA in the UK and Europe (220V AC). Determine the minimum delay time required to prevent nuisance tripping. This will typically be 1 to 2 ms. The value of C2 required to provide the desired delay time is:

$$C2 = 6 \times T$$

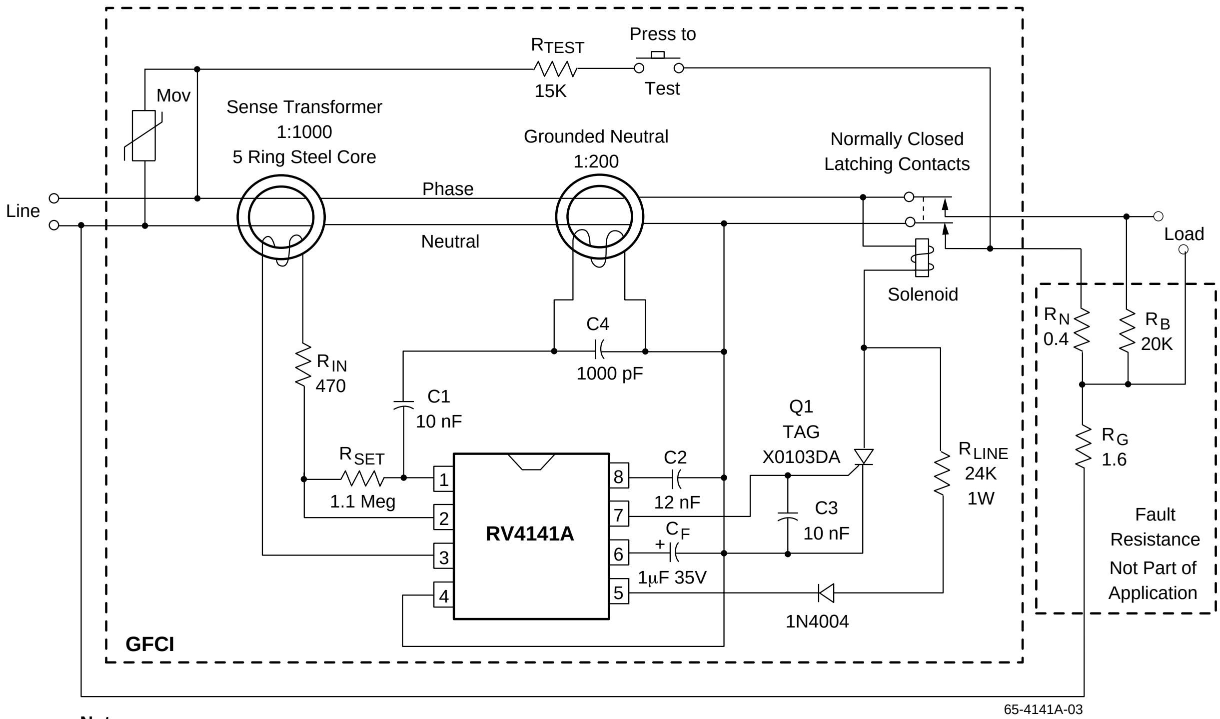
where:
C2 is in nF
T is the desired delay time in ms.

The value of $R_{SET}$ to meet the nominal ground fault trip current specification is:

$$R_{SET} = \frac{4.6 \times N}{I_{FAULT} \times COS\ 180(T/P)}$$

where:
$R_{SET}$ is in kΩ
T is the time delay in ms
P is the period of the line frequency in ms
$I_{FAULT}$ is the desired ground fault trip current in mA RMS
N is the number of sense transformer secondary turns.

This formula assumes an ideal sense transformer is used. The calculated value of $R_{SET}$ may have to be changed up to 30% to when using a non-ideal transformer.




**Note:**
1. Portions of this schematic are subject to U.S. patents 3,878,435 and Re. 30,678.

**Figure 1. GFI Application Circuit**

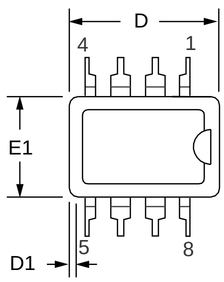
# Mechanical Dimensions

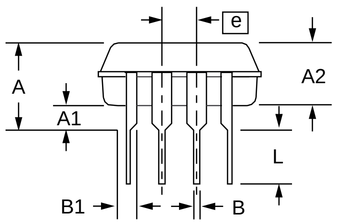
## 8-Lead Plastic DIP Package

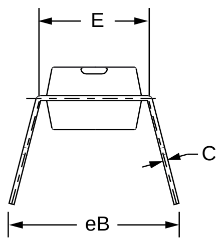
| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | — | .210 | — | 5.33 | |
| A1 | .015 | — | .38 | — | |
| A2 | .115 | .195 | 2.93 | 4.95 | |
| B | .014 | .022 | .36 | .56 | |
| B1 | .045 | .070 | 1.14 | 1.78 | |
| C | .008 | .015 | .20 | .38 | 4 |
| D | .348 | .430 | 8.84 | 10.92 | 2 |
| D1 | .005 | — | .13 | — | |
| E | .300 | .325 | 7.62 | 8.26 | |
| E1 | .240 | .280 | 6.10 | 7.11 | 2 |
| e | .100 BSC | | 2.54 BSC | | |
| eB | — | .430 | — | 10.92 | |
| L | .115 | .160 | 2.92 | 4.06 | |
| N | 8° | | 8° | | 5 |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



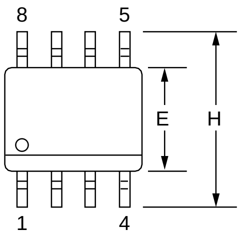
# Mechanical Dimensions (continued)

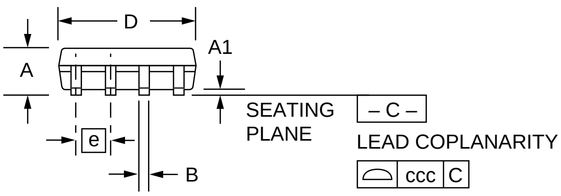
## 8-Lead SOIC Package

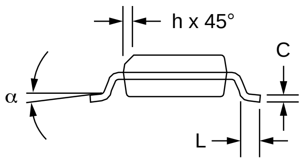
| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | **Min.** | **Max.** | **Min.** | **Max.** | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | |
| C | .008 | .010 | 0.20 | 0.25 | 5 |
| D | .189 | .197 | 4.80 | 5.00 | 2 |
| E | .150 | .158 | 3.81 | 4.01 | 2 |
| e | .050 BSC | | 1.27 BSC | | |
| H | .228 | .244 | 5.79 | 6.20 | |
| h | .010 | .020 | 0.25 | 0.50 | |
| L | .016 | .050 | 0.40 | 1.27 | 3 |
| N | 8 | | 8 | | 6 |
| $\alpha$ | 0° | 8° | 0° | 8° | |
| ccc | — | .004 | — | 0.10 | |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



## Ordering Information

| Part Number | Package | Operating Temperature Range |
|---|---|---|
| RV4141AN | 8-Lead Plastic DIP | -35°C to +80°C |
| RV4141AM | 8-Lead Plastic SOIC | -35°C to +80°C |

# Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RV/RV4141a.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RV4141a.pdf.

# RV4145A

## Low Power Ground Fault Interrupter

### Features

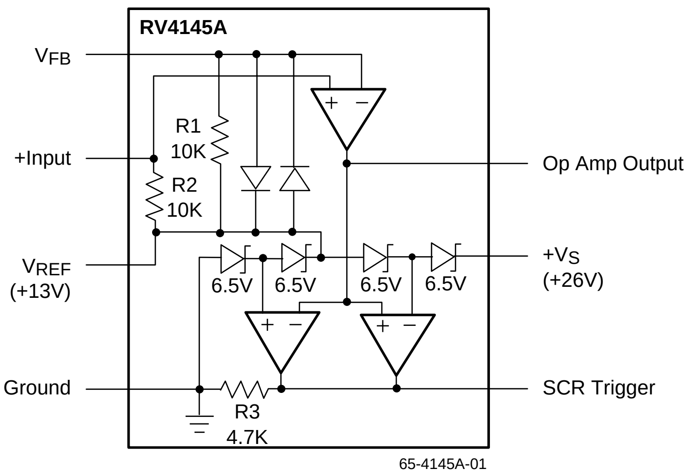
- No potentiometer required
- Direct interface to SCR
- Supply voltage derived from AC line – 26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets U.L. 943 standards
- 450µA quiescent current
- Ideal for 120V or 220V systems

### Description

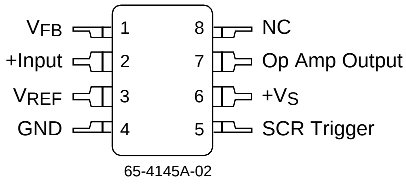
The RV4145A is a low power controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions, such as equipment (connected to opposite phases of the AC line) in contact with a pool of water and open circuits the line before a harmful or lethal shock occurs.

Contained internally are a 26V zener shunt regulator, an op amp, and an SCR driver. WIth the addition of two sense transformers, a bridge rectifier, an SCR, a relay, and a few additional components, the RV4145A will detect and protect against both hot wire to ground and neutral wire to ground faults. The simple layout and conventional design ensure ease of application and long-term reliability.

### Block Diagram



## Pin Assignments




## Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Current | | | | 18 | mA |
| Internal Power Dissipation | | | | 500 | mW |
| Storage Temperature Range | | -65 | | +150 | °C |
| Operating Temperature Range | | -35 | | +85 | °C |
| Junction Temperature | | | | 125°C | |
| Lead Soldering Temperature | 60 Sec, DIP | | | 300 | °C |
| | 10 Sec, SOIC | | | 260 | °C |
| $P_D$ $T_A$ < 50°C | SOIC | | | 300 | mW |
| | PDIP | | | 468 | mW |
| For $T_A$ > 50°C Derate at | SOIC | | 4.1 | | mW/°C |
| | PDIP | | 6.25 | | mW/°C |

**Notes:**

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

## Operating Conditions

| Parameter | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal resistance | SOIC | | 240 | | °C/W |
| | | PDIP | | 160 | | °C/W |

## Electrical Characteristics ($I_S$ = 1.5mA and $T_A$ = +25°C)

| Parameters | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Detector Reference Voltage | Pin 7 to Pin 3 | 6.8 | 7.2 | 8.1 | ±V |
| **Shunt Regulator** | | | | | |
| Zener Voltage (+$V_S$) | Pin 6 to Pin 4 | 25 | 26 | 29.2 | V |
| Reference Voltage ($V_{REF}$) | Pin 3 to Pin 4 | 12.5 | 13 | 14.6 | V |
| Quiescent Current ($I_S$) | +$V_S$ = 24V | | 450 | 750 | µA |
| **Operational Amplifier** | | | | | |
| Offset Voltage | Pin 2 to Pin 3 | -3.0 | 0.5 | +3.0 | mV |
| +Output Voltage Swing | Pin 7 to Pin 3 | 6.8 | 7.2 | 8.1 | V |
| –Output Voltage Swing | Pin 7 to Pin 3 | -9.5 | -11.2 | -13.5 | V |
| +Output Source Current | Pin 7 to Pin 3 | | 650 | | µA |
| –Output Source Current | Pin 7 to Pin 3 | | 1.0 | | mA |
| Gain Bandwidth Product | F = 50KHz | 1.0 | 1.8 | | MHz |
| **Resistors** | **$I_S$ = 0mA** | | | | |
| R1 | Pin 1 to Pin 3 | | 10 | | kΩ |
| R2 | Pin 2 to Pin 3 | | 10 | | kΩ |
| R3 | Pin 5 to Pin 4 | 3.5 | 4.7 | 5.9 | kΩ |
| **SCR Trigger Voltage** | **Pin 5 to Pin 4** | | | | |
| Detector On | | 1.5 | 2.8 | | V |
| Detector Off | | 0 | 1 | 10 | mV |

## Electrical Characteristics ($I_S$ = 1.5mA and -35°C ≤ $T_A$ ≤ +85°C)

| Parameters | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Detector Reference Voltage | Pin 7 to Pin 3 | 6.5 | 7.2 | 8.3 | ±V |
| **Shunt Regulator** | | | | | |
| Zener Voltage (+$V_S$) | Pin 6 to Pin 4 | 24 | 26 | 30 | V |
| Reference Voltage ($V_{REF}$) | Pin 3 to Pin 4 | 12 | 13 | 15 | V |
| Quiescent Current ($I_S$) | +$V_S$ = 23V | | 500 | | µA |
| **Operational Amplifier** | | | | | |
| Offset Voltage | Pin 2 to Pin 3 | -5.0 | 0.5 | +5.0 | mV |
| +Output Voltage Swing | Pin 7 to Pin 3 | 6.5 | 7.2 | 8.3 | V |
| –Output Voltage Swing | Pin 7 to Pin 3 | -9 | -11.2 | -14 | V |
| Gain Bandwidth Product | F = 50KHz | | 1.8 | | MHz |
| **Resistors** | **$I_S$ = 0mA** | | | | |
| R1 | Pin 1 to Pin 3 | | 10 | | kΩ |
| R2 | Pin 2 to Pin 3 | | 10 | | kΩ |
| R3 | Pin 5 to Pin 4 | 3.5 | 4.7 | 5.9 | kΩ |
| **SCR Trigger Voltage** | **Pin 5 to Pin 4** | | | | |
| Detector On | | 1.3 | 2.8 | | V |
| Detector Off | | 0 | 3 | 50 | mV |

## Principles of Operation

The 26V shunt regulator voltage generated by the string of zener diodes is divided into three reference voltages: 3/4 $V_S$, 1/2 $V_S$, and 1/4 $V_S$. $V_{REF}$ is at 1/2VS and is used as a reference to create an artifical ground of +13V at the op amp non-inverting input.

Figure 1 shows a three-wire 120V AC outlet GFI application using an RV4145A. Fault signals from the sense transformer are AC coupled into the input and are amplified according to the following equation:

$$V_7 = R_{SENSE} \times I_{SENSE}/N$$

Where $V_7$ is the RMS voltage at pin 7 relative to pin 3, $R_{SENSE}$ is the value of the feedback resistor connected from pin 7 to pin 1, $I_{SENSE}$ is the fault current in amps RMS and N is the turns ratio of the transformer. When $V_7$ exceeds plus or minus 7.2V relative to pin 3 the SCR Trigger output will go high and fire the external SCR.

The formula for $V_7$ is approximate because it does not include the sense transformer characteristics.

Grounded neutral fault detection is accomplished when a short or fault closes a magnetic path between the sense transformer and the grounded neutral transformer. The resultant AC coupling closes a positive feedback path around the op amp, and therefore the op amp oscillates. When the peaks of the oscillation voltage exceed the SCR trigger comparator thresholds, the SCR output will go high.

### Shunt Regulator

$R_{LINE}$ limits the current into the shunt regulator; 220V applications will require substituting a 47kΩ 2W resistor. In addition to supplying power to the IC, the shunt regulator creates internal reference voltages (see above).

### Operational Amplifier

$R_{SENSE}$ is a feedback resistor that sets gain and therefore sensitivity to normal faults. To adjust $R_{SENSE}$, follow this procedure: apply the desired fault current (a difference in current of 5mA is the UL 943 standard). Adjust $R_{SENSE}$ upward until the SCR activates. A fixed resistor can be used for $R_{SENSE}$, since the resultant ±15% variation in sensitivity will meet UL's 943 4-6mA specification window.

The roll-off frequency is greater than the grounded neutral fault oscillation frequency, in order to preserve loop gain for oscillation (which is determined by the inductance of the 200:1 transformer and C4).

The senstivity to grounded neutral faults is adjusted by changing the frequency of oscillation. Increasing the frequency reduces the sensitivity by reducing the loop gain of the positive feedback circuit. As frequency increases, the signal becomes attenuated and the loop gain decreases. With the values shown the circuit will detect a grounded neutral fault having resistance of 2Ω or less.

The input to the op amp are protected from overvoltage by back-toback diodes.

### SCR Driver

The SCR used must have a high dV/dt rating to ensure that line noise (generated by noisy appliances such as a drill motor) does not falsely trigger the SCR. Also, the SCR must have a gate drive requirement of less than 200μA. $C_F$ is a noise filter capacitor that prevents narrow pulses from firing the SCR.

The relay solenoid used should have a 3ms or less response time in order to meet the UL 943 timing requirement.

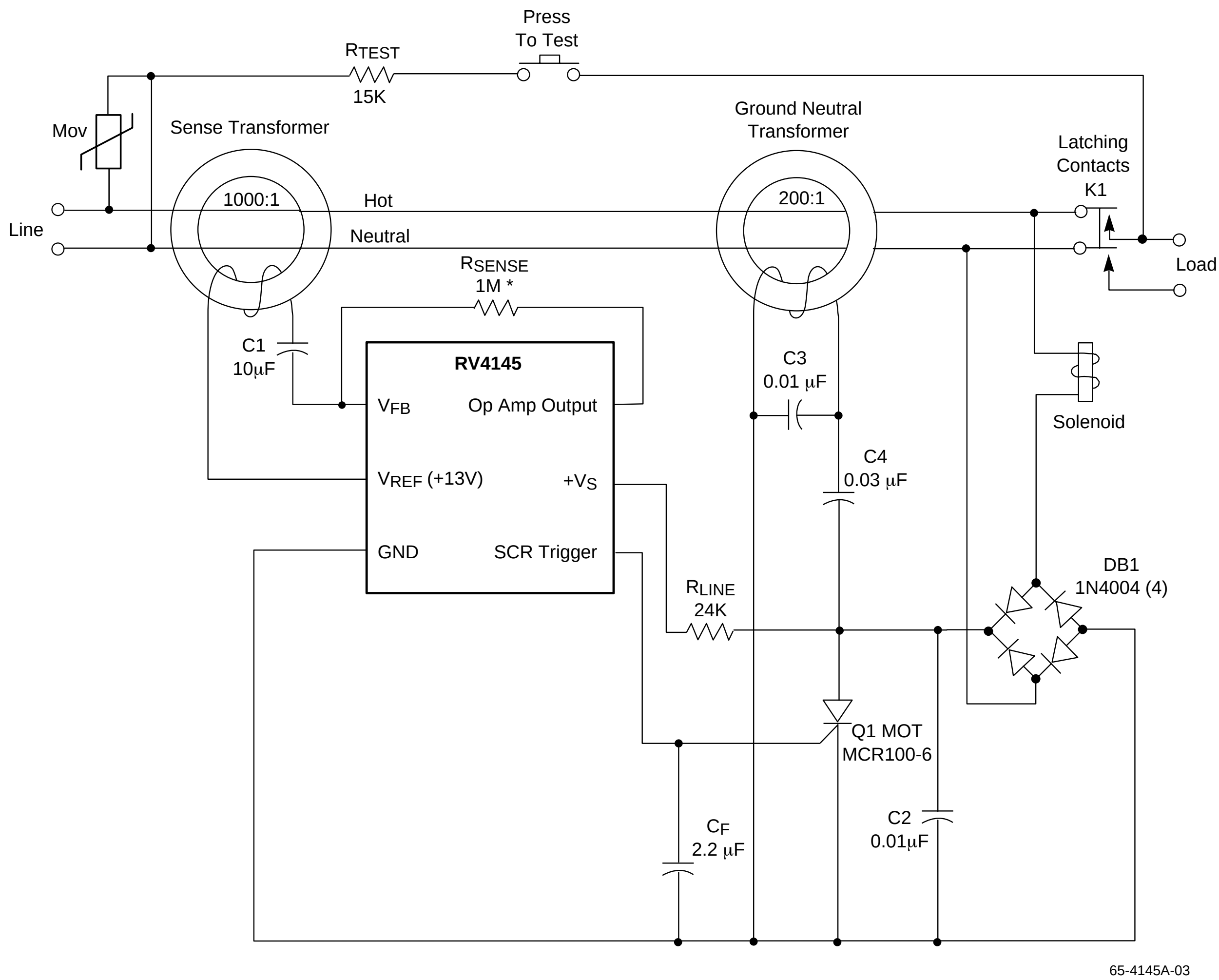
## Sense Transformers and Cores

The sense and grounded neutral transformer cores are usually fabricated using high permeability laminated steel rings. Their single turn primary is created by passing the line and neutral wires through the center of its core. The secondary is usually from 200 to 1500 turns.

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842, and Magnetics, 900 E. Butler Road, P.O. Box 391, Butler, PA 16003, (412) 282-8282 are full line suppliers of ring cores and transformers designed specifically for GFI applications.

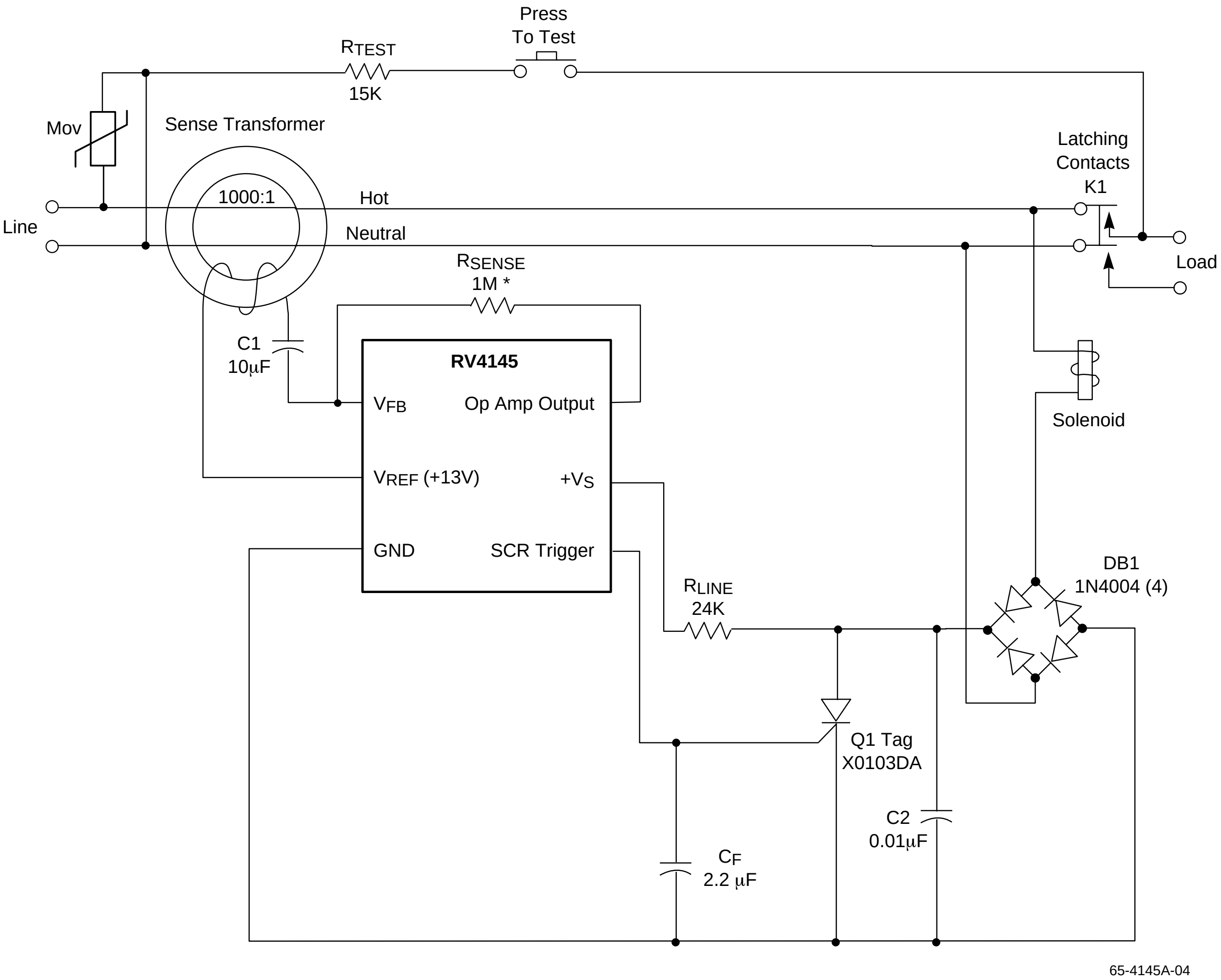
## Two-Wire Application Circuit

Figure 2 shows the diagram of a 2-wire 120V AC outlet GFI circuit using an RV4145A. This circuit is not designed to detect grounded neutral faults. Thus, the grounded neutral transformer and capacitors C3 and C4 of Figure 1 are not used.




* Value depends on transformer characteristics.

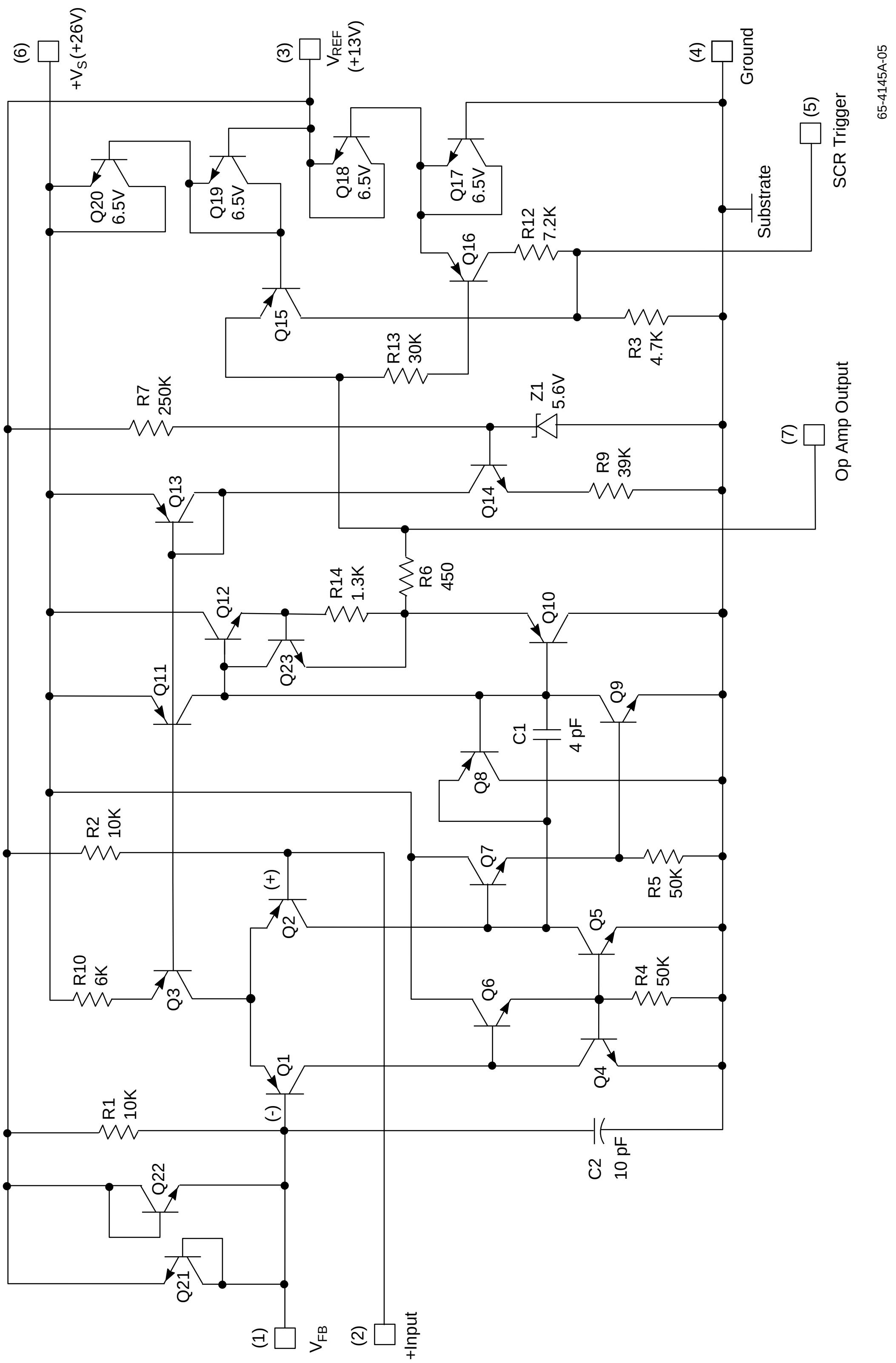
**Figure 1. GFI Application Circuit (Three-Wire Outlet)**




* Value depends on transformer characteristics.

**Figure 2. GFI Application Circuit (Two-Wire Outlet)**

## Schematic Diagram



## Notes:

## Notes:

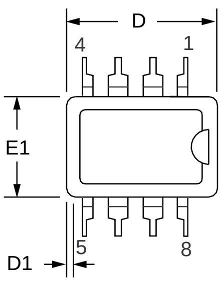
# Mechanical Dimensions

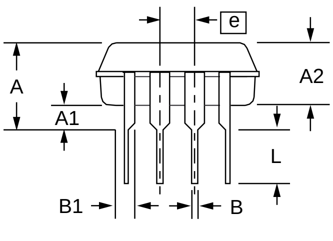
## 8-Lead Plastic DIP Package

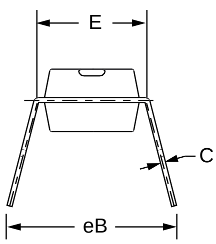
| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | — | .210 | — | 5.33 | |
| A1 | .015 | — | .38 | — | |
| A2 | .115 | .195 | 2.93 | 4.95 | |
| B | .014 | .022 | .36 | .56 | |
| B1 | .045 | .070 | 1.14 | 1.78 | |
| C | .008 | .015 | .20 | .38 | 4 |
| D | .348 | .430 | 8.84 | 10.92 | 2 |
| D1 | .005 | — | .13 | — | |
| E | .300 | .325 | 7.62 | 8.26 | |
| E1 | .240 | .280 | 6.10 | 7.11 | 2 |
| e | .100 BSC | | 2.54 BSC | | |
| eB | — | .430 | — | 10.92 | |
| L | .115 | .160 | 2.92 | 4.06 | |
| N | 8° | | 8° | | 5 |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



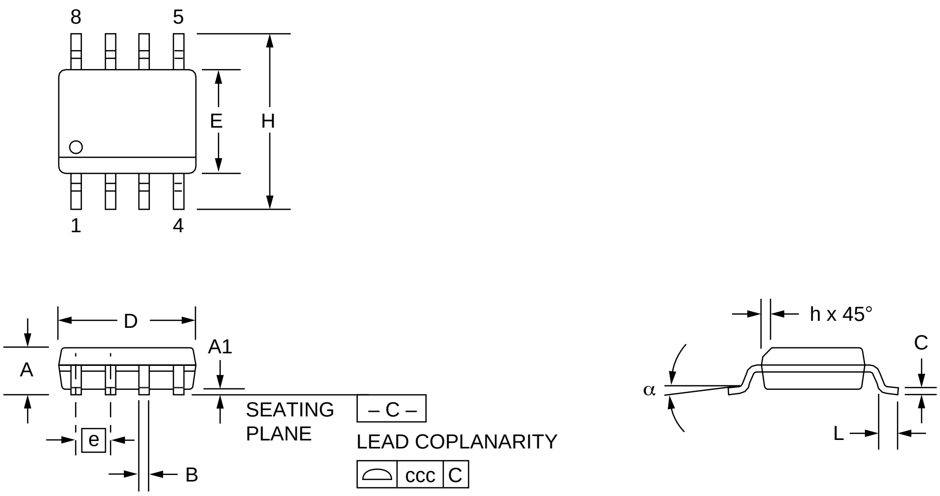
# Mechanical Dimensions (continued)

## 8-Lead SOIC Package

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | **Min.** | **Max.** | **Min.** | **Max.** | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | |
| C | .008 | .010 | 0.20 | 0.25 | 5 |
| D | .189 | .197 | 4.80 | 5.00 | 2 |
| E | .150 | .158 | 3.81 | 4.01 | 2 |
| e | .050 BSC | | 1.27 BSC | | |
| H | .228 | .244 | 5.79 | 6.20 | |
| h | .010 | .020 | 0.25 | 0.50 | |
| L | .016 | .050 | 0.40 | 1.27 | 3 |
| N | 8 | | 8 | | 6 |
| $\alpha$ | 0° | 8° | 0° | 8° | |
| ccc | — | .004 | — | 0.10 | |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



## Ordering Information

| Part Number | Package | Operating Temperature Range |
|---|---|---|
| RV4145AN | 8-Lead Plastic DIP | -35°C to +85°C |
| RV4145AM | 8-Lead Plastic SOIC | -35°C to +85°C |

# Embedded Secure Document

The file *http://www.fairchildsemi.com/ds/RV/RV4145a.pdf* is a secure document that has been embedded in this document. Double click the pushpin to view RV4145a.pdf.

# RV4146
# Low Power Ground Fault Interrupter

## Description

The RV4146 is a low power controller for AC receptacle ground fault circuit interrupters. These devices detect hazardous current paths to ground and ground to neutral faults. The circuit interrupter then disconnects the load from the line before a harmful or lethal shock occurs.

Internally, the RV4146 contains an oscillator, shunt regulator, precision sense amplifier, current reference, time delay circuit, and SCR driver.

Two sense transformers, SCR, solenoid, four diodes, three resistors and four capacitors complete the design of the basic circuit interrupter. The simple layout and minimum component count insure ease of application and long term reliability.

Features not found in other GFCI controllers include a low offset voltage sense amplifier, eliminating the need for a coupling capacitor between the sense transformer and sense amplifier, and an internal oscillator to eliminate the sensitivities of the dormant oscillator

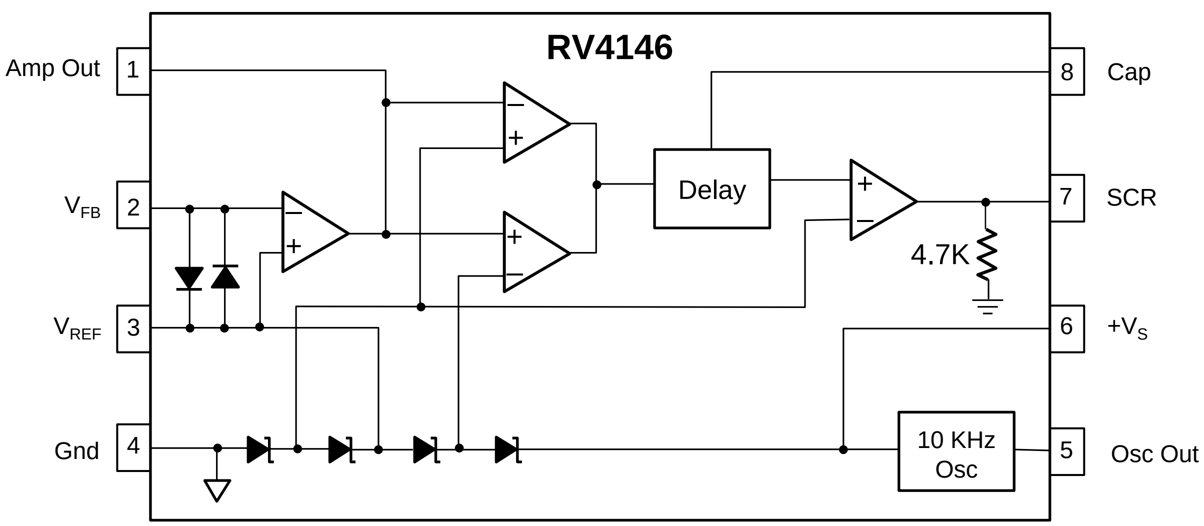
## Features

- Built-in grounded neutral oscillator
- Direct interface to SCR
- 1 mA quiescent current
- Precision sense amplifier
- Adjustable time delay
- Minimum external components
- Meets UL 943 requirements
- For use with 110V or 220V systems
- Available in 8 pin DIP or SOIC package
- Differential circuitry for noise immunity
- Trip time dependent on fault magnitude

The RV4146 senses current faults independent of its phase relative to the line voltage. The gate of the SCR is driven during both cycles of the line voltage.

Noise immunity is maximized on the RVxxxx, but the use of differential circuitry with 3 times the discharge current as charge, and low output impedance on the SCR driver.

## Functional Block Diagram




65-????

## Absolute Maximum Ratings

Supply Current ....................................... 10 mA
Internal Power Dissipation.................... 500 mW
Storage Temperature
    Range ............................... -65°C to +150°C
Operating Temperature
    Range ................................. -35°C to +80°C
Lead Soldering Temperature
    (60 Sec., DIP) ..................................+300°C
    (10 Sec., SO) ..................................+260°C

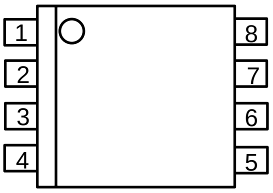
## Ordering Information

| Part Number | Package | Operating Temperature Range |
|---|---|---|
| RV4146N | N | -35°C to +80°C |
| RV4146M | M | -35°C to +80°C |

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC

## Connection Information

**8-Lead Plastic**
**Dual In-Line SO-8**
(Top View)

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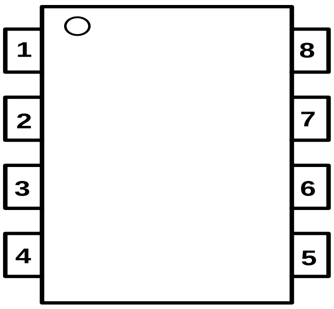
**8-Lead Plastic**
**Dial In-Line Package**
(Top View)




65-0093

| Pin | Function |
|---|---|
| 1 | Amp Out |
| 2 | $V_{FB}$ |
| 3 | $V_{REF}$ (+13V) |
| 4 | Ground |
| 5 | Line |
| 6 | $+V_S$ |
| 7 | SCR Trigger |
| 8 | Delay Cap |

## Thermal Characteristics

| | 8-Lead Plastic SOIC | 8-Lead Plastic DIP |
|---|---|---|
| Max. Junction Temp. | +125°C | +125°C |
| Max. $P_D$ $T_A$ <50°C | 300 mW | 468 mW |
| Therm. Res $\theta_{JC}$ | — | — |
| Therm. Res. $\theta_{JA}$ | 240°C/W | 160°C/W |
| For $T_A$ >50°C Derate at | 4.1 mW per °C | 6.25 mW per °C |

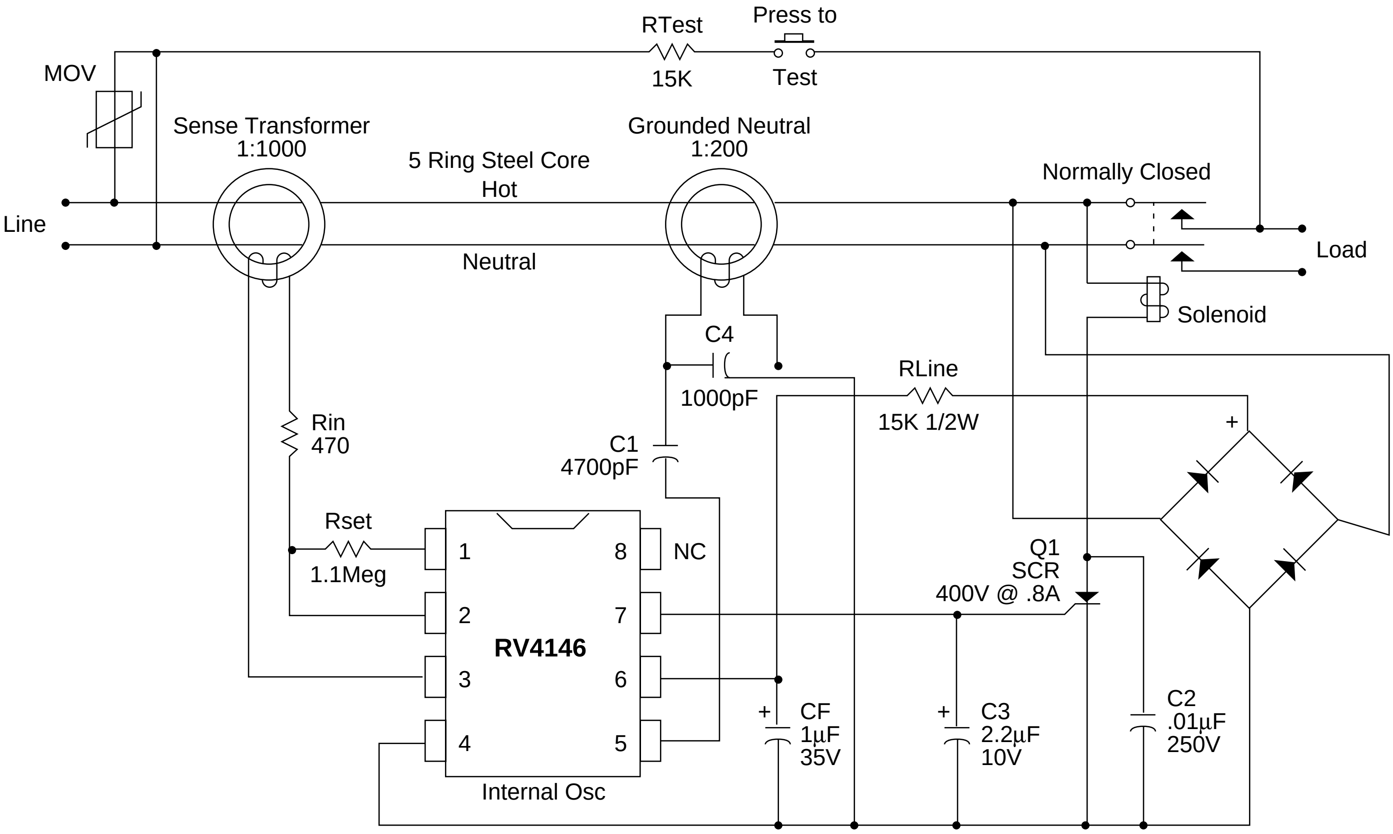



Figure 1. GFI Application Circuit (Full-Wave)

## Electrical Characteristics

($I_{LINE}$ = 2.5 mA and $T_A$ = +25°C, $R_{SET}$ = 650 kΩ)

| Parameters | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Shunt Regulator** (Pins 6 to 4) | | | | | |
| Regulated Voltage | $I_{2-3}$ = 11 µA | 25.0 | 27.0 | 29.0 | Volts |
| Regulated Voltage | $I_{LINE}$ = 750 µA, $I_{2-3}$ = 9 µA | 25.0 | 27.0 | 29.0 | Volts |
| Quiescent Current | $V_{5-4}$ = 24V | — | 51 | — | mA |
| **Sense Amplifier** (Pins 2 to 3) | | | | | |
| Offset Voltage | | 250 | 0 | 250 | µV |
| Gain Bandwidth | (Design Value) | — | 1.5 | — | MHz |
| Input Bias Current | (Design Value) | | 30 | 100 | nA |
| **SCR Trigger** (Pins 7 to 4) | | | | | |
| Output Voltage | $I_{2-3}$ = 9 µA | 0 | 0.1 | .2 | V |
| Output Voltage | $I_{2-3}$ = 11 µA | 2.4 | 3.0 | 3.6 | Volts |
| Output Current | $V_{7-4}$ = 0V, $I_{2-3}$ = 11 µA | 500 | 1000 | 2500 | µA |
| **Reference Voltage** (Pins 3 to 4) | | | | | |
| Reference Voltage | $I_{LINE}$ = 750 µA | 12.0 | 13.0 | 14.0 | Volts |
| **Delay Timer** (Pins 8 to 4) | | | | | |
| Delay Time (Note 1) | $C_{8-4}$ = 12 nF | — | 2.0 | — | ms |
| Delay Current | $I_{2-3}$ = 11 µA | 30 | 40 | 50 | µA |
| **Oscillator** | | | | | |
| Frequency | | 5 | 10 | 15 | KHz |
| Voltage | | | 1.5 | | V |
| Output Current | | 2 | 4 | | mA |

Note:
1. Delay time is defined as starting when the instantaneous sense current ($I_{2-3}$) exceeds 6.5 V/$R_{SET}$ and ending when the SCR trigger voltage $V_{7-6}$ goes high.

## Circuit Operation

(Refer to Block Diagram and Figure 1)

The precision op amp connected to Pins 1 through 3 senses the fault current flowing in the secondary of the sense transformer, converting it to a voltage at Pin 1. The ratio of secondary current to output voltage is directly proportional to feedback resistor, $R_{SET}$.

$R_{SET}$ converts the sense transformer secondary current to a voltage at Pin 1. Due to the virtual ground created at the sense amplifier input by its negative feedback loop, the sense transformer's burden is equal to the value of $R_{IN}$. From the transformer's point of view, the ideal value for $R_{IN}$ is 0Ω. This will cause it to operate as a true current transformer with minimal error. However, making $R_{IN}$ equal to zero creates a large offset voltage at Pin 1 due to the sense amplifier's very high DC gain. $R_{IN}$ should be selected as high as possible consistent with preserving the transformer's operation as a true current mode transformer. A typical value for $R_{IN}$ is between 200 and 1000Ω.

As seen by the equation below, maximizing $R_{IN}$ minimizes the DC offset error at the sense amplifiers output. The DC offset voltage at Pin 1 contributes directly to the trip current error. The offset voltage at Pin 1 is:

$$V_{OS} \times R_{SET}/(R_{IN} + R_{SEC})$$

Where:
$V_{OS}$ = Input offset voltage of sense amplifier
$R_{SET}$ = Feedback resistor
$R_{IN}$ = Input resistor
$R_{SEC}$= Transformer secondary winding resistance

The sense amplifier has a specified maximum offset voltage of 200 μV to minimize trip current errors.

Two comparators connected to the sense amplifier output are configured as a window detector, whose references are -6.5 volts and +6.5 volts referred to Pin 3. When the sense transformer secondary RMS current exceeds $4.6/R_{SET}$ the output of the window detector starts the delay circuit. If the secondary current exceeds the predetermined trip current for longer than the delay time a current pulse appears at Pin 7, triggering the SCR.

The SCR anode is directly connected to a solenoid or relay coil. The SCR can be tripped only when its anode is more positive than its cathode.

### Supply Current Requirements

The RV4146 is powered directly from the line through a series limiting resistor called $R_{LINE}$, of 15 kΩ. The controller IC requires and external full wave bridge diode.

The recommended value for $R_{LINE}$ is 15 kΩ for 110V systems and 36 kΩ for 220V systems. When $R_{LINE}$ is 30 kΩ the shunt regulator current is limited to 5 mA. The recommended maximum peak line current through $R_{LINE}$ is 15 mA.

## GFCI Application

(Refer to Figure 1)

The GFCI detects a ground fault by sensing a difference current in the line and neutral wires. The difference current is assumed to be a fault current creating a potentially hazardous path from line to ground. Since the line and neutral wires pass through the center of the sense transformer, only the differential primary current is transferred to the secondary. Assuming the turns ratio is 1:1000 the secondary current is 1/1000th the fault current. The RV4146's sense amplifier converts the secondary current to a voltage which is compared with either of the two window detector reference voltages. If the fault current exceeds the design value for the duration of the programmed time delay, the RV4146 will send a current pulse to the gate of the SCR.

Detecting ground to neutral faults is more difficult. $R_B$ represents a normal ground fault resistance, $R_N$ is the wire resistance of the electrical circuit between load/ neutral and earth ground. $R_G$ represents the ground to neutral fault condition. According to UL 943, the GFCI must trip when $R_N$ = 0.4Ω, $R_G$ = 1.6Ω and the normal ground fault is 6 mA.

Assuming the ground fault to be 5 mA, 1 mA and 4 mA will go through $R_G$ and $R_N$, respectively, causing an effective 1 mA fault current. This current is detected by the sense transformer and amplified by the sense amplifier. The ground/neutral and sense transformers are mutually coupled by $R_G$, $R_N$ and the neutral wire ground loop, through the use of an on-board 10KHz oscillator.

C2 is used to program the time required for the fault to be present before the SCR is triggered. Refer to the equation below for calculating the value of C2. Its typical value is 12 nF for a 2 ms delay.

$R_{SET}$ is used to set the fault current at which the GFCI trips. When used with a 1:1000 sense transformer, its typical value is 1 MΩ for a GFCI designed to trip at 5 mA.

$R_{IN}$ should be the highest value possible which insures a predictable secondary current from the sense transformer. If $R_{IN}$ is set too high, normal production variations in the transformer permeability will cause unit to unit variations in the secondary current. If it is too low, a large offset voltage error at Pin 1 will be present. This error voltage in turn creates a trip current error proportional to the input offset voltage of the sense amplifier. As an example, if $R_{IN}$ is 500Ω, $R_{SET}$ is 1 MΩ, $R_{SEC}$ is 45Ω and the $V_{OS}$ of the sense amplifier is its maximum of 200 µV, the trip current error is ±5.6%.

The SCR anode is directly connected to a solenoid or relay coil. It can be tripped only when its anode is more positive than its cathode. It must have a high dV/dt rating to ensure that line noise (generated by electrically noisy appliances) does not falsely trigger it. Also the SCR must have a gate drive requirement less than 200 µA. C3 is a noise filter that prevents high frequency line pulses from triggering the SCR.

The relay solenoid used should have a response time of 3 ms or less to meet the UL 943 timing requirement.

## Sense Transformers and Cores

The sense and ground/neutral transformer cores are usually fabricated using high permeability laminated steel rings. Their single turn primary is created by passing the line and neutral wires through the center of its core. The secondary is usually from 200 to 1500 turns.

Magnetic Metals Corporation, Camden, NJ 08101, (609) 964-7842 and Magnetics, 900 E. Butler Road, P.O. Box 391, Butler, PA 16003, (412) 282-8282 are full-line suppliers of ring cores and transformers designed specifically for GFCI and related applications.

## Calculating The Values of $R_{SET}$ and C2

Determine the nominal ground fault trip current requirement. This will be typically 5 mA in North America (117V AC) and 22 mA in the UK and Europe (220V AC).

Determine the minimum delay time required to prevent nuisance tripping. This will typically be 1 to 2 ms.

The value of C2 required to provide the desired delay time is:

$$C2 = 6 \times T$$

where:
- C2 is in nF
- T is the desired delay time in ms.

The value of $R_{SET}$ to meet the nominal ground fault trip current specification is:

$$R_{SET} = \frac{4.6 \times N}{I_{FAULT} \times \cos 180(T/P)}$$

Where:
- $R_{SET}$ is in kΩ
- T is the time delay in ms
- P is the period of the line frequency in ms
- $I_{FAULT}$ is the desired ground fault trip current in mA RMS
- N is the number of sense transformer secondary turns.

This formula assumes an ideal sense transformer is used. The calculated value of $R_{SET}$ may have to be changed up to 30% to when using a non-ideal transformer.