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REALTEK 3.3V SINGLE CHIP FAST ETHERNET CONTROLLER WITH POWER MANAGEMENT RTL8139C(L)+

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1. Features

- 128 pin QFP/LQFP (pin-to-pin compatible with the RTL8139C(L))
- Software compatible to the RTL8139 series when configured in RTL8139C mode (C mode)
- Supports descriptor-based buffer management when configured in RTL8139C+ mode (C+ mode)
- Supports Microsoft* NDIS5 Checksum Offloads (IP, TCP, UDP), and Largesend Offload in C+ mode
- Supports IEEE802.1Q VLAN tagging in C+ mode
- Supports Transmit (Tx) Priority Queue for QoS, CoS applications in C+ mode
- Integrated Fast Ethernet MAC, PHY and transceiver in one chip
- 10Mbps and 100Mbps operation
- Supports 10Mbps and 100Mbps N-way Auto-negotiation operation
- PCI local bus single-chip Fast Ethernet controller
  - ✧ Compliant to PCI Revision 2.2
  - ✧ Supports PCI clocks 16.75MHz-40MHz
  - ✧ Supports PCI target fast back-to-back transaction
  - ✧ Supports Memory Read Line, Memory Read Multiple, Memory Write and Invalidate, and Dual Address Cycle, when set to C+ mode.
  - ✧ Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of the RTL8139C(L)+'s operational registers
  - ✧ Supports PCI VPD (Vital Product Data)
  - ✧ Supports ACPI, PCI power management
  - ✧ Supports optional PCI multi-function with additional function in slave mode only.
- Supports CardBus. The CIS can be stored in the 93C56 or expansion ROM
- Supports either MII or Boot ROM interface, though only one interface can be implemented at a time. Up to 128K byte Boot ROM interface for both EPROM and Flash memory can be supported
- Supports 25MHz crystal or 25MHz OSC as the internal clock source. The frequency deviation of either crystal or OSC must be within 50 PPM
- Compliant to PC99 and PC2001 standards
- Supports Wake-On-LAN function and remote wake-up (Magic Packet*, LinkChg and Microsoft wake-up frame)
- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse, and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power still remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space
- Includes a programmable, PCI burst size and early Tx/Rx threshold
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large (2Kbyte) independent receive (Rx) and transmit (Tx) FIFOs
- Advanced power saving mode when LAN function or wakeup function is not used
- Uses 93C46 (64*16-bit EEPROM) or 93C56 (128*16-bit EEPROM) to store resource configuration, ID parameter, and VPD data. The 93C56 can also be used to store the CIS data structure for the CardBus application
- Supports LED pins for various network activity indications
- Supports digital and analog loopback capability on both ports
- Half/Full duplex capability
- Supports Full Duplex Flow Control (IEEE 802.3x)
- 3.3V power supply with 5V tolerant I/Os

* Third-party brands and names are the property of their respective owners.

Note: The model number of the QFP package is RTL8139C+. The LQFP package model number is RTL8139CL+.

2. General Description

The Realtek RTL8139C(L)+ is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that is capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management. The RTL8139CL+ is suitable for applications such as CardBus or mobile with built-in network controller. The CIS data can be stored in either the 93C56 EEPROM or an external expansion ROM.

In addition to the ACPI feature, the RTL8139C(L)+ also supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft wake-up frame) in both ACPI and APM environments. The RTL8139C(L)+ is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is on and the main power remains off, the RTL8139C(L)+ is ready and waiting for the Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8139C(L)+ LWAKE pin provides motherboards with the Wake-On-LAN (WOL) function. The RTL8139C(L)+ also supports Analog Auto-Power-down, that is, the analog part of the RTL8139C(L)+ can be shut down temporarily according to user requirements or when the RTL8139C(L)+ is in a power down state with the wakeup function disabled. In addition, when the analog part is shut down and the IsolateB pin is low (i.e. the main power is off), then both the analog and digital parts stop functioning and power consumption of the RTL8139C(L)+ will be negligible. The RTL8139C(L)+ also supports an auxiliary power auto-detect function, and will auto-configure related bits of their own PCI power management registers in PCI configuration space.

The PCI Vital Product Data (VPD) is also supported to provide the information that uniquely identifies hardware (i.e., the RTL8139C(L)+ LAN card). The information may consist of part number, serial number, and other detailed information.

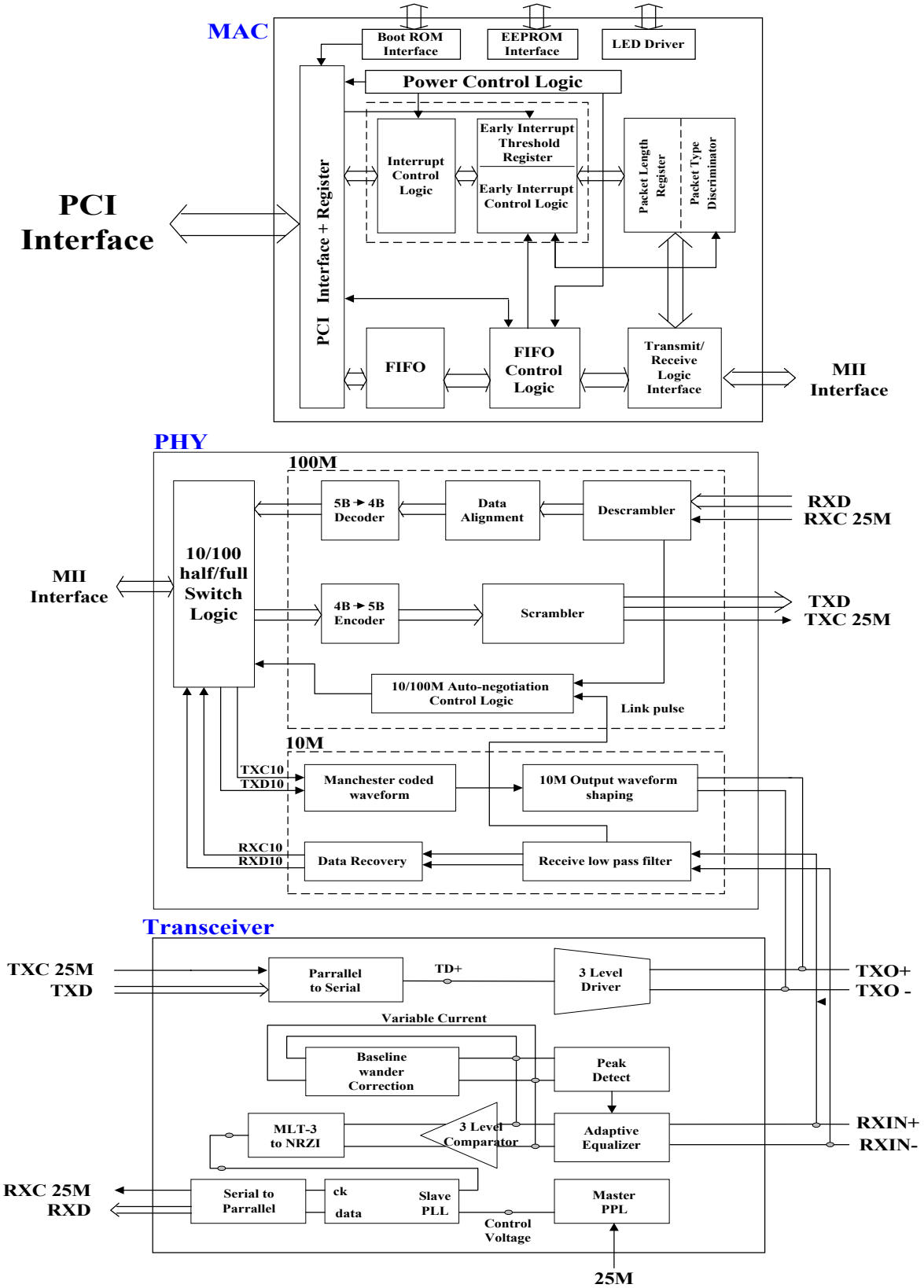
In order to provide a lower cost system, the RTL8139C(L)+ is capable of using a 25MHz crystal as its internal clock source. A 25MHz OSC can also be used.

There are 2 modes of buffer management modes which are supported by the RTL8139C(L)+. The first, C mode, is just like the buffer management algorithm which former RTL8139 series products use; the second is C+ mode (set only by software to the relative C+ mode registers and descriptors) which is an enhanced descriptor-based design especially suitable for server applications. The RTL8139C(L)+ is hardware compatible to the RTL8139C(L), and is software backwards compatible to the RTL8139 series when set to C mode (the default setting). The RTL8139C(L)+ can be configured by software to apply a new buffer management algorithm, i.e., enhanced descriptor-based buffer management architecture, which is an essential design as a modern network server card.

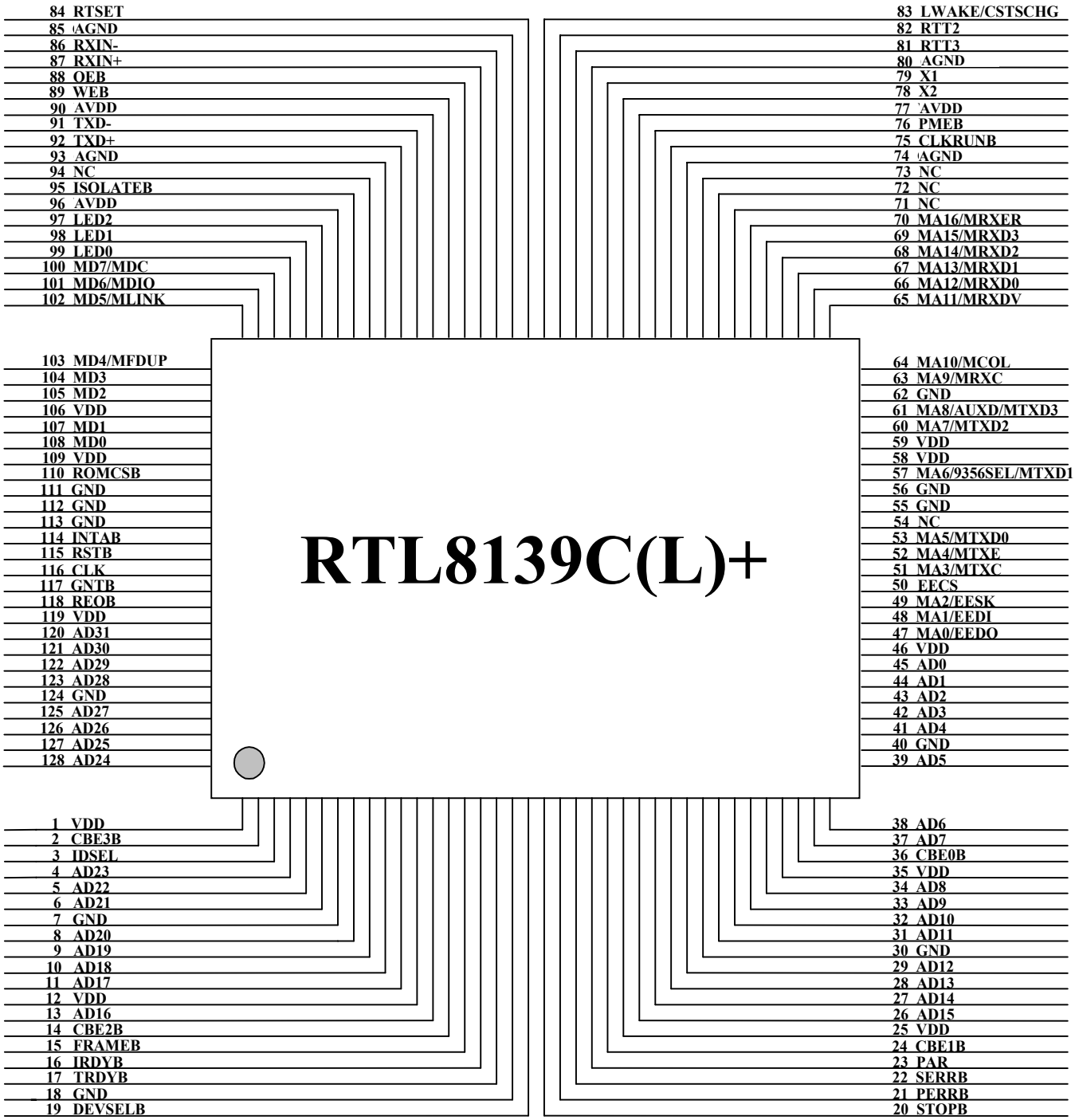
The RTL8139C(L)+ fully complies to Microsoft NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE802.1Q VLAN (Virtual Bridged Local Area Network). All of the above RTL8139C(L)+ new features contribute to lower CPU utilization, which is a plus when serving as a network server card. Also, the RTL8139C(L)+ boosts its PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, Memory Write and Invalidate when receiving. To be better qualified as a server card, the RTL8139C(L)+ also supports the PCI Dual Address Cycle (DAC) command, when the assigned buffers reside at the physical memory addresses higher than 4 Gigabytes. For QoS and CoS requirements, the RTL8139C(L)+ supports hardware high priority queuing to reduce software implementation effort and significantly improve performance.

The RTL8139C(L)+ keeps network maintenance costs low and eliminates usage barriers. It is the easiest way to upgrade a network from 10 to 100Mbps. It also supports full-duplex operation, making 200Mbps of bandwidth possible at no additional cost. To improve compatibility with other brands' products, the RTL8139C(L)+ is also capable of receiving packets with InterFrameGap no less than 40 Bit-Time. The RTL8139C(L)+ is highly integrated and requires no "glue" logic or external memory. It includes an interface for a boot ROM and can be used in diskless workstations, providing maximum network security and ease of management. For special applications, the RTL8139C(L)+ also supports an MII interface, which can be used, for example, to provide a redundant link with an external PHYceiver, or a connection to a Fiber channel with a Fiber transceiver. Because of pin count limitation, the RTL8139C(L)+ does not support a Boot ROM interface when the MII interface is used, and vice versa.

3. Block Diagram



4. Pin Assignments



5. Pin Descriptions

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In those cases, the functions are separated with a "/" symbol. Refer to the Pin Assignment diagram for a graphical representation.

5.1 Power Management/Isolation Interface

Symbol	Type	Pin No	Description
PMEB (PME#)	O/D	76	**Power Management Event:** Open drain, active low. Used by the RTL8139C(L)+ to request a change in its current power management state and/or to indicate that a power management event has occurred.
ISOLATEB (ISOLATE#)	I	95	**Isolate Pin:** Active low. Used to isolate the RTL8139C(L)+ from the PCI bus. The RTL8139C(L)+ does not drive its PCI outputs (excluding PME#) and does not sample its PCI input (including RST# and PCICLK) as long as the Isolate pin is asserted.
LWAKE/ CSTSCHG	O	83	**LAN WAKE-UP Signal (When CardB_En=0, bit2 Config3):** This signal is used to inform the motherboard to execute the wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 choices of output, including active high, active low, positive pulse, and negative pulse, that may be asserted from the LWAKE pin. Please refer to the LWACT bit in the CONFIG1 register and the LWPTN bit in the CONFIG4 register for the setting of this output signal. The default output is an active high signal. Once a PME event is received, the LWAKE and PMEB assert at the same time when the LWPME (bit4, CONFIG4) is set to 0. If the LWPME is set to 1, the LWAKE asserts only when the PMEB asserts and the ISOLATEB is low. **CSTSCHG Signal (When CardB_En=1, bit2 Config3):** This signal is used in CardBus applications only and is used to inform the motherboard to execute the wake-up process whenever a PME event occurs. This is always an active high signal, and the setting of LWACT (bit 4, Config1), LWPTN (bit2, Config4), and LWPME (bit4, Config4) mean nothing in this case. This pin is a 3.3V signaling output pin.

5.2 PCI Interface

Symbol	Type	Pin No	Description
AD31-0	T/S	120-123, 125-128, 4-6, 8-11, 13, 26-29, 31-34, 37-39, 41-45	PCI address and data multiplexed pins.
C/BE3-0	T/S	2, 14, 24, 36	PCI bus command and byte enables multiplexed pins.
CLK	I	116	**Clock:** This PCI Bus clock provides timing for all transactions and bus phases, and is input to PCI devices. The rising edge defines the start of each phase. The clock frequency ranges from 0 to 33MHz. For network operation to be functional, the PCI Bus clock frequency should be higher than 16.75MHz.
CLKRUNB	I/O	75	**Clock Run:** This signal is used by the RTL8139C(L)+ to request starting (or speeding up) the clock, CLK. CLKRUNB also indicates the clock status. For the RTL8139C(L)+, CLKRUNB is an open drain output as well as an input. The RTL8139C(L)+ requests the central resource to start, speed up, or maintain the interface clock by the assertion of CLKRUNB. For the host system, it is an S/T/S signal. The host system (central resource) is responsible for maintaining CLKRUNB asserted, and for driving it high to the negated (deasserted) state.
DEVSELB	S/T/S	19	**Device Select:** As a bus master, the RTL8139C(L)+ samples this signal to insure that a PCI target recognizes the destination address for the data transfer. As a target, the RTL8139C(L)+ asserts this signal low when it recognizes its target address after FRAMEB is asserted.
FRAMEB	S/T/S	15	**Cycle Frame:** As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is deasserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
GNTB	I	117	**Grant:** This signal is asserted low to indicate to the RTL8139C(L)+that the central arbiter has granted ownership of the bus to the RTL8139C(L)+. This input is used when the RTL8139C(L)+is acting as a bus master.
REQB	T/S	118	**Request:** The RTL8139C(L)+will assert this signal low to request the ownership of the bus from the central arbiter.
IDSEL	I	3	**Initialization Device Select**: This pin allows the RTL8139C(L)+to identify when configuration read/write transactions are intended for it.
INTAB	O/D	114	**Interrupt A:** Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, and Interrupt Mask registers.
IRDYB	S/T/S	16	**Initiator Ready**: This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal will be asserted low when the RTL8139C(L)+is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYB	S/T/S	17	**Target Ready:** This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations and with the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in

			conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low.
PAR	T/S	23	**Parity:** This signal indicates even parity across AD31-0 and C/BE3-0 including the PAR pin. As a master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
PERRB	S/T/S	21	**Parity Error:** When the RTL8139C(L)+is the bus target and a parity error is detected, the RTL8139C(L)+asserts this PERRB pin low.
SERRB	O/D	22	**System Error:** If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, RTL8139C(L)+ asserts both SERRB pin low and bit 14 of Status register in Configuration Space.
STOPB	S/T/S	20	**Stop:** Indicates the current target is requesting the master to stop the current transaction.
RSTB	I	115	**Reset:** When RSTB is asserted low, the RTL8139C(L)+ performs an internal system hardware reset. RSTB must be held for a minimum of 120 ns.

5.3 FLASH/BootPROM/EEPROM/MII Interface

Symbol	Type	Pin No	Description
			In Boot PROM (or flash) Mode:
MA[16:9], MA7, MA[5:3]	O	70-63, 60, 53-51	**MA16-3:** (In Boot PROM mode only) Output pins as Boot PROM address bus. These pins are used to access up to a 128k-byte flash memory or EPROM.
MA8	O, I	61	**MA8:** (In both Boot PROM mode and MII mode) Input pin as Aux. Power detect pin to detect if Aux. power exists or not, when initial power-on or PCI reset is de-asserted. Besides connecting this pin to Boot PROM or MII TXD3, it should be pulled high to the Aux. power via a resistor to detect Aux. power. If this pin is not pulled high to the Aux. power, the RTL8139C(L)+ assumes that no Aux. power exists. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. power via a resistor.
MA6	O, I	57	**MA6/9356SEL:** (In both Boot PROM mode and MII mode) Input pin as 9356 select pin at initial power-up. When this pin is pulled high with a 10KΩ resistor, the 93C56 EEPROM is used to store the resource data and CIS for the RTL8139C(L)+. The RTL8139C(L)+ latches the status of this pin at power-up to determine what EEPROM(93C46 or 93C56) is used, afterwards, this pin is used as MA6 or MTXD1.
			In MII mode:
MRXER(MA16)	I	70	**MII Receive Error:** (MA16 in MII mode) This pin is asserted to indicate that invalid symbol has been detected in 100Mbps MII mode. This signal is synchronized to RXC and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the ISE bit of the RSR register in the header of the Rx packet.
MRXD[3:0](MA[15:12])	I	69-66	**MII Receive Data:** (MA15-12 in MII mode) This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXC by the external physical unit.
MRXDV(MA11)	I	65	**MII Receive Data Valid:** (MA11 in MII mode) Data valid is asserted by an external PHY when receive data is present on the MRXD[3:0] lines, and it is deasserted at the end of the packet. This signal is valid on the rising of the MRXC.
MCOL(MA10)	I	64	**MII Collision Detected:** (MA10 in MII mode) This signal is asserted high synchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
MRXC(MA9)	I	63	**MII Receive Clock:** (MA9 in MII mode) This is a continuous clock that is recovered from the incoming data. MRXC is 25MHz in 100Mbps and 2.5Mhz in 10Mbs.
MTXD[3:0](MA[8:5])	O	61, 60, 57, 53	**MII Transmit Data:** (MA8-5 in MII mode) Four parallel transmit data lines which are driven synchronous to the MTXC for transmission by the external physical layer chip.

MTXE(MA4)	O	52	**MII Transmit Enable:** (MA4 in MII mode) Indicates the presence of valid nibble data on MTXD[3:0].
MTXC(MA3)	I	51	**MII Transmit Clock:** (MA3 in MII mode) MTXC is a continuous clock that provides a timing reference for the transfer of MTXD[3:0], MTXE. In MII mode, it uses the 25 MHz or 2.5 MHz supplied by the external PMD device.
MA2/EESK	O	49	The MA2-0 pins are switched to EESK, EEDI, EEDO in 93C46 (93C56) programming or auto-load mode.
MA1/EEDI	O	48	
MA0/EEDO	O, I	47	
EECS	O	50	**93C46 (93C56) Chip Select**
MD0-7	I/O	108, 107, 105-100	Boot PROM data bus in Boot PROM mode.
MDC(MD7)	O	100	**MDC:** (MD7 at MII mode) Management Data Clock: Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks.
MDIO(MD6)	I/O	101	**MDIO:** (MD6 in MII mode) Management Data: Bi-directional signal used to transfer management information.
MLINK(MD5)	I	102	**MLINK:** (MD5 in MII mode) link status notification from external PHYceiver.
MFDUP(MD4)	I	103	**MFDUP:** (MD4 in MII mode) full-duplex status notification from external PHYceiver.
ROMCSB	O	110	**ROM Chip Select:** This is the chip select signal of the Boot PROM.
OEB	O	88	**Output Enable:** This enables the output buffer of the Boot PROM or Flash memory during a read operation.
WEB	O	89	**Write Enable:** This signal strobes data into the Flash memory during a write cycle.

5.4 Power Pins

Symbol	Type	Pin No	Description
VDD	P	1, 12, 25, 35, 46, 58, 59, 106, 109, 119	**Digital Power +3.3V**
AVDD	P	77, 90, 96	**Analog Power +3.3V**
GND	P	7, 18, 30, 40, 55, 56, 62, 111, 112, 113, 124	**Digital Ground**
AGND	P	74, 80, 85, 93	**Analog Ground**

5.5 LED Interface

Symbol	Type	Pin No	Description
LED0, 1, 2	O	99, 98, 97	LED pins

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ACT
LED1	LINK100	LINK10/100	LINK10/100	LINK100/ACT
LED2	LINK10	FULL	Rx	FULL

During power down mode, the LEDs are OFF.

5.6 Attachment Unit Interface

Symbol	Type	Pin No	Description
TXD+ TXD-	O O	92 91	**100/10BASE-T transmit (Tx) Data**
RXIN+ RXIN-	I I	87 86	**100/10BASE-T receive (Rx) Data**
X1	I	79	**25 MHz crystal/OSC. Input**
X2	O	78	**Crystal Feedback Output:** This output is used in crystal connection only. It must be left open when X1 is driven with an external 25MHz oscillator.

5.7 Test and Other Pins

Symbol	Type	Pin No	Description
RTT2-3	TEST	81, 82	Chip test pins.
RTSET	I/O	84	This pin must be pulled low by a resistor. Please refer to the application circuit for correct value.
NC	-	54, 71, 72, 73, 94	**Reserved**

6. Register Descriptions

The RTL8139C(L)+ provides the following set of operational registers mapped into PCI memory space or I/O space.

Offset	R/W	Tag		Description	
0000h	R/W	IDR0		**ID Register 0:** The ID registers 0-5 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from the EEPROM EthernetID field.	
0001h	R/W	IDR1		**ID Register 1**	
0002h	R/W	IDR2		**ID Register 2**	
0003h	R/W	IDR3		**ID Register 3**	
0004h	R/W	IDR4		**ID Register 4**	
0005h	R/W	IDR5		**ID Register 5**	
0006h-0007h	-	-		**Reserved**	
0008h	R/W	MAR0		**Multicast Register 0:** The MAR registers 0-7 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers.	
0009h	R/W	MAR1		**Multicast Register 1**	
000Ah	R/W	MAR2		**Multicast Register 2**	
000Bh	R/W	MAR3		**Multicast Register 3**	
000Ch	R/W	MAR4		**Multicast Register 4**	
000Dh	R/W	MAR5		**Multicast Register 5**	
000Eh	R/W	MAR6		**Multicast Register 6**	
000Fh	R/W	MAR7		**Multicast Register 7**	
0010h-0013h	R/W	TSD0		**Transmit Status of Descriptor 0** (C mode only)	**Dump Tally Counter Command Register** (C+ mode only)
0014h-0017h	R/W	TSD1		**Transmit Status of Descriptor 1** (C mode only)	
0018h-001Bh	R/W	TSD2		**Transmit Status of Descriptor 2** (C mode only)	
001Ch-001Fh	R/W	TSD3		**Transmit Status of Descriptor 3** (C mode only)	
0020h-0023h	R/W	TSAD0	TNPDS	**Transmit Start Address (32-bit) of Descriptor0** (C mode only, double-word alignment)	**Transmit Normal Priority Descriptors Start address** (64-bit). (C+ mode only, 256-byte alignment)
0024h-0027h	R/W	TSAD1		**Transmit Start Address (32-bit) of Descriptor1** (C mode only, double-word alignment)	
0028h-002Bh	R/W	TSAD2	THPDS	**Transmit Start Address (32-bit) of Descriptor2** (C mode only, double-word alignment)	**Transmit High Priority Descriptors Start address** (64-bit). (C+ mode only, 256-byte alignment)
002Ch-002Fh	R/W	TSAD3		**Transmit Start Address (32-bit) of Descriptor3** (C mode only, double-word alignment)	
0030h-0033h	R/W	RBSTART		**Receive (Rx) Buffer Start Address** (C mode only, double-word alignment)	
0034h-0035h	R	ERBCR		**Early Receive (Rx) Byte Count Register**	
0036h	R	ERSR		**Early Rx Status Register**	
0037h	R/W	CR		**Command Register**	
0038h-0039h	R/W	CAPR		**Current Address of Packet Read** (C mode only, the initial value is 0FFF0h)	
003Ah-003Bh	R	CBR		**Current Buffer Address:** The initial value is 0000h. It reflects total received byte-count in the Rx buffer. (C mode only)	
003Ch-003Dh	R/W	IMR		**Interrupt Mask Register**	
003Eh-003Fh	R/W	ISR		**Interrupt Status Register**	
0040h-0043h	R/W	TCR		**Transmit (Tx) Configuration Register**	
0044h-0047h	R/W	RCR		**Receive (Rx) Configuration Register**	

0048h-004Bh	R/W	TCTR	**Timer Count Register:** This register contains a 32-bit general-purpose timer. Writing any value to this 32-bit register will reset the original timer and begin to count from zero.
004Ch-004Fh	R/W	MPC	**Missed Packet Counter:** Indicates the number of packets discarded due to Rx FIFO overflow. It is a 24-bit counter. After a s/w reset, MPC is cleared. Only the lower 3 bytes are valid. Writing any value to this register will reset MPC.
0050h	R/W	9346CR	**93C46 (93C56) Command Register**
0051h	R/W	CONFIG0	**Configuration Register 0**
0052h	R/W	CONFIG1	**Configuration Register 1**
0053H	-	-	**Reserved**
0054h-0057h	R /W	TimerInt	**Timer Interrupt Register:** When a nonzero value is written to this register, the Timeout bit of the ISR register will be set whenever the TCTR reaches this value. The Timeout bit will never be set as long as the TimerInt register is zero.
0058h	R/W	MSR	**Media Status Register**
0059h	R/W	CONFIG3	**Configuration register 3**
005Ah	R/W	CONFIG4	**Configuration register 4**
005Bh	-	-	**Reserved**
005Ch-005Dh	R/W	MULINT	**Multiple Interrupt Select**
005Eh	R	RERID	**PCI Revision ID** = 10h
005Fh	-	-	**Reserved**
0060h-0061h	R	TSAD	**Transmit Status of All Descriptors** (C mode only)
0062h-0063h	R/W	BMCR	**Basic Mode Control Register**
0064h-0065h	R	BMSR	**Basic Mode Status Register**
0066h-0067h	R/W	ANAR	**Auto-Negotiation Advertisement Register**
0068h-0069h	R	ANLPAR	**Auto-Negotiation Link Partner Register**
006Ah-006Bh	R	ANER	**Auto-Negotiation Expansion Register**
006Ch-006Dh	R	DIS	**Disconnect Counter**
006Eh-006Fh	R	FCSC	**False Carrier Sense Counter**
0070h-0071h	R/W	NWAYTR	**N-way Test Register**
0072h-0073h	R	REC	**RX_ER Counter**
0074h-0075h	R/W	CSCR	**CS Configuration Register**
0076-0077h	-	-	**Reserved**
0078h-007Bh	R/W	PHY1_PARM	**PHY Parameter 1**
007Ch-007Fh	R/W	TW_PARM	**Twister Parameter**
0080h	R/W	PHY2_PARM	**PHY Parameter 2**
0081h	-	-	**Reserved**
0082-0083h	R	_TDOKLAddr	**Low Address of a Tx Descriptor with Tx DMA Ok**
0084h	R/W	CRC0	**Power Management CRC register0 for wakeup frame0**
0085h	R/W	CRC1	**Power Management CRC register1 for wakeup frame1**
0086h	R/W	CRC2	**Power Management CRC register2 for wakeup frame2**
0087h	R/W	CRC3	**Power Management CRC register3 for wakeup frame3**
0088h	R/W	CRC4	**Power Management CRC register4 for wakeup frame4**
0089h	R/W	CRC5	**Power Management CRC register5 for wakeup frame5**
008Ah	R/W	CRC6	**Power Management CRC register6 for wakeup frame6**
008Bh	R/W	CRC7	**Power Management CRC register7 for wakeup frame7**
008Ch–0093h	R/W	Wakeup0	**Power Management wakeup frame0 (64bit)**
0094h–009Bh	R/W	Wakeup1	**Power Management wakeup frame1 (64bit)**
009Ch–00A3h	R/W	Wakeup2	**Power Management wakeup frame2 (64bit)**
00A4h–00ABh	R/W	Wakeup3	**Power Management wakeup frame3 (64bit)**
00ACh–00B3h	R/W	Wakeup4	**Power Management wakeup frame4 (64bit)**
00B4h–00BBh	R/W	Wakeup5	**Power Management wakeup frame5 (64bit)**

00BCh–00C3h	R/W	Wakeup6	**Power Management wakeup frame6 (64bit)**
00C4h–00CBh	R/W	Wakeup7	**Power Management wakeup frame7 (64bit)**
00CCh	R/W	LSBCRC0	**LSB of the mask byte of wakeup frame0 within offset 12 to 75**
00CDh	R/W	LSBCRC1	**LSB of the mask byte of wakeup frame1 within offset 12 to 75**
00CEh	R/W	LSBCRC2	**LSB of the mask byte of wakeup frame2 within offset 12 to 75**
00CFh	R/W	LSBCRC3	**LSB of the mask byte of wakeup frame3 within offset 12 to 75**
00D0h	R/W	LSBCRC4	**LSB of the mask byte of wakeup frame4 within offset 12 to 75**
00D1h	R/W	LSBCRC5	**LSB of the mask byte of wakeup frame5 within offset 12 to 75**
00D2h	R/W	LSBCRC6	**LSB of the mask byte of wakeup frame6 within offset 12 to 75**
00D3h	R/W	LSBCRC7	**LSB of the mask byte of wakeup frame7 within offset 12 to 75**
00D4h-00D7h	R/W	FLASH	**Flash memory read/write register**
00D8h	R/W	Config5	**Configuration register 5**
00D9h	W	TPPoll	**Transmit Priority Polling register** (C+ mode only)
00DAh-00DFh	-	-	**Reserved**
00E0h-00E1h	R/W	C+CR	**C+ Command Register** (C+ mode only)
00E2h-00E3h	--	-	**Reserved**
00E4h-00EBh	R/W	RDSAR	**Receive Descriptor Start Address Register** (C+ mode only, 256-byte alignment)
00ECh	R/W	ETThR	**C+ Early Transmit Threshold Register** (C+ mode only)
00EDh-00EFh	-	-	**Reserved**
00F0h-00F3h	R/W	FER	**Function Event Register** (Cardbus only)
00F4h-00F7h	R/W	FEMR	**Function Event Mask Register** (CardBus only)
00F8h-00FBh	R	FPSR	**Function Present State Register** (CardBus only)
00FCh-00FFh	W	FFER/MIIR	**Function Force Event Register** (CardBus only)/MII Register (Auto-Detect or MII mode only)

6.1 Receive Status Register in Rx Packet Header (C mode only)

Bit	R/W	Symbol	Description
15	R	MAR	**Multicast Address Received:** This bit set to 1 indicates that a multicast packet is received.
14	R	PAM	**Physical Address Matched:** This bit set to 1 indicates that the destination address of this packet matches the value written in ID registers.
13	R	BAR	**Broadcast Address Received:** This bit set to 1 indicates that a broadcast packet is received. BAR, MAR bit will not be set simultaneously.
12-6	-	-	**Reserved**
5	R	ISE	**Invalid Symbol Error:** (100BASE-TX only) This bit set to 1 indicates that an invalid symbol was encountered during the reception of this packet.
4	R	RUNT	**Runt Packet Received:** This bit set to 1 indicates that the received packet length is smaller than 64 bytes (i.e. media header + data + CRC < 64 bytes)
3	R	LONG	**Long Packet:** This bit set to 1 indicates that the size of the received packet exceeds 4k bytes.
2	R	CRC	**CRC Error:** When set, indicates that a CRC error occurred on the received packet.
1	R	FAE	**Frame Alignment Error:** When set, indicates that a frame alignment error occurred on this received packet.
0	R	ROK	**Receive OK:** When set, indicates that a good packet is received.

6.2 Transmit Status Register (TSD0-3)(Offset 0010h-001Fh, R/W, C mode only)

The read-only bits (CRS, TABT, OWC, CDH, NCC3-0, TOK, TUN) will be cleared by RTL8139C(L)+ when the Transmit Byte Count (bit12-0) in the corresponding Tx descriptor is written. It is not affected when software writes to these bits. These registers are only permitted to write by double-word access. After software reset, all bits except OWN bit are reset to "0".

Bit	R/W	Symbol	Description
31	R	CRS	**Carrier Sense Lost:** This bit is set to 1 when the carrier is lost during transmission of a packet.
30	R	TABT	**Transmit Abort:** This bit is set to 1 if the transmission of a packet was aborted. This bit is read only, writing to this bit is not affected.
29	R	OWC	**Out of Window Collision:** This bit is set to 1 if the RTL8139C(L)+ encountered an "out of window" collision during the transmission of a packet.
28	R	CDH	**CD Heart Beat:** The same as RTL8139(A/B). This bit is cleared in the 100 Mbps mode.
27-24	R	NCC3-0	**Number of Collision Count:** Indicates the number of collisions encountered during the transmission of a packet.
23-22	-	-	**Reserved**
21-16	R/W	ERTXTH5-0	**Early Tx Threshold:** Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet) the RTL8139C(L)+ will transmit this packet. 000000 = 8 bytes These fields count from 000001 to 111111 in unit of 32 bytes. This threshold must be avoided from exceeding 2K byte.
15	R	TOK	**Transmit OK:** Set to 1 indicates that the transmission of a packet was completed successfully and no transmit underrun occurs.
14	R	TUN	**Transmit FIFO Underrun:** Set to 1 if the Tx FIFO was exhausted during the transmission of a packet. The RTL8139C(L)+can re-transfer data if the Tx FIFO underruns and can also transmit the packet to the wire successfully even though the Tx FIFO underruns. That is, when TSD<TUN>=1, TSD<TOK>=0 and ISR<TOK>=1 (or ISR<TER>=1).
13	R/W	OWN	**OWN:** The RTL8139C(L)+sets this bit to 1 when the Tx DMA operation of this descriptor was completed. The driver must set this bit to 0 when the Transmit Byte Count (bit0-12) is written. The default value is 1.
12-0	R/W	SIZE	**Descriptor Size:** The total size in bytes of the data in this descriptor. If the packet length is more than 1792 byte (0700h), the Tx queue will be invalid, i.e. the next descriptor will be written only after the OWN bit of that long packet's descriptor has been set.

6.3 Dump Tally Counter Command Register (DTCCR) (Offset 0010h-0017h, R/W, C+ mode only)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>63-6</td><td>R/W</td><td>CntrAddr</td><td>Starting address of the 12 Tally Counters being dumped to. (64-byte alignment, 64 bytes long)
<table>
<tr><th>Offset of starting address</th><th>Counter</th><th>Description</th></tr>
<tr><td>0</td><td>TxOk</td><td>64-bit counter of Tx DMA Ok packets.</td></tr>
<tr><td>8</td><td>RxOk</td><td>64-bit counter of Rx Ok packets.</td></tr>
<tr><td>16</td><td>TxErr</td><td>64-bit packet counter of Tx errors including Tx abort, carrier lost, Tx underrun (should occur only on jumbo frames), and out of window collision.</td></tr>
<tr><td>24</td><td>RxErr</td><td>32-bit packet counter of Rx errors including CRC error packets (should be larger than 8 bytes) and missed packets.</td></tr>
<tr><td>28</td><td>MissPkt</td><td>16-bit counter of missed packets (CRC Ok) resulted from Rx FIFO full.</td></tr>
<tr><td>30</td><td>FAE</td><td>16-bit counter of Frame Alignment Error packets (MII mode only)</td></tr>
<tr><td>32</td><td>Tx1Col</td><td>32-bit counter of Tx Ok packets with only 1 collision occurring before Tx Ok.</td></tr>
<tr><td>36</td><td>TxMCol</td><td>32-bit counter of Tx Ok packets with more than 1 and less than 16 collisions happened before Tx Ok.</td></tr>
<tr><td>40</td><td>RxOkPhy</td><td>64-bit counter of all Rx Ok packets with physical addresses matching destination ID.</td></tr>
<tr><td>48</td><td>RxOkBrd</td><td>64-bit counter of all Rx Ok packets with broadcast destination ID.</td></tr>
<tr><td>56</td><td>RxOkMul</td><td>32-bit counter of all Rx Ok packets with multicast destination ID.</td></tr>
<tr><td>60</td><td>TxAbt</td><td>16-bit counter of Tx abort packets.</td></tr>
<tr><td>62</td><td>TxUndrn</td><td>16-bit counter of Tx underrun and discard packets (only possible on jumbo frames).</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>Cmd</td><td>Command:
- When set, the RTL8139C(L)+ begins dumping 13 Tally counters to the address specified above.
- When this bit is reset by RTL8139C(L)+, the dumping is completed.</td></tr>
<tr><td>2-0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

6.4 ERSR: Early Rx Status Register (Offset 0036h, R)

Bit	R/W	Symbol	Description
7-4	-	-	**Reserved**
3	R	ERGood	**Early Rx Good packet:** This bit is set whenever a packet is completely received and the packet is good. This bit is cleared when writing 1 to it.
2	R	ERBad	**Early Rx Bad packet:** This bit is set whenever a packet is completely received and the packet is bad. Writing 1 will clear this bit.
1	R	EROVW	**Early Rx OverWrite:** This bit is set when the RTL8139C(L)+'s local address pointer is equal to CAPR. In the early mode, this is different from buffer overflow. It happens that the RTL8139C(L)+ detected an Rx error and wanted to fill another packet data from the beginning address of that error packet. Writing 1 will clear this bit.
0	R	EROK	**Early Rx OK:** The power-on value is 0. It is set when the Rx byte count of the arriving packet exceeds the Rx threshold. After the whole packet is received, the RTL8139C(L)+ will set ROK or RER in ISR and clear this bit simultaneously. Setting this bit will invoke a ROK interrupt.

6.5 Command Register (Offset 0037h, R/W)

This register is used for issuing commands to the RTL8139C(L)+. These commands are issued by setting the corresponding bits for the function. A global software reset along with individual reset and enable/disable for transmitter and receiver are provided here.

Bit	R/W	Symbol	Description
7-5	-	-	**Reserved**
4	R/W	RST	**Reset:** Setting to 1 forces the RTL8139C(L)+ to a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, resets the system buffer pointer to the initial value (Tx buffer is at TSAD0, Rx buffer is empty). The values of IDR0-5 and MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the RTL8139C(L)+ when the reset operation is complete.
3	R/W	RE	**Receiver Enable:** When set to 1, and the receive state machine is idle, the receive machine becomes active. This bit will read back as a 1 whenever the receive state machine is active. After initial power-up, software must insure that the receiver has completely reset before setting this bit.
2	R/W	TE	**Transmitter Enable:** When set to 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit.
1	-	-	**Reserved**
0	R	BUFE	**Buffer Empty:** Rx Buffer Empty; There is no packet stored in the Rx buffer ring.

6.6 Interrupt Mask Register (Offset 003Ch-003Dh, R/W)

This register masks the interrupts that can be generated from the ISR. Writing a "1" to the bit enables the corresponding interrupt. During a hardware reset, all mask bits are cleared. Setting a mask bit allows the corresponding bit in the ISR to cause an interrupt. ISR bits are always set to 1, however, if the condition is present, regardless of the state of the corresponding mask bit.

Bit	R/W	Symbol	Description
15	R/W	SERR	**System Error Interrupt:** 1: Enable, 0: Disable.
14	R/W	TimeOut	**Time Out Interrupt:** 1: Enable, 0: Disable.
13	R/W	LenChg	**Cable Length Change Interrupt:** 1: Enable, 0: Disable.
12	-	-	**Reserved**
11	-	-	**Reserved**
10	-	-	**Reserved**
9	-	-	**Reserved**
8	R/W	_SWInt	**Software Interrupt:** 1: Enable, 0: Disable.
7	R/W	_TDU	**Tx Descriptor Unavailable Interrupt:** 1: Enable, 0: Disable.
6	R/W	FOVW	**Rx FIFO Overflow Interrupt**: 1: Enable, 0: Disable.
5	R/W	PUN/LinkChg	**Packet Underrun/Link Change Interrupt:** 1: Enable, 0: Disable.
4	R/W	RBO/_RDU	**Rx Buffer Overflow/Rx Descriptor Unavailable Interrupt:** 1: Enable, 0: Disable.
3	R/W	TER	**Tx Error Interrupt:** 1: Enable, 0: Disable.
2	R/W	TOK/TI	**Tx (OK) Interrupt:** 1: Enable, 0: Disable.
1	R/W	RER	**Rx Error Interrupt:** 1: Enable, 0: Disable.
0	R/W	ROK	**Rx OK Interrupt:** 1: Enable, 0: Disable.

6.7 Interrupt Status Register (Offset 003Eh-003Fh, R/W)

This register indicates the source of an interrupt when the INTA pin goes active. Enabling the corresponding bits in the Interrupt Mask Register (IMR) allows bits in this register to produce an interrupt. When an interrupt is active, one of more bits in this register are set to a "1". The interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the IMR. Writing a 1 to any bit will reset that bit, but writing a 0 has no effect.

Bit	R/W	Symbol	Description
15	R/W	SERR	**System Error:** Set to 1 when the RTL8139C(L)+ signals a system error on the PCI bus.
14	R/W	TimeOut	**Time Out:** Set to 1 when the TCTR register reaches to the value of the TimerInt register.
13	R/W	LenChg	**Cable Length Change:** Cable length is changed after Receiver is enabled.
12	-	-	**Reserved**
11	-	-	**Reserved**
10	-	-	**Reserved**
9	-	-	**Reserved**
8	R/W	_SWInt	**Software Interrupt:** (C+ mode only) i. Set to 1 whenever FSWInt (bit0, offset D9h, TPPoll register) is written 1 by software. ii. Reserved bit in C mode.
7	R/W	_TDU	**Tx Descriptor Unavailable**: (C+ mode only) i. When set, indicates Tx descriptor is unavailable. ii. Reserved bit in C mode.
6	R/W	FOVW	**Rx FIFO Overflow:** Caused by RBO/RDU, poor PCI performance, or overloaded PCI traffic.
5	R/W	PUN/LinkChg	**Packet Underrun/Link Change:** Set to 1 when CAPR is written but Rx buffer is empty, or when link status is changed.
4	R/W	RBO/_RDU	**Rx Buffer Overflow:** (C mode only) Set when receive (Rx) buffer ring storage resources have been exhausted. **Rx Descriptor Unavailable:** (C+ mode only) When set, indicates Rx descriptor is unavailable. The MPC (Missed Packet Counter, offset 4Ch-4Fh) indicates the number of packets discarded after the Rx FIFO overflow.
3	R/W	TER	**Transmit (Tx) Error:** Indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR setting
2	R/W	TOK/TI	**Transmit (Tx) OK:** (C mode only) Indicates that a packet transmission is completed successfully. **Transmit Interrupt:** (C+ mode only) Indicates that the DMA of the last descriptor of a Tx packet has completed and the last descriptor has been closed.
1	R/W	RER	**Receive (Rx) Error:** Indicates that a packet has either a CRC error or a frame alignment error (FAE). The collided frame will not be recognized as a CRC error if the length of this frame is shorter than 16 bytes.
0	R/W	ROK	**Receive (Rx) OK:** In normal mode, this indicates the successful completion of a packet reception. In early mode, this indicates that the Rx byte count of the arriving packet exceeds the early Rx threshold.

6.8 Transmit Configuration Register (Offset 0040h-0043h, R/W)

This register defines the Transmit Configuration for the RTL8139C(L). It controls such functions as Loopback, Heartbeat, Auto Transmit Padding, programmable Interframe Gap, Fill and Drain Thresholds, and maximum DMA burst size. The TCR register can only be changed after having set the TE (bit2, Command register, offset 0037h).

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>31</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>30-26</td><td>R</td><td>HWVERID</td><td>Hardware Version ID:
<table>
<tr><th></th><th>Bit30</th><th>Bit29</th><th>Bit28</th><th>Bit27</th><th>Bit26</th><th>Bit23</th></tr>
<tr><td>RTL8139</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139A</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139A-G</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>RTL8139B</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>RTL8130</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>RTL8139C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>RTL8139C+</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="6">All other combination</td></tr>
</table></td></tr>
<tr><td>25-24</td><td>R/W</td><td>IFG1, 0</td><td>Interframe Gap Time: This field allows adjustment of the interframe gap time below the standards of 9.6 us for 10Mbps, 960 ns for 100Mbps. The time can be programmed from 9.6 us to 8.4 us (10Mbps) and 960ns to 840ns (100Mbps). Note that any value of IFG [2:0] other than (0,1,1) will violate the IEEE 802.3 standard.
The formula for the inter frame gap is:
<table>
<tr><th colspan="3">IFG[2:0]</th><th>IFG@100MHz (nS)</th><th>IFG@10MHz (uS)</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>960</td><td>9.6</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>960 + 8 * 10</td><td>9.6 +8 * 0.1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>960 + 16 * 10</td><td>9.6 + 16 * 0.1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>960 + 24 * 10</td><td>9.6 + 24 * 0.1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>960 + 32 * 10</td><td>9.6 + 32 * 0.1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>960 + 40 * 10</td><td>9.6 + 40 * 0.1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>960 + 48 * 10</td><td>9.6 + 48 * 0.1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>960 + 96 * 10</td><td>9.6 + 96 * 0.1</td></tr>
</table></td></tr>
<tr><td>23</td><td>R</td><td>8139A-G</td><td>RTL8139A rev.G ID = 1. For others, this bit is 0.</td></tr>
<tr><td>22-20</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>19</td><td>R/W</td><td>IFG2</td><td>InterFrameGap2</td></tr>
<tr><td>18, 17</td><td>R/W</td><td>LBK1, LBK0</td><td>Loopback Test: There will be no packet on the TX+/- lines under the Loopback test condition. The loopback function must be independent of the link state.
00 : Normal operation
01 : Reserved
10 : Reserved
11 : Loopback mode</td></tr>
<tr><td>16</td><td>R/W</td><td>CRC</td><td>Append CRC:
0: A CRC is appended at the end of a packet
1: No CRC appended at the end of a packet</td></tr>
<tr><td>15-11</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>10-8</td><td>R/W</td><td>MXDMA2, 1, 0</td><td>Max DMA Burst Size per Tx DMA Burst: This field sets the maximum size of transmit DMA data bursts according to the following table:
000 = 16 bytes
001 = 32 bytes
010 = 64 bytes</td></tr>
</table>

			011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = 2048 bytes
7-4	R/W	TXRR	**Tx Retry Count:** These are used to specify additional transmission retries in multiples of 16 (IEEE 802.3 CSMA/CD retry count). If the TXRR is set to 0, the transmitter will re-transmit 16 times before aborting due to excessive collisions. If the TXRR is set to a value greater than 0, the transmitter will re-transmit a number of times equal to the following formula before aborting: Total retries = 16 + (TXRR * 16) The TER bit in the ISR register or transmit descriptor will be set when the transmission fails and reaches to this specified retry count.
3-1	-	-	**Reserved**
0	W	CLRABT	**Clear Abort:** (C mode only) Setting this bit to 1 causes the RTL8139C(L)+ to retransmit the packet at the last transmitted descriptor when this transmission was aborted. Setting this bit is only permitted in the transmit abort state.

6.9 Receive Configuration Register (Offset 0044h-0047h, R/W)

This register is used to set the receive configuration for the RTL8139C(L)+. Receive properties such as accepting error packets, runt packets, setting the receive drain threshold etc. are controlled here.

Bit	R/W	Symbol	Description
31-28	-	-	**Reserved**
27-24	R/W	ERTH3, 2, 1, 0	**Early Rx Threshold Bits:** These bits are used to select the Rx threshold multiplier of the whole packet that has been transferred to the system buffer in early mode when the frame protocol is under the RTL8139C(L)+'s definition. 0000 = No early Rx threshold 0001 = 1/16 0010 = 2/16 0011 = 3/16 0100 = 4/16 0101 = 5/16 0110 = 6/16 0111 = 7/16 1000 = 8/16 1001 = 9/16 1010 = 10/16 1011 = 11/16 1100 = 12/16 1101 = 13/16 1110 = 14/16 1111 = 15/16
23-18	-	-	**Reserved**

17	R/W	MulERINT	**Multiple Early Interrupt Select:** In C mode: When this bit is set, any received packet invokes early interrupt according to the MULINT<MISR[11:0]> setting in early mode. When this bit is reset, the packets of familiar protocols (IPX, IP, NDIS, etc) invoke early interrupts according to the RCR<ERTH[3:0]> setting in early mode. The packets of unfamiliar protocols will invoke early interrupts according to the setting of MULINT<MISR[11:0]>. In C+ mode: This bit enables/disables early interrupt according to the MULINT<MISR[11:0]> setting.
16	R/W	RER8	**Receive Error Packets Larger than 8 Bytes:** The RTL8139C(L)+ receives error packets with length larger than 8 bytes after setting the RER8 bit to 1. The RTL8139C(L)+ receives error packets larger than 64-bytes when the RER8 bit is cleared. The power-on default is zero. If AER or AR is set, the RER bit will be set when the RTL8139C(L)+ receives an error packet whose length is larger than 8 bytes. The RER8 setting is " Don't care " in this situation.
15-13	R/W	RXFTH2, 1, 0	**Rx FIFO Threshold:** Specifies the Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into the RTL8139C(L)+'s Rx FIFO, has reached this level (or the FIFO contains a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following table: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = No Rx threshold. The RTL8139C(L)+ begins the transfer of data after having received a whole packet in the FIFO.
12-11	R/W	RBLEN1, 0 (C mode only)	(C mode only) **Rx Buffer Length:** This field indicates the size of the Rx ring buffer. 00 = 8k + 16 byte 01 = 16k + 16 byte 10 = 32K + 16 byte 11 = 64K + 16 byte
10-8	R/W	MXDMA2, 1, 0	**Max DMA Burst Size per Rx DMA Burst:** This field sets the maximum size of the receive DMA data bursts according to the following table: 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes Other combinations are reserved.

7	R/W	WRAP (C mode only)	0: The RTL8139C(L)+ will transfer the rest of the packet data into the beginning of the Rx buffer if this packet has not been completely moved into the Rx buffer and the transfer has arrived at the end of the Rx buffer. 1: The RTL8139C(L)+ will keep moving the rest of the packet data into the memory immediately after the end of the Rx buffer, if this packet has not been completely moved into the Rx buffer and the transfer has arrived at the end of the Rx buffer. The software driver must reserve at least 1.5K bytes buffer to accept the remainder of the packet. We assume that the remainder of the packet is X bytes. The next packet will be moved into the memory from the X byte offset at the top of the Rx buffer. This bit is invalid when Rx buffer is selected to 64K bytes.
6	R	9356SEL	**EEPROM Select:** This bit reflects what type of EEPROM is used. 0: The EEPROM used is 9346. 1: The EEPROM used is 9356.
5	R/W	AER	**Accept Error Packets:** This bit determines if packets with CRC error, alignment error and/or collided fragments will be accepted or rejected. 0: Reject error packets 1: Accept error packets
4	R/W	AR	**Accept Runt Packets:** This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. 0: Reject runt packets 1: Accept runt packets
3	R/W	AB	**Accept Broadcast Packets:** This bit allows the receiver to accept or reject broadcast packets. 0: Reject broadcast packets 1: Accept broadcast packets
2	R/W	AM	**Accept Multicast Packets:** This bit allows the receiver to accept or reject multicast packets. 0: Reject multicast packets 1: Accept multicast packets
1	R/W	APM	**Accept Physical Match Packets:** This bit allows the receiver to accept or reject physical match packets. 0: Reject physical match packets 1: Accept physical match packets
0	R/W	AAP	**Accept Physical Address Packets:** This bit allows the receiver to accept or reject packets with a physical destination address. 0: Reject packets with a physical destination address 1: Accept packets with a physical destination address

6.10 9346CR: 93C46 (93C56) Command Register (Offset 0050h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7-6</td><td>R/W</td><td>EEM1-0</td><td>These 2 bits select the RTL8139C(L)+ operating mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal: RTL8139C(L)+ network/host communication mode.</td></tr>
<tr><td>0</td><td>1</td><td>Auto-load: Entering this mode will make the RTL8139C(L)+ load the contents of 93C46 (93C56), as when the RSTB signal is asserted. This auto-load operation will take about 2 ms. After it is completed, the RTL8139C(L)+ goes back to the normal mode automatically (EEM1 = EEM0 = 0) and all the other registers are reset to default values.</td></tr>
<tr><td>1</td><td>0</td><td>93C46 (93C56) Programming: In this mode, both network and host bus master operations are disabled. The 93C46 (93C56) can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config. Register Write Enable: Before writing to the CONFIG0, 1, 3, 4 registers, and bits 13, 12, 8 of BMCR (offset 62h-63h), the RTL8139C(L)+ must be placed in this mode. This will protect the RTL8139C(L)+ configuration from accidental change.</td></tr>
</table></td></tr>
<tr><td>4-5</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>EECS</td><td rowspan="4">These bits reflect the state of EECS, EESK, EEDI & EEDO pins in auto-load or 93C46 (93C56) programming mode.
Note: EESK, EEDI and EEDO are invalid during BootROM/FLASH access.</td></tr>
<tr><td>2</td><td>R/W</td><td>EESK</td></tr>
<tr><td>1</td><td>R/W</td><td>EEDI</td></tr>
<tr><td>0</td><td>R</td><td>EEDO</td></tr>
</table>

6.11 Configuration Register 0 (CONFIG 0) (Offset 0051h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7-3</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>2-0</td><td>R</td><td>BS2, BS1, BS0</td><td>Select Boot ROM size (Autoloaded from EEPROM)
<table>
<tr><th>BS2</th><th>BS1</th><th>BS0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No Boot ROM</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8K Boot ROM</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16K Boot ROM</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>32K Boot ROM</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>64K Boot ROM</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>128K Boot ROM</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>unused</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>unused</td></tr>
</table></td></tr>
</table>

6.12 Configuration Register 1 (CONFIG 1) (Offset 0052h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7-6</td><td>R/W</td><td>LEDS1-0</td><td>Refer to LED PIN definition. These bits initial value com from 93C46/93C56.</td></tr>
<tr><td>5</td><td>R/W</td><td>DVRLOAD</td><td>Driver Load: Software may use this bit to make sure that the driver has been loaded. Writing 1 is 1. Writing 0 is 0. When the command register bits IOEN, MEMEN, BMEN of PCI configuration space are written, the RTL8139C(L)+ will automatically clear this bit.</td></tr>
<tr><td>4</td><td>R/W</td><td>LWACT</td><td>LWAKE Active Mode: The LWACT and LWPTN bits in the CONFIG4 register are used to program the output signal of the LWAKE pin. According to the combination of these two bits, there may be 4 choices of LWAKE signal, i.e., active high, active low, positive (high) pulse, and negative (low) pulse. The output pulse width is about 150 ms. In CardBus mode applications, LWACT and LWPTN have no meaning.

The default value of each of these two bits is 0, i.e., the default output signal of the LWAKE pin is an active high signal.

<table>
<tr><th colspan="2" rowspan="2">LWAKE output</th><th colspan="2">LWACT</th></tr>
<tr><th>0</th><th>1</th></tr>
<tr><td rowspan="2">LWPTN</td><td>0</td><td>Active high*</td><td>Active low</td></tr>
<tr><td>1</td><td>Positive pulse</td><td>Negative pulse</td></tr>
</table>
* Default value.</td></tr>
<tr><td>3</td><td>R</td><td>MEMMAP</td><td>Memory Mapping: The operational registers are mapped into PCI memory space.</td></tr>
<tr><td>2</td><td>R</td><td>IOMAP</td><td>I/O Mapping: The operational registers are mapped into PCI I/O space.</td></tr>
<tr><td>1</td><td>R/W</td><td>VPD</td><td>Enable Vital Product Data: Set to 1 to enable vital product data. The VPD data is stored in 93C46 or 93C56 from within offset 40h-7Fh. If this bit is set, the New_Cap bit in RTL8139C(L)+'s PCI Configuration Space (Offset 06H) is set, and the VPD registers are from offset 60H to 67H in the PCI configuration space of the RTL8139C(L)+.</td></tr>
<tr><td>0</td><td>R/W</td><td>PMEn</td><td>Power Management Enable: Writable only when 93C46CR register EEM1=EEM0=1
Let A denote the New_Cap bit (bit 4 of the Status Register) in the PCI Configuration space offset 06H.

Let B denote the Cap_Ptr register in the PCI Configuration space offset 34H.

Let C denote the Cap_ID (power management) register in the PCI Configuration space offset 50H.

Let D denote the power management registers in the PCI Configuration space offset from 52H to 55H.

Let E denote the Next_Ptr (power management) register in the PCI Configuration space offset 51H.

PMEn setting:
- 0: A=B=C=E=0, D is invalid. (Assume VPD bit = 0)
- 1: A=1, B=50h, C=01h, D is valid, E is valid and depends on whether or not VPD is enabled.</td></tr>
</table>

6.13 Media Status Register (Offset 0058h, R/W)

This register allows configuration of a variety of device and PHY options, and provides PHY status information.

Bit	R/W	Symbol	Description
7	R/W	TXFCE/ LdTXFCE	**Tx Flow Control Enable:** The flow control is valid in full-duplex mode only. This register's default value comes from 93C46 (93C56). RTL8139C(L)+ / Remote / TXFCE/LdTXFCE ANE = 1 / NWAY FLY mode / R/O ANE = 1 / NWAY mode only / R/W ANE = 1 / No NWAY / R/W ANE = 0 & full-duplex mode / - / R/W ANE = 0 & half-duplex mode / - / invalid NWAY FLY mode: NWAY with flow control capability NWAY mode only: NWAY without flow control capability
6	R/W	RXFCE	**Rx Flow Control Enable:** The flow control is enabled in full-duplex mode only. The default value comes from 93C46 (93C56).
5	-	-	**Reserved**
4	R	Aux_Status	**Aux. Power Present Status:** The value of this bit is fixed after each PCI reset. 1: Aux. Power is present 0: Aux. Power is absent
3	R	SPEED_10	**Media Speed:** Set when current media is 10 Mbps mode. Reset when current media is 100 Mbps mode.
2	R	LINKB	**Inverse of Link Status:** 0: Link OK 1: Link Fail
1	R	TXPF	**Transmit Pause Flag:** Set when the RTL8139C(L)+ sends a pause packet. Reset when the RTL8139C(L)+ sends a timer done packet.
0	R	RXPF	**Receive Pause Flag:** Set when the RTL8139C(L)+ is in backoff state because a pause packet has been received. Reset when pause state is clear.

6.14 Configuration Register3 (CONFIG 3) (Offset 0059h, R/W)

Bit	R/W	Symbol	Description
7	R	GNTSel	**Grant Select:** Select the Frame's asserted time after the Grant signal has been asserted. The Frame and Grant are the PCI signals. 0: No delay 1: Delay one clock from GNT assertion
6	R/W	PARM_En	**Parameter Enable:** (These parameters are used in 100Mbps mode.) Setting to 0 and 9346CR register EEM1=EEM0=1 enable the PHY1_PARM, PHY2_PARM, TW_PARM be written via software. Setting to 1 will allow parameters to be auto-loaded from the 93C46 (93C56) and disable writing to the PHY1_PARM, PHY2_PARM and TW_PARM registers via software. The PHY1_PARM, PHY2_PARM, and TW_PARM can be auto-loaded from EEPROM in this mode. The parameter auto-load process is executed every time when the Link is working properly in 100Mbps mode.
5	R/W	Magic	**Magic Packet:** This bit is valid when the PWEn bit of CONFIG1 register is set. The RTL8139C(L)+ will assert the PMEB signal to wakeup the operating system when the Magic Packet is received. Once the RTL8139C(L)+ has been enabled for Magic Packet wakeup and has been put into an adequate state, it scans all incoming packets addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame. A Magic Packet frame must also meet the basic requirements: Destination address + Source address + data + CRC The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address. The specific sequence consists of 16 duplications of 6 byte ID registers, with no breaks or interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE address match the address of the ID registers. If the Node ID is 11h 22h 33h 44h 55h 66h, then the format of the magic frame format is as follows: Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC
4	R/W	LinkUp	**Link Up:** This bit is valid when the PWEn bit of the CONFIG1 register is set. The RTL8139C(L)+, in adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is re-established.

3	R	CardB_En	**Card Bus Enable:** Set to 1 to enable CardBus related registers and functions. Set to 0 to disable CardBus related registers and functions.
2	R	CLKRUN_En	**CLKRUN Enable:** Set to 1 to enable CLKRUN. Set to 0 to disable CLKRUN.
1	R	FuncRegEn	**Functions Registers Enable**: CardBus only Set to 1 to enable the 4 Function Registers (Function Event Register, Function Event Mask Register, Function Present State Register, and Function Force Event Register) for CardBus application. Set to 0 to disable the 4 Function Registers for CardBus application.
0	R	FBtBEn	**Fast Back to Back Enable:** Set to 1 to enable Fast Back to Back.

6.15 Configuration Register4 (CONFIG 4) (Offset 005Ah, R/W)

Bit	R/W	Symbol	Description
7	R/W	RxFIFOAutoClr	**Clear Rx FIFO Overflow:** Set to 1, the RTL8139C(L)+ will clear Rx FIFO overflow automatically.
6	R/W	AnaOff	**Analog Power Off:** This bit can not be auto-loaded from EEPROM (9346 or 9356). 0: Normal working state. This is also the power-on default value. 1: Turn off the analog power of the RTL8139C(L)+ internally.
5	R/W	LongWF	**Long Wake-up Frame:** The initial power-on value is 0. This bit does not participate in EEPROM autoload, and PCI RST# has no effect to this bit. 0: The RTL8139C(L)+ supports up to 8 wake-up frames, each with masked bytes selected from offset 12 to 75. 1: The RTL8139C(L)+ supports up to 5 wake-up frames, each with 16-bit CRC algorithm for MS Wakeup Frame, the low byte of 16-bit CRC should be placed at the corresponding CRC register, and the high byte of the 16-bit CRC should be placed at the corresponding LSBCRC register. Wake-up frames 0 and 1 are the same as above, except that the masked bytes start from offset 0 to 63. Wake-up frames 2 and 3 are merged into one long wake-up frame with masked bytes selected from offset 0 to 127. Wake-up frames 4 & 5 and 6 & 7 are merged respectively into two other long wake-up frames. Please refer to 7.4 PCI Power Management functions for a detailed description.
4	R/W	LWPME	**LANWAKE vs PMEB:** 0: The LWAKE and PMEB are asserted at the same time. 1: The LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low. In CardBus applications, this bit has no meaning.
3	-	-	**Reserved**
2	R/W	LWPTN	**LWAKE Pattern:** Please refer to LWACT bit in the CONFIG1 register.
1	-	-	**Reserved**
0	R/W	PBWakeup	**Pre-Boot Wakeup:** The initial value comes from the EEPROM autoload. 0: Pre-Boot Wakeup enabled 1: Pre-Boot Wakeup disabled (suitable for CardBus and MiniPCI application.)

6.16 Multiple Interrupt Select Register (Offset 005Ch-005Dh, R/W)

If the received packet data is not the familiar protocol (IPX, IP, NDIS, etc.) to RTL8139C(L)+, RCR<ERTH[3:0]> will not be used to transfer data in early mode. This register will be written to the received data length in order to make early Rx interrupt for the unfamiliar protocol.

Bit	R/W	Symbol	Description
15-12	-	-	**Reserved**
11-0	R/W	MISR11-0	**Multiple Interrupt Select:** Indicates that the RTL8139C(L)+ makes an rx interrupt after RTL8139C(L)+ has transferred the byte data into the system memory. If the value of these bits is zero, there will be no early interrupt as soon as the RTL8139C(L)+ prepares to execute the first PCI transaction of the received data. Bit1, 0 must be zero. The ERTH3-0 bits should not be set to 0 when the multiple interrupt select register is used.

- The above is true when MulERINT=0 (bit17, RCR). When MulERINT=1, any received packet invokes early interrupt according to MISR[11:0] setting in early mode.
- In C+ mode, all packets are unfamiliar packets.

6.17 PCI Revision ID (Offset 005Eh, R)

Bit	R/W	Symbol	Description
7-0	R	Revision ID	The value in PCI Configuration Space offset 08h is 10h.

6.18 Transmit Status of All Descriptors Register (TSAD) (Offset 0060h-0061h, R/W, C mode only)

Bit	R/W	Symbol	Description
15	R	TOK3	**TOK bit of Descriptor 3**
14	R	TOK2	**TOK bit of Descriptor 2**
13	R	TOK1	**TOK bit of Descriptor 1**
12	R	TOK0	**TOK bit of Descriptor 0**
11	R	TUN3	**TUN bit of Descriptor 3**
10	R	TUN2	**TUN bit of Descriptor 2**
9	R	TUN1	**TUN bit of Descriptor 1**
8	R	TUN0	**TUN bit of Descriptor 0**
7	R	TABT3	**TABT bit of Descriptor 3**
6	R	TABT2	**TABT bit of Descriptor 2**
5	R	TABT1	**TABT bit of Descriptor 1**
4	R	TABT0	**TABT bit of Descriptor 0**
3	R	OWN3	**OWN bit of Descriptor 3**
2	R	OWN2	**OWN bit of Descriptor 2**
1	R	OWN1	**OWN bit of Descriptor 1**
0	R	OWN0	**OWN bit of Descriptor 0**

6.19 Basic Mode Control Register (Offset 0062h-0063h, R/W)

Bit	Name	Description/Usage	Default/Attribute
15	Reset	This bit sets the status and control registers of the PHY (register 0062-0074H) in a default state. This bit is self-clearing. 1: Software reset 0: Normal operation	0, RW
14	-	Reserved	-
13	Spd_Set	This bit sets the network speed in UTP mode. This bit's initial value comes from 93C46 (93C56). 1: 100Mbps 0: 10Mbps	0, RW
12	Auto Negotiation Enable (ANE)	This bit enables/disables the N-Way auto-negotiation function in UTP mode. When set to 1 to enable auto-negotiation, bit13 will be ignored. Set to 0 disables auto-negotiation, and bits 13 and 8 will determine the link speed and the data transfer mode, respectively. This bit's initial value comes from 93C46 (93C56).	0, RW
11	MLinkP	The initial value comes from EEPROM. 1: MLINK pin = high ⇔ MII link OK 0: MLINK pin = low ⇔ MII link OK	0, R
10	MFDupP	The initial value comes from EEPROM. 1: MFDUP pin = high ⇔ MII interface is in full duplex mode 0: MFDUP pin = low ⇔ MII interface is in full duplex mode	0, R
9	Restart Auto Negotiation	This bit allows the NWay auto-negotiation function to be reset in UTP mode. 1: Re-start auto-negotiation 0: Normal operation	0, RW
8	Duplex Mode	In UTP mode: This bit sets the duplex mode. 1 = full-duplex; 0 = normal operation. This bit's initial value comes from 93C46 (93C56). If bit12 = 1, read = status write = register value. If bit12=1, ie the chip is in N-Way mode, and the link partner is in N-Way mode as well, then this bit is a read-only status bit showing N-Way results. Else, this bit is a command bit to force the chip to run in either full-duplex or half duplex mode. If bit12 = 0, read = write = register value. In MII mode (Read only): This bit is a status bit, indicating either the external PHY chip is in full-duplex mode or half-duplex mode. 1: Indicating that the external PHY is in full-duplex mode. 0: Indicating that the external PHY is in half-duplex mode.	0, RW
7-0	-	Reserved	-

6.20 Basic Mode Status Register (Offset 0064h-0065h, R)

<table>
<tr><th>Bit</th><th>Name</th><th>Description/Usage</th><th>Default/Attribute</th></tr>
<tr><td>15</td><td>100Base-T4</td><td>1: Enable 100Base-T4 support
0: Suppress 100Base-T4 support.</td><td>0, RO</td></tr>
<tr><td>14</td><td>100Base_TX_ FD</td><td>1: Enable 100Base-TX full duplex support
0: Suppress 100Base-TX full duplex support</td><td>1, RO</td></tr>
<tr><td>13</td><td>100BASE_TX_HD</td><td>1: Enable 100Base-TX half-duplex support
0: Suppress 100Base-TX half-duplex support</td><td>1, RO</td></tr>
<tr><td>12</td><td>10Base_T_FD</td><td>1: Enable 10Base-T full duplex support
0: Suppress 10Base-T full duplex support</td><td>1, RO</td></tr>
<tr><td>11</td><td>10_Base_T_HD</td><td>1: Enable 10Base-T half-duplex support
0: Suppress 10Base-T half-duplex support</td><td>1, RO</td></tr>
<tr><td>10-8</td><td>-</td><td>Reserved</td><td>-</td></tr>
<tr><td>7-6</td><td>Medium1, Medium0</td><td>These two bits are used to select medium mode. The initial values of these 2 bits come from EEPROM autoload.
<table>
<tr><td colspan="2" rowspan="2">Medium Mode</td><td colspan="2">Medium0</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td rowspan="2">Medium1</td><td>0</td><td>AutoDetect</td><td>UTP</td></tr>
<tr><td>1</td><td>MII</td><td>X</td></tr>
</table>
In AutoDetect mode, the priority is UTP > MII.</td><td>(Medium1, Medium0) = (0,0), R/W</td></tr>
<tr><td>5</td><td>Auto Negotiation Complete</td><td>1: Auto-negotiation process completed
0: Auto-negotiation process not completed</td><td>0, RO</td></tr>
<tr><td>4</td><td>Remote Fault</td><td>1: Remote fault condition detected (cleared on read)
0: No remote fault condition detected</td><td>0, RO</td></tr>
<tr><td>3</td><td>Auto Negotiation</td><td>1: Link had not been experienced fail state
0: Link had been experienced fail state</td><td>1, RO</td></tr>
<tr><td>2</td><td>Link Status</td><td>1: Valid link established
0: No valid link established</td><td>0, RO</td></tr>
<tr><td>1</td><td>Jabber Detect</td><td>1: Jabber condition detected
0: No jabber condition detected</td><td>0, RO</td></tr>
<tr><td>0</td><td>Extended Capability</td><td>1: Extended register capability
0: Basic register capability only</td><td>1, RO</td></tr>
</table>

This register indicates RTL8139C(L)+'s internal PHYceiver status, and medium mode.

6.21 Auto-negotiation Advertisement Register (Offset 0066h-0067h, R/W)

Bit	Name	Description/Usage	Default/Attribute
15	NP	Next Page bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	0, RO
14	ACK	1: Acknowledge reception of link partner capability data word	0, RO
13	RF	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	0, RW
12-11	-	Reserved	-
10	Pause	1: flow control is supported by local node 0: flow control is not supported by local mode	The default value comes from EEPROM, RO
9	T4	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node	0, RO
8	TXFD	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node	1, RW
7	TX	1: 100Base-TX is supported by local node 0: 100Base-TX not supported by local node	1, RW
6	10FD	1: 10Base-T full duplex supported by local node 0: 10Base-T full duplex not supported by local node	1, RW
5	10	1: 10Base-T is supported by local node 0: 10Base-T not supported by local node	1, RW
4-0	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD <00001> is specified. No other protocols are supported.	<00001>, RW

- This register indicates Nway advertisement info of RTL8139C(L)+'s internal PHYceiver.

6.22 Auto-Negotiation Link Partner Ability Register (Offset 0068h-0069h, R)

Bit	Name	Description/Usage	Default/Attribute
15	NP	Next Page bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	0, RO
14	ACK	1: Link partner acknowledges reception of local node's capability data word.	0, RO
13	RF	1: Link partner is indicating a remote fault	0, RO
12-11	-	Reserved	-
10	Pause	1: Flow control is supported by link partner 0: Flow control is not supported by link partner	0, RO
9	T4	1: 100Base-T4 is supported by link partner 0: 100Base-T4 not supported by link partner	0, RO
8	TXFD	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner	0, RO
7	TX	1: 100Base-TX is supported by link partner 0: 100Base-TX not supported by link partner	0, RO
6	10FD	1: 10Base-T full duplex is supported by link partner 0: 10Base-T full duplex not supported by link partner	0, RO
5	10	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner	0, RO
4-0	Selector	Link Partner's binary encoded node selector. Currently only CSMA/CD <00001> is specified.	<00000>, RO

When current medium mode is at UTP, this register shows the Nway Link partner's ability.

6.23 Auto-negotiation Expansion Register (Offset 006Ah-006Bh, R)

This register contains additional status of internal PHYceiver for NWay auto-negotiation.

Bit	Name	Description/Usage	Default/Attribute
15-5	-	Reserved, This bit is always set to 0.	-
4	MLF	Status indicating if a multiple link fault has occurred. 1: Fault occurred 0: No fault occurred.	0, RO
3	LP_NP_ABLE	Status indicating if the link partner supports Next Page negotiation. 1: Supported 0: Not supported.	0, RO
2	NP_ABLE	This bit indicates if the local node is able to send additional Next Pages.	0, RO
1	PAGE_RX	This bit is set when a new Link Code Word Page has been received. The bit is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.	0, RO
0	LP_NW_ABLE	1: Link partner supports N-Way auto-negotiation.	0, RO

6.24 Disconnect Counter (Offset 006Ch-006Dh, R)

This register is valid only when in UTP mode.

Bit	Name	Description/Usage	Default/Attribute
15-0	DCNT	This 16-bit counter increments by 1 for every disconnect event. It rolls over when becomes full. It is cleared to zero by a read command.	h'[0000], R

6.25 False Carrier Sense Counter (Offset 006Eh-006Fh, R)

This counter provides information required to implement the "False Carriers" attribute within the MAU managed object class of Clause 30 of the IEEE 802.3u specification. This register is valid only when in UTP mode.

Bit	Name	Description/Usage	Default/Attribute
15-0	FCSCNT	This 16-bit counter increments by 1 for each false carrier event. It is cleared to zero by a read command.	h'[0000], R

6.26 NWay Test Register (Offset 0070h-0071h, R/W)

This register is valid only when in UTP mode.

Bit	Name	Description/Usage	Default/Attribute
15-8	-	Reserved	-
7	NWLPBK	1: Set NWay to loopback mode.	0, RW
6-4	-	Reserved	-
3	ENNWLE	1: LED0 Pin indicates linkpulse	0, RW
2	FLAGABD	1: Auto-neg experienced ability detect state	0, RO
1	FLAGPDF	1: Auto-neg experienced parallel detection fault state	0, RO
0	FLAGLSC	1: Auto-neg experienced link status check state	0, RO

6.27 RX_ER Counter (Offset 0072h-0073h, R)

This register is valid only when in UTP mode.

Bit	Name	Description/Usage	Default/Attribute
15-0	RXERCNT	This 16-bit counter increments by 1 for each valid packet received. It is cleared to zero by a read command.	h'[0000], R

6.28 CS Configuration Register (Offset 0074h-0075h, R/W)

This register is valid only when in UTP mode.

Bit	Name	Description/Usage	Default/Attribute
15	Testfun	1: Auto-neg speeds up internal timer	0,WO
14-10	-	Reserved	-
9	LD	Active low TPI link disable signal. When low, TPI still transmits link pulses and TPI stays in good link state.	1, RW
8	HEART BEAT	The HEART BEAT function is only valid in 10Mbps mode. 1: HEART BEAT enable 0: HEART BEAT disable.	1, RW
7	JBEN	1: Enable jabber function 0: Disable jabber function	1, RW
6	F_LINK_100	Used to login force good link in 100Mbps for diagnostic purposes. 1: DISABLE 0: ENABLE.	1, RW
5	F_Connect	Assertion of this bit forces the disconnect function to be bypassed.	0, RW
4	-	Reserved	-
3	Con_status	This bit indicates the status of the connection. 1: Valid connected link detected 0: Disconnected link detected	0, RO
2	Con_status_En	Assertion of this bit configures LED1 pin to indicate connection status.	0, RW
1	-	Reserved	-
0	PASS_SCR	Bypass Scramble	0, RW

6.29 Low Address of a Tx Descriptor with Tx DMA Ok (Offset 0082h-0083h, R)

Bit	R/W	Symbol	Description
15-0	R	_TDOKLAddr	This is a 16-bit address indicating the low part address of a Tx descriptor that has already asserted an interrupt of Tx DMA complete.

6.30 Flash Memory Read/Write Register (FLASH) (Offset 00D4h-00D7h, R/W)

Bit	R/W	Symbol	Description
31-24	R/W	MD7-MD0	**Flash Memory Data Bus:** These bits set and reflect the state of the MD7 - MD0 pins, during write and read process respectively.
23-21	-	-	**Reserved**
20	W	ROMCSB	**Chip Select:** This bit sets the state of the ROMCSB pin.
19	W	OEB	**Output Enable:** This bit sets the state of the OEB pin.
18	W	WEB	**Write Enable:** This bit sets the state of the WEB pin.
17	W	SWRWEn	**Enable software access to flash memory:** 0: Disable read/write access to flash memory via software 1: Enable read/write access to flash memory via software and disable the EEPROM access during flash memory access via software
16-0	W	MA16-MA0	**Flash Memory Address Bus:** These bits set the state of the MA16-0 pins.

6.31 Configuration Register 5 (Config5) (Offset 00D8h, R/W)

This register, unlike other Config registers, is not protected by 93C46 Command register. Therefore, there is no need to enable Config register write prior to writing to Config5.

Bit	R/W	Symbol	Description
7	-	-	**Reserved**
6	R/W	BWF	**Broadcast Wakeup Frame:** 0: Disable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF. 1: Enable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF. The power-on default value of this bit is 0.
5	R/W	MWF	**Multicast Wakeup Frame:** 0: Disable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address. 1: Enable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address. The power-on default value of this bit is 0.
4	R/W	UWF	**Unicast Wakeup Frame:** 0: Disable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address. 1: Enable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address. The power-on default value of this bit is 0.
3	R/W	FIFOAddrPtr	**FIFO Address Pointer:** (Realtek internal use only to test FIFO SRAM) 0: Both Rx and Tx FIFO address pointers are updated in ascending way from 0 and upwards. The initial FIFO address pointer is 0. 1: Both Rx and Tx FIFO address pointers are updated in a descending method from 1FFh and downwards. The initial FIFO address pointer is 1FFh. This bit does not participate in the EEPROM auto-load. The FIFO address pointers can not be reset, except initial power-on. The power-on default value of this bit is 0.
2	R/W	LDPS	**Link Down Power Saving mode:** 1: Disable. 0: Enable. When cable is disconnected (Link Down), the analog part will power down itself (PHY Tx part & part of twister) automatically except PHY Rx part and part of twister to monitor SD signal in case that cable is re-connected and Link should be established again.
1	R/W	LANWake	**LANWake Signal Enable/Disable:** 1: Enable LANWake signal 0: Disable LANWake signal
0	R/W	PME_STS	**PME_Status Bit:** Always sticky; can be reset by PCI RST# and software. 1: The PME_Status bit can be reset by PCI reset or by software. 0: The PME_Status bit can only be reset by software.

- Config5 register, offset D8h: (SYM_ERR register is changed to Config5, the function of SYM_ERR register is no longer supported by RTL8139C.)
- The 3 bits (bit2-0) are auto-loaded from EEPROM Config5 byte to RTL8139C Config5 register.

6.32 Transmit Priority Polling Register (TPPoll) (Offset 00D9h, R/W, C+ mode only)

Bit	R/W	Symbol	Description
7	W	HPQ	**High Priority Queue Polling:** i. Write a 1 to this bit by software to notify the RTL8139C(L)+ that there is high priority packet(s) waiting to be transmitted. ii. The RTL8139C(L)+ will clear this bit automatically after all high priority packets have been transmitted. iii. Writing 0 to this bit has no effect.
6	W	NPQ	**Normal Priority Queue Polling:** i. Write a 1 to this bit by software to notify the RTL8139C(L)+ that there is a normal priority packet(s) waiting to be transmitted. ii. The RTL8139C(L)+ will clear this bit automatically after all normal priority packets have been transmitted. iii. Writing 0 to this bit has no effect.
5-1	-	-	**Reserved**
0	W	FSWInt	**Forced Software Interrupt:** i. Writing a 1 to this bit will trigger an interrupt, and the _SWInt bit (bit8, ISR, offset3Eh-3Fh) will set. ii. The RTL8139C(L)+ will clear this bit automatically after the _SWInt bit (bit8, ISR) is cleared. iii. Writing 0 to this bit has no effect.

6.33 C+ Command Register (C+CR) (Offset 00E0h-00E1h, R/W, C+ mode only)

This register is the key to entering C+ mode operation before configuring other C+ mode registers and descriptors. This register is word access only, byte access to this register has no effect.

Recommendation to C+ mode programming: Enable C+ mode functions in C+CR register first, => Enable transmit/receive in Command register (offset 37h), => Configure other related registers (ex. Descriptor start address, TCR, RCR, …).

Bit	R/W	Symbol	Description
15-9	-	-	**Reserved**
8	-	-	**Reserved** (Home LAN Enable, always 0)
7	-	-	**Reserved**
6	R/W	RxVLAN	**Receive VLAN De-tagging Enable:** (In C+ mode) 1: Enable; 0: Disable
5	R/W	RxChkSum	**Receive Checksum Offload Enable:** (In C+ mode) 1: Enable; 0: Disable
4	R/W	DAC	**PCI Dual Address Cycle Enable:** (In C+ mode) 1: Enable; 0: Disable When set, the RTL8139C(L)+ will perform Tx/Rx DMA using PCI Dual Address Cycle only when the High 32-bit buffer address is not equal to 0.
3	R/W	MulRW	**PCI Multiple Read/Write Enable:** (In C+ mode) 1: Enable; 0: Disable
2	-	-	-
1	R/W	C+Rx	Receive Enable: (In C+ mode) 1: Enable; 0: Disable
0	R/W	C+Tx	Transmit Enable: (In C+ mode) 1: Enable; 0: Disable

6.34 Receive Descriptor Start Address Register (RDSAR) (Offset 00E4h-00EBh, R/W, C+ mode only)

Bit	R/W	Symbol	Description
63-0	R/W	RDSA	**Receive Descriptor Start Address:** (64-bit address) Bit[31:0]: Offset E7h-E4h, low 32-bit address. Bit[63:32]: Offset EBh-E8h, high 32-bit address.

6.35 Early Transmit Threshold Register (ETThR) (Offset 00ECh, R/W, C+ mode only)

Bit	R/W	Symbol	Description
7-6	R/W	TestMode	**Test Mode:** For RTL8139C(L)+ to operate normally, please set to "Normal" mode. The Test1-3 modes are for testing only.
5-0	R/W	ETTh	**Early Tx Threshold:** 1. Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet) the RTL8139C(L)+ will transmit this packet. 000000 = 8 bytes 2. These fields count from 000001 to 111111 in unit of 32 bytes. 3. This threshold must be avoided from exceeding 2K byte.

Bit[7:6]	Mode	Description
(0,0)	Normal	RTL8139C(L)+ operation mode
(0,1)	Test1	Test mode 1: To test waveform's rise time and fall time.
(1,0)	Test2	Test mode 2: Internal test signals output from Boot ROM interface.
(1,1)	Test3	Test mode 3: Receive signals output from Boot ROM interface.

6.36 Function Event Register (Offset 00F0h-00F3h, R/W)

Bit	R/W	Symbol	Description
31-16	-	-	**Reserved**
15	R/W	INTR	**Interrupt:** Set to 1 when INTR field in the Function Force Event Register is set. Writing a 1 may clear this bit. Writing a 0 has no effect. This bit must not be affected by RST# pin and software reset.
14-5	-	-	**Reserved**
4	R/W	GWAKE	**General Wakeup:** Set to 1 when the GWAKE field in the Function Present State Register changes its state from 0 to 1. This bit can also be set when the GWAKE bit of the Function Force Register is set. Writing a 1 may clear this bit. Writing a 0 has no effect. This bit can not be affected by the RST#.
3-0	-	-	**Reserved**

- This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).
- The Function Event (Offset F0h), Function Event Mask (Offset F4h), Function Present State (Offset F8h), and Function Force Event (Offset FCh) registers have some corresponding fields with the same names. The GWAKE and INTR bits of these registers reflect the wake-up event signaled on the SCTCSCHG pin. The operation of CSTCSCHG pin is similar to PME# pin except that the CSTCSCHG pin is asserted high.

6.37 Function Event Mask Register (Offset 00F4h-00F7h, R/W)

Bit	R/W	Symbol	Description
31-16	-	-	**Reserved**
15	R/W	INTR	**Interrupt Mask:** When cleared (0), setting of the INTR bit in either the Function Present State Register or the Function Event Register will neither cause assertion of the INT# signal while the CardBus PC Card interface is powered up, nor cause a system Wakeup (CSTSCHG) while the interface is powered off. Setting this bit to 1 enables the INTR bit in both the Function Present State Register and the Function Event Register to generate the INT# signal (and the system Wakeup if the corresponding WKUP field in this Function Event Mask Register is also set). This bit is not affected by RST#.
14	R/W	WKUP	**Wakeup Mask:** When cleared (0), the Wakeup function is disabled, i.e., the setting of this bit in the Function Event Register will not assert the CSTSCHG signal. Setting this bit to 1 enables the fields in the Function Event Register to assert the CSTSCHG signal. This bit is not affected by RST#.
13-5	-	-	**Reserved**
4	R/W	GWAKE	**General Wakeup Mask:** When cleared (0), setting this bit in the Function Event Register will not cause the CSTSCHG pin to assert. Setting this bit to 1 enables the GWAKE field in the Function Event Register to assert CSTSCHG pin if bit14 of this register is also set. This bit is not affected by RST#.
3-0	-	-	**Reserved**

- This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).

6.38 Function Present State Register (Offset 00F8h-00FBh, R)

Bit	R/W	Symbol	Description
31-16	-	-	**Reserved**
15	R	INTR	**Interrupt:** This bit is set when one of the ISR register bits has been set to 1 and remains set (1), until all of the ISR register bits have been cleared. It is not affected by RST#.
14-5	-	-	**Reserved**
4	R	GWAKE	**General Wakeup:** This bit reflects the current state of the Wakeup event(s), and is just like the PME_Status bit of the PMCSR register. This bit remains set (1) until the PME_Status bit of the PMCSR register is cleared. It is not affected by RST#.
3-0	-	-	**Reserved**

- This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).
- This read-only register reflects the current state of the function.

6.39 Function Force Event Register/MII Register (Offset 00FCh-00FFh, W)/(Offset 00FCh, R/W)

Bit	R/W	Symbol	Description
31	R	MII	1: The RTL8139C(L)+ processes current network traffic through its external MII interface. 0: The RTL8139C(L)+ processes current network traffic through its UTP interface (via its embedded phyceiver).
30	R	UTP	1: The RTL8139C(L)+ processes current network traffic through its UTP interface (via its embedded phyceiver). 0: The RTL8139C(L)+ processes current network traffic through its external MII interface.
29-28	-	-	**Reserved**
27	R/W	MDM	**Management Data Mode:** Setting this bit indicates that the MDIO pin is output, and the state of the MDIO pin reflects with the MDO bit. When this pin is reset, the MDIO pin is input. The MDI bit reflects the state of the MDIO pin. The default value is "0".
26	R/W	MDO	**MII Management Data-OUT:** Used by the RTL8139C+ to write data to the MDIO pin.
25	R/W	MDI	**MII Management Data-IN:** Used by the RTL8139C+ to read data from the MDIO pin.
24	R/W	MDC	**Management Data Clock:** This bit reflects the state of the MDC pin.
23-16	-	-	**Reserved**
15	W	INTR	**Interrupt:** Writing a 1 sets the INTR bit in the Function Event Register. However, the INTR bit in the Function Present State Register is not affected and continues to reflect the current state of the ISR register. Writing a 0 to this bit has no effect.
14-5	-	-	**Reserved**
4	W	GWAKE	**General Wakeup:** Setting this bit to 1, sets the GWAKE bit in the Function Event Register. However, the GWAKE bit in the Function Present State Register is not affected and continues to reflect the current state of the Wakeup request. Writing a 0 to this bit has no effect.
3-0	-	-	**Reserved**

- This register (except bits 31-30, and bits 27-24) is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3). The bit31-30, and bit27-24 are valid only when FuncRegEn=0 (bit1, Config3).
- MII Register is valid (i.e. bits 31, 30, 27-24, are valid) only when current Medium select is set to Auto-Dectect or MII mode.
- Bit7, and bit6 indicate current network traffic path that the RTL8139C(L)+ uses. When FuncRegEn=1 (bit1, Config3) in CardBus mode, these 2 bits are reserved bits.
- Bits 3-0 provide a path for software to access the MII registers of an external PHYceiver. When FuncRegEn=1 (bit1, Config3) in CardBus mode, these 4 bits are reserved bits.

7. EEPROM Contents (93C46 or 93C56)

The 93C46 is a 1K-bit EEPROM (the 93C56 is a 2K-bit EEPROM). Although it is actually addressed by words, its contents are listed below by bytes for convenience. After the valid duration of the RSTB pin or auto-load command in 9346CR, the RTL8139C(L) performs a series of EEPROM read operations from the 93C46 (93C56) address 00H to 31H.

- It is suggested to obtain Realtek approval before changing the default settings of the EEPROM.

<table>
<tr><th>Bytes</th><th>Contents</th><th>Description</th></tr>
<tr><td>00h
01h</td><td>29h
81h</td><td>These 2 bytes contain the ID code word for the RTL8139C(L)+. The RTL8139C(L)+ will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct, otherwise, the Vendor ID and Device ID of the PCI configuration space are hex 10EC and 8129 respectively.</td></tr>
<tr><td>02h-03h</td><td>VID</td><td>PCI Vendor ID, PCI configuration space offset 00h-01h.</td></tr>
<tr><td>04h-05h</td><td>DID</td><td>PCI Device ID, PCI configuration space offset 02h-03h.</td></tr>
<tr><td>06h-07h</td><td>SVID</td><td>PCI Subsystem Vendor ID, PCI configuration space offset 2Ch-2Dh.</td></tr>
<tr><td>08h-09h</td><td>SMID</td><td>PCI Subsystem ID, PCI configuration space offset 2Eh-2Fh.</td></tr>
<tr><td>0Ah</td><td>MNGNT</td><td>PCI Minimum Grant Timer, PCI configuration space offset 3Eh.</td></tr>
<tr><td>0Bh</td><td>MXLAT</td><td>PCI Maximum Latency Timer, PCI configuration space offset 3Fh.</td></tr>
<tr><td>0Ch</td><td>MSRBMCR</td><td>Bits 7-6 map to bits 7-6 of the Media Status register (MSR), Bits 5, 4, 3, 2, 0 map to bits 13, 12, 8, 3, 2 of the Basic Mode Control register (BMCR). If the network speed is set to Auto-Detect mode (i.e. Nway mode), then Bit 1=0 means the local RTL8139C(L)+ supports flow control (IEEE 802.3x). In this case, Bit 10=1 in Auto-negotiation Advertisement Register (offset 66h-67h).

Bit 1=1 means the local RTL8139C(L)+ does not support flow control. In this case, Bit 10=0 in Auto-negotiation Advertisement. This is because that there are Nway switch hubs which keep sending flow control pause packets for no reason, if the link partner supports Nway flow control.
<table>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Load-to</td><td>TXFCE/LdTXFCE (bit7, MSR)</td><td>RXFCE (bit6, MSR)</td><td>Spd_Set (bit13, BMCR)</td><td>ANE (bit12, BMCR)</td><td>MLinkP (bit3, BMCR)</td><td>MFdupP (bit2, BMCR)</td><td>-</td><td>Duplex Mode (bit8, BMCR)</td></tr>
</table>
</td></tr>
<tr><td>0Dh</td><td>CONFIG3</td><td>RTL8139C(L)+ Configuration register 3, operational register offset 59H.</td></tr>
<tr><td>0Eh-13h</td><td>Ethernet ID</td><td>After auto-load command or hardware reset, the RTL8139C(L)+ loads the Ethernet ID to IDR0-IDR5 of the RTL8139C(L)+'s I/O registers.</td></tr>
<tr><td>14h</td><td>CONFIG0</td><td>RTL8139C(L)+ Configuration register 0, operational registers offset 51h.</td></tr>
<tr><td>15h</td><td>CONFIG1</td><td>RTL8139C(L)+ Configuration register 1, operational registers offset 52h.</td></tr>
<tr><td>16h-17h</td><td>PMC</td><td>Reserved. Do not change this field without Realtek approval.
Power Management Capabilities. PCI configuration space address 52h and 53h.</td></tr>
<tr><td>18h</td><td>-</td><td>Reserved</td></tr>
<tr><td>19h</td><td>CONFIG4</td><td>Reserved. Do not change this field without Realtek approval.
RTL8139C(L)+ Configuration register 4, operational registers offset 5Ah.</td></tr>
<tr><td>1Ah-1Dh</td><td>PHY1_PARM_U</td><td>Reserved. Do not change this field without Realtek approval.
PHY Parameter 1-U for RTL8139C. Operational registers of the RTL8139C(L)+ are from 78h to 7Bh.</td></tr>
<tr><td>1Eh</td><td>PHY2_PARM_U</td><td>Reserved. Do not change this field without Realtek approval.
PHY Parameter 2-U for RTL8139C. Operational register of the RTL8139C(L)+ is 80h.</td></tr>
</table>

1Fh	CONFIG_5	Do not change this field without Realtek approval. Bit5, 3: Reserved. Bit7: Medium1 at BMSR. Medium select bit1. Bit6: Medium0 at BMSR. Medium select bit0. Bit5: PCI multi-function enable. Set to 1: Enable PCI multi-function capability. The RTL8139C+ can be a multi-function device with an external PCI device at slave mode on the same PCB, ex. an external software modem. Set to 0: Disable PCI multi-function capability. Bit4: Reserved Bit2: Link Down Power Saving mode: Set to 1: Disable. Set to 0: Enable. When cable is disconnected(Link Down), the analog part will power down itself (PHY Tx part & part of twister) automatically except PHY Rx part and part of twister to monitor SD signal in case that cable is re-connected and Link should be established again. Bit1: LANWake signal Enable/Disable Set to 1: Enable LANWake signal. Set to 0: Disable LANWake signal. Bit0: PME_Status bit property Set to 1: The PME_Status bit can be reset by PCI reset or by software if D3cold_support_PME is 0. If D3cold_support_PME=1, the PME_Status bit is a sticky bit. Set to 0: The PME_Status bit is always a sticky bit and can only be reset by software.
20h-23h	TW_PARM_U	Reserved. Do not change this field without Realtek approval. Twister Parameter U for RTL8139C. Operational registers of the RTL8139C(L)+ are 7Ch-7Fh.
24h-27h	TW_PARM_T	Reserved. Do not change this field without Realtek approval. Twister Parameter T for RTL8139C. Operational registers of the RTL8139C(L)+ are 7Ch-7Fh.
28h-2Bh	PHY1_PARM_T	Reserved. Do not change this field without Realtek approval. PHY Parameter 1-T for RTL8139C. Operational registers of the RTL8139C(L)+ are from 78h to 7Bh.
2Ch	PHY2_PARM_T	Reserved. Do not change this field without Realtek approval. PHY Parameter 2-T for RTL8139C. Operational register of the RTL8139C(L)+ is 80h.
2Dh-2Fh	-	Reserved.
30h-31h	CISPointer	Reserved. Do not change this field without Realtek approval. CIS Pointer.
32h-33h	CheckSum	Reserved. Do not change this field without Realtek approval. Checksum of the EEPROM content.
34h-3Eh	-	Reserved. Do not change this field without Realtek approval.
3Fh	PXE_Para	Reserved. Do not change this field without Realtek approval. PXE ROM code parameter.
40h-7Fh	VPD_Data	VPD data field. Offset 40h is the start address of the VPD data.
80h-FFh	CIS_Data	CIS data field. Offset 80h is the start address of the CIS data. (93C56 only).

7.1 Summary of EEPROM Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0 – IDR5	R/W*								
51h	CONFIG0	R		-	-	-	-	BS2	BS1	BS0
		W*	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	DVRLOAD	LWACT	MEMMAP	IOMAP	VPD	PMEN
		W*	LEDS1	LEDS0	DVRLOAD	LWACT	-	-	VPD	PMEN
58h	MSRBMCR	R	TxFCE	RxFCE	-	-	-	-		
		W*	TxFCE	RxFCE	-	-	-	-		
63H		R	-	-	Spd_Set	ANE	-	-	-	FUDUP
		W*	-	-	Spd_Set	ANE	-	-	-	FUDUP
59h	CONFIG3	R	GNTDel	PARM_EN	Magic	LinkUp	CardB_En	CLKRUN_En	FuncRegEn	FBtBEn
		W*	-	PARM_EN	Magic	LinkUp	-	-	-	-
5Ah	CONFIG4	R/W*	RxFIFO AutoClr	-	-	LWPME	-	LWPTN	-	-
78h-7Bh	PHY1_PARM	R/W**	32 bit Read Write							
7Ch-7Fh	TW1_PARM TW2_PARM	R/W**	32 bit Read Write 32 bit Read Write							
80h	PHY2_PARM	R/W**	8 bit Read Write							
D8h	CONFIG5	R/W*	-	-	-	-	-	LDPS	LANWake	PME_STS
E0h	C+CR	R/W	-	-	-	DAC	-	-	-	-

* The registers marked with type = W* can be written only if bits EEM1=EEM0=1.

** The registers marked with type = W** can be written only if bits EEM1=EEM0=1 and CONFIG3<PARM_EN> = 0.

7.2 Summary of EEPROM Power Management Registers

Configuration Space offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3$_{cold}$	PME_D3$_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

8. PCI Configuration Space Registers

8.1 PCI Bus Interface

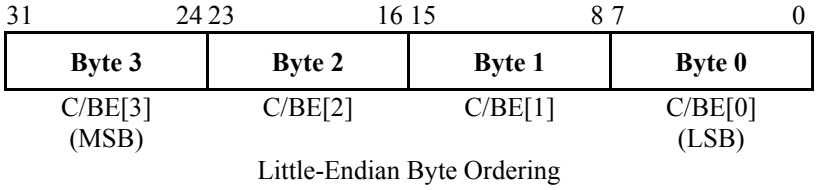
The RTL8139C(L)+ implements the PCI bus interface as defined in the PCI Local Bus Specifications Rev. 2.2. When internal registers are being accessed, the RTL8139C(L)+ acts as a PCI target (slave mode). When accessing host memory for descriptor or packet data transfer, the RTL8139C(L)+ acts as a PCI bus master.

All of the required pins and functions are implemented in the RTL8139C(L)+ as well as the optional pin, INTAB for support of interrupt requests is implemented as well. For more information, refer to the PCI Local Bus Specifications Rev. 2.2, December 18, 1998.

8.1.1 Byte Ordering

The RTL8139C(L)+ is permanently configured to order the bytes of data on the AD[31:0] bus to conform to little-endian ordering. Byte ordering affects bus mastered packet data transfers in 32-bit mode. Register information remains bit aligned (i.e. AD[31] maps to bit 31 in any register space, AD[0] maps to bit 0, etc.) when registers are accessed with 32-bit operations. Bus mastered transfers of buffer descriptor information also remain bit aligned.

Byte orientation for receive and transmit data and descriptors in system memory are done as follows:



Little-Endian Byte Ordering

8.1.2 Interrupt Control

Interrupts are performed by asynchronously asserting the INTAB pin. This pin is an open drain output. The source of the interrupt can be determined by reading the Interrupt Status Register (ISR). One or more bits in the ISR will be set, denoting all currently pending interrupts. Masking of specific interrupts can be accomplished by using the Interrupt Mask Register (IMR). This allows the system to defer interrupt processing as needed.

8.1.3 Latency Timer

The PCI Latency Timer described in MXLAT defines the maximum number of bus clocks that the device will hold the bus. Once the device gains control of the bus and issues FRAMEB, the Latency Timer will begin counting down. If GNTB is deasserted before the RTL8139C(L)+ has finished with the bus, the device will maintain ownership of the bus until the timer reaches zero (or has finished the bus transfer).

8.1.4 32-Bit Data Operation

The RTL8139C(L)+ supports only 32-bit data access.

8.1.5 64-Bit Addressing

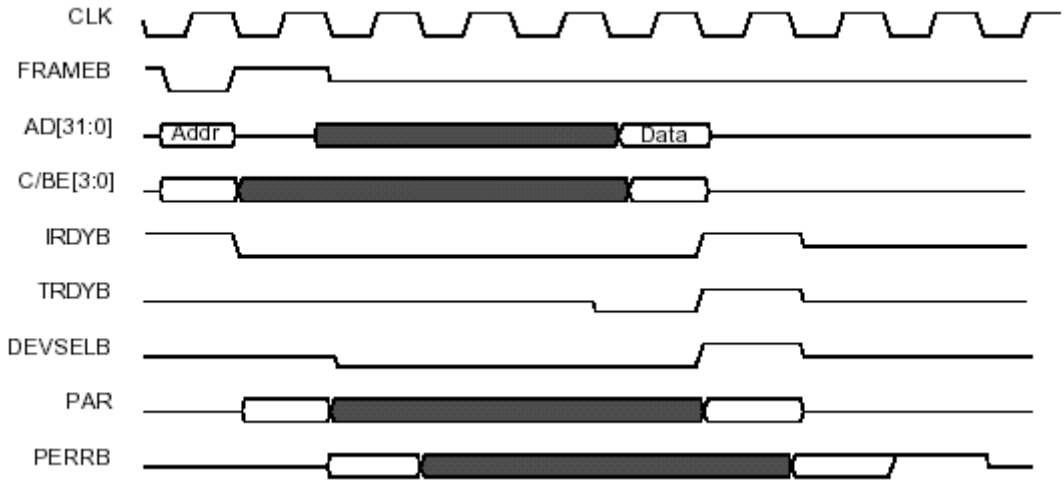
The RTL8139C(L)+ supports 64-bit addressing (Dual Address Cycle) as a bus master for transferring descriptor and packet data information. This mode can be enabled or disabled through software.

8.2 Bus Operation

8.2.1 Target Read

A Target Read operation starts with the system generating FRAMEB, Address, and either an IO read (0010b) or Memory Read (0110b) command. If the 32-bit address on the address bus matches the IO address range specified in IOAR (for I/O reads) or the memory address range specified in MEM (for memory reads), the RTL8139C(L)+ will generate DEVSELB 2 clock cycles later (medium speed). The system must tri-state the Address bus, and convert the C/BE bus to byte enables, after the address cycle. On the 2nd cycle after the assertion of DEVSELB, all 32-bits of data and TRDYB will become valid. If IRDYB is asserted at that time, TRDYB will be forced HIGH on the next clock for 1 cycle, and then tri-stated.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8139C(L)+ will still make data available as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.

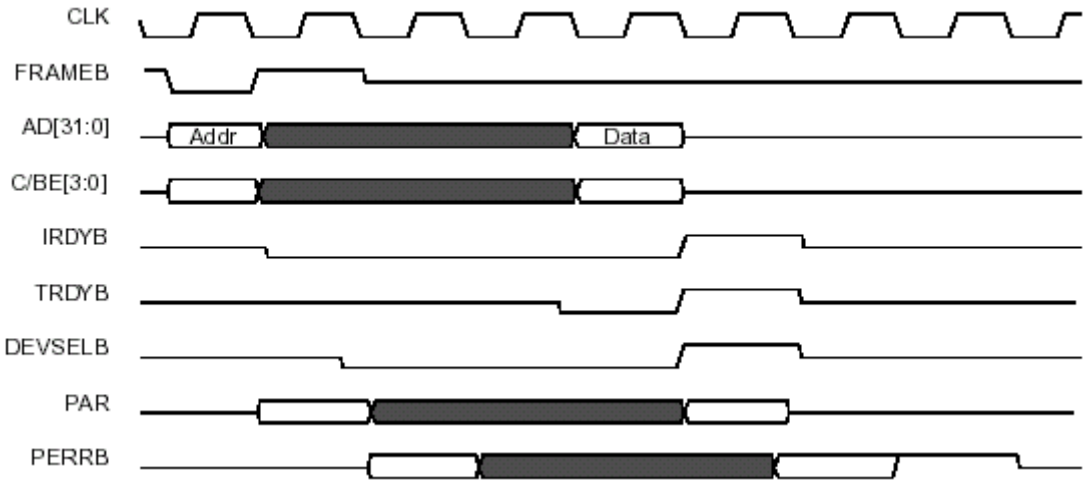


Target Read Operation

8.2.2 Target Write

A Target Write operation starts with the system generating FRAMEB, Address, and Command (0011b or 0111b). If the upper 24 bits on the address bus match IOAR (for I/O reads) or MEM (for memory reads), the RTL8139C(L)+ will generate DEVSELB 2 clock cycles later. On the 2nd cycle after the assertion of DEVSELB, the device will monitor the IRDYB signal. If IRDYB is asserted at that time, the RTL8139C(L)+ will assert TRDYB. On the next clock the 32-bit double word will be latched in, and TRDYB will be forced HIGH for 1 cycle and then tri-stated. Target write operations must be 32-bits wide.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8139C(L)+ will still latch the first double word as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.



Target Write Operation

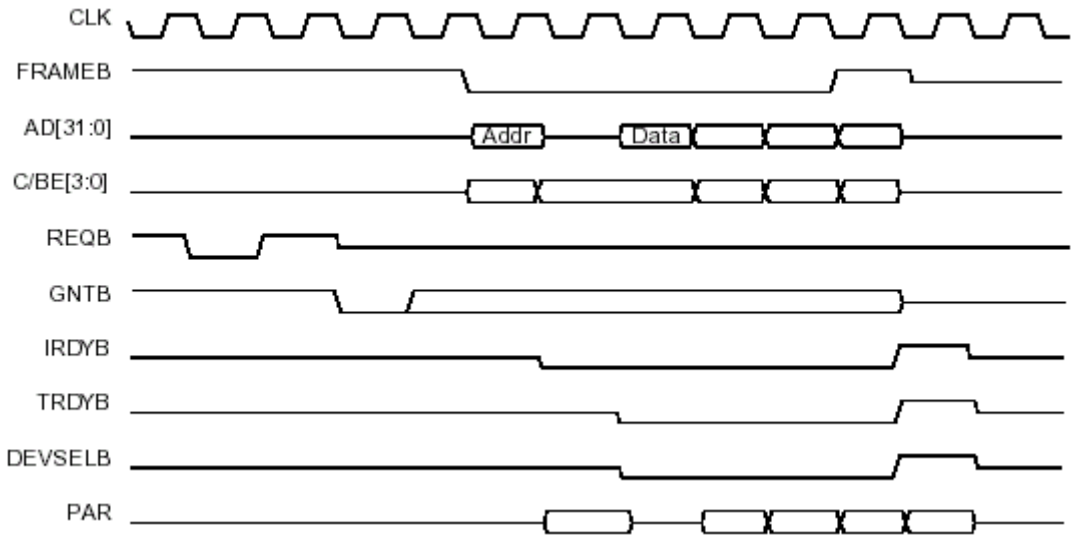
8.2.3 Master Read

A Master Read operation starts with the RTL8139C(L)+ asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a master abort by asserting FRAMEB HIGH for 1 cycle, and IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the address bus will become tri-state, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, data will be latched in (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last read cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the read operation. The RTL8139C(L)+ will never force a wait state during a read operation.



Master Read Operation

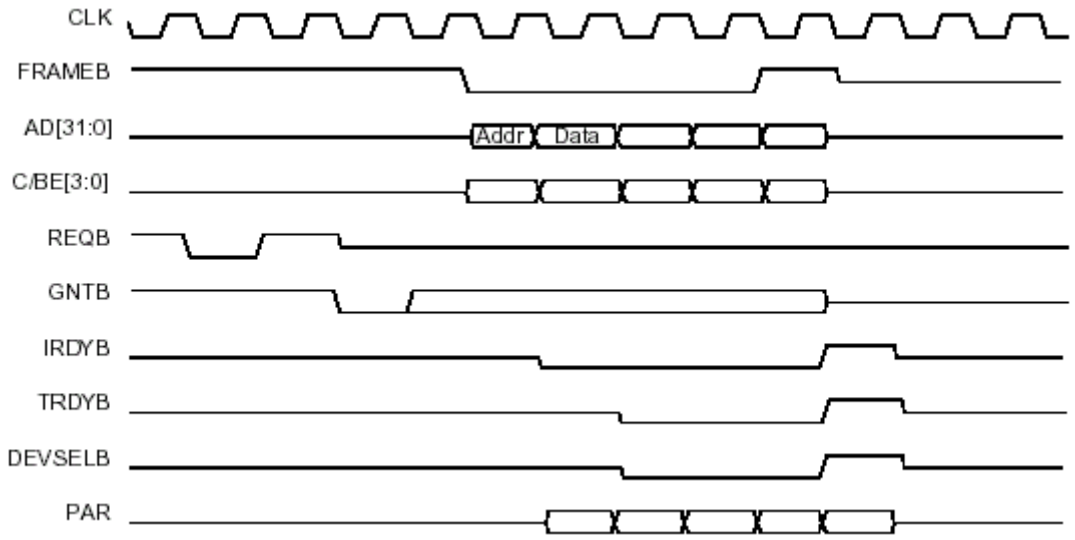
8.2.4 Master Write

A Master Write operation starts with the RTL8139C(L)+ asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a Master Abort by asserting FRAMEB HIGH for 1 cycle. IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the data bus will become valid, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, valid data for the next cycle will become available (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last write cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the write operation. The RTL8139C(L)+ will never force a wait state during a write operation.



Master Write Operation

8.2.5 Configuration Access

Configuration register accesses are similar to target reads and writes in that they are single data word transfers and are initiated by the system. For the system to initiate a Configuration access, it must also generate IDSEL as well as the correct Command (1010b or 1011b) during the Address phase. The RTL8139C(L)+ will respond as it does during Target operations. Configuration reads must be 32-bits wide, but writes may access individual bytes.

8.3 Packet Buffering

The RTL8139C(L)+ incorporates two independent FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data freeing the host system from the real-time demands of the network.

The way in which the FIFOs are emptied and filled is controlled by the FIFO threshold values in the Transmit Configuration and Receive Configuration registers. These values determine how full or empty the FIFOs must be before the device requests the bus. Additionally, there is a threshold value that determines how full the transmit FIFO must be before beginning transmission. Once the RTL8139C(L)+ requests the bus, it will attempt to empty or fill the FIFOs as allowed by the respective MXDMA settings in the Transmit Configuration and Receive Configuration registers.

The RTL8139C(L)+ uses two different modes of buffer management for transmission and reception of data. These two modes are C and C+.

8.3.1 Transmit Buffer Manager

C Mode:

The host CPU initiates a transmit by storing an entire packet of data in one of the descriptors in the main memory, and those descriptors should be double-word alignment. When the entire packet has been transferred to the Tx buffer, the RTL8139C(L)+ is instructed to move the data from the Tx buffer to the internal transmit FIFO in PCI bus master mode. When the transmit FIFO contains a complete packet or is filled to the programmed threshold level, the RTL8139C(L)+ begins packet transmission. Please refer to the Realtek RTL8139 series programming guide for detailed information.

C+ Mode:

The buffer management scheme used on the RTL8139C(L)+ allows quick, simple and efficient use of the frame buffer memory. The buffer management scheme uses separate buffers and descriptors for packet information. This allows effective transfers of data to the transmit buffer manager by simply transferring the descriptor information to the transmit queue.

The Tx Buffer Manager DMAs packet data from PCI memory space and places it in the 2KB transmit FIFO, and pulls data from the FIFO to send to the Tx MAC. Multiple packets may be present in the FIFO, allowing packets to be transmitted with minimum interframe gap. The way in which the FIFO is emptied and filled is controlled by the ETTH (Early Transmit Threshold) and RXFTH (Rx FIFO Threshold) values. Additionally, once the RTL8139C(L)+ requests the bus, it will attempt to fill the FIFO as allowed by the MXDMA setting.

The Tx Buffer Manager process also supports priority queuing of transmit packets. It handles this by drawing from four separate descriptor lists to fill the internal FIFO. If packets are available in the higher priority queues, they will be loaded into the FIFO before those of lower priority.

8.3.2 Receive Buffer Manager

C Mode:

The incoming packet is placed in the Rx FIFO of the RTL8139C(L)+. Concurrently, the RTL8139C(L)+ performs address filtering of multicast packets according to its hash algorithms. When the amount of data in the Rx FIFO reaches the level defined in the Receive Configuration Register (RCR), the RTL8139C(L)+ requests the PCI bus to begin transferring the data to the Rx buffer in PCI bus master mode. The Rx buffer should be pre-allocated and indicated in RCR before packet reception. All received packets stored in Rx buffer, including Rx header and 4-byte CRC, are double-word alignment. I.e., each received packet is placed at next available double-word alignment address after the last received packet in Rx buffer. Please refer to the Realtek RTL8139 series programming guide for detailed information.

C+ Mode:

The Rx Buffer Manager uses the same buffer management scheme as used for transmits. The Rx Buffer Manager retrieves packet data from the Rx MAC and places it in the 2KB receive data FIFO, and pulls data from the FIFO for DMA to PCI memory space. Similar to the transmit FIFO, the receive FIFO is controlled by the FIFO threshold value in RXFTH. This value determines the number of long words written into the FIFO from the MAC unit before a DMA request for system memory occurs. Once the RTL8139C(L)+ gets the bus, it will continue to transfer the long words from the FIFO until the data in the FIFO is less than one long word, or has reached the end of the packet, or the max DMA burst size is reached , as set in MXDMA.

8.3.3 Packet Recognition

The Rx packet filter and recognition logic allows software to control which packets are accepted, based on destination address and packet type. Address recognition logic includes support for broadcast, multicast hash, and unicast addresses. The packet recognition logic includes support for WOL, Pause, and programmable pattern recognition.

8.4 PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	MWIEN	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	MWIEN	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	FBTBEN	SERREN
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	FBBC	0	0	NewCap	0	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	DST1	DST0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R/W	0	0	0	0	0	0	0	0
0Dh	LTR	R	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		R/W	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		R/W	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		R/W	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h	MEMAR	R	0	0	0	0	0	0	0	MEMIN
		W	-	-	-	-	-	-	-	-
15h		R/W	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
16h		R/W	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
17h		R/W	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
18h-27h	RESERVED									
28h-2Bh	CISPtr	Cardbus CIS Pointer								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		R/W	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	1	0	0	0	0

35h-3Bh	RESERVED									
3Ch	ILR	R/W	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h–4Fh	RESERVED									
50h	PMID	R	0	0	0	0	0	0	0	1
51h	NextPtr	R	0	0	0	0	0	0	0	0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3$_{cold}$	PME_D3$_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
54h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
55h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
56h–5Fh	RESERVED									
60h	VPDID	R	0	0	0	0	0	0	1	1
61h	NextPtr	R	0	0	0	0	0	0	0	0
62h	Flag VPD Address	R/W	VPDADDR 7	VPDADDR 6	VPDADD R5	VPDADD R4	VPDADD R3	VPDADD R2	VPDADD R1	VPDADD R0
63h		R/W	Flag	VPDADDR 14	VPDADD R13	VPDADD R12	VPDADD R11	VPDADD R10	VPDADD R9	VPDADD R8
64h	VPD Data	R/W	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
65h		R/W	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
66h		R/W	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
67h		R/W	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
68h-FFh	RESERVED									

8.5 PCI Configuration Space Functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the configuration space for the RTL8139C(L)+ are described below.

VID: Vendor ID. This field will be set to a value corresponding to PCI Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Vendor ID.

DID: Device ID. This field will be set to a value corresponding to PCI Device ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Symbol	Description
15-10	-	**Reserved**
9	FBTBEN	**Fast Back-To-Back Enable:** Config3<FBtBEn>=0:Read as 0. Write operation has no effect. The RTL8139C(L)+ will not generate Fast Back-to-back cycles. When Config3<FbtBEn>=1, This read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means the master is allowed to generate fast back-to-back transaction to different agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent. This bit's state after RST# is 0.
8	SERREN	**System Error Enable:** When set to 1, the RTL8139C(L)+ asserts the SERRB pin when it detects a parity error on the address phase (AD<31:0> and CBEB<3:0>).
7	ADSTEP	**Address/Data Stepping:** Read as 0, write operation has no effect. The RTL8139C(L)+ never make address/data stepping.
6	PERRSP	**Parity Error Response:** When set to 1, the RTL8139C(L)+ will assert the PERRB pin on the detection of a data parity error when acting as the target, and will sample the PERRB pin as the master. When set to 0, any detected parity error is ignored and the RTL8139C(L)+ continues normal operation. Parity checking is disabled after hardware reset (RSTB).
5	VGASNOOP	**VGA palette SNOOP:** Read as 0, write operation has no effect.
4	MWIEN	**Memory Write and Invalidate Cycle Enable:** This is an enable bit for using Memory Write and Invalidate command. When this bit is 1, the RTL8139C(L)+ as a master may generate the command. When this bit is 0, the RTL8139C(L)+ may generate Memory Write command instead. State after PCI RSTB is 0.
3	SCYCEN	**Special Cycle Enable:** Read as 0, write operation has no effect. The RTL8139C(L)+ ignores all special cycle operations.
2	BMEN	**Bus Master Enable:** When set to 1, the RTL8139C(L)+ is capable of acting as a bus master. When set to 0, it is prohibited from acting as a PCI bus master. For normal operations, this bit must be set by the system BIOS.
1	MEMEN	**Memory Space Access:** When set to 1, the RTL8139C(L)+ responds to memory space accesses. When set to 0, the RTL8139C(L)+ ignores memory space accesses.
0	IOEN	**I/O Space Access:** When set to 1, the RTL8139C(L)+ responds to IO space access. When set to 0, the RTL8139C(L)+ ignores I/O space accesses.

Status: The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Bit	Symbol	Description
15	DPERR	**Detected Parity Error:** When set indicates that the RTL8139C(L)+ detected a parity error, even if parity error handling is disabled in command register PERRSP bit.
14	SSERR	**Signaled System Error:** When set indicates that the RTL8139C(L)+ asserted the system error pin, SERRB. Writing a 1 clears this bit to 0.
13	RMABT	**Received Master Abort:** When set indicates that the RTL8139C(L)+ terminated a master transaction with master abort. Writing a 1 clears this bit to 0.
12	RTABT	**Received Target Abort:** When set indicates that the RTL8139C(L)+ master transaction was terminated due to a target abort. Writing a 1 clears this bit to 0.
11	STABT	**Signaled Target Abort:** Set to 1 whenever the RTL8139C(L)+ terminates a transaction with target abort. Writing a 1 clears this bit to 0.
10-9	DST1-0	**Device Select Timing:** These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the RTL8139C(L)+ will assert DEVSELB two clocks after FRAMEB is asserted.
8	DPD	**Data Parity error Detected:** This bit sets when the following conditions are met: • The RTL8139C(L)+ asserts parity error(PERRB pin) or it senses the assertion of PERRB pin by another device. • The RTL8139C(L)+ operates as a bus master for the operation that caused the error. • The Command register PERRSP bit is set. Writing a 1 clears this bit to 0.
7	FBBC	**Fast Back-To-Back Capable:** Config3<FbtBEn>=0, Read as 0, write operation has no effect. Config3<FbtBEn>=1, Read as 1.
6	UDF	**User Definable Features Supported:** Read as 0, write operation has no effect. The RTL8139C(L)+ does not support UDF.
5	66MHz	**66 MHz Capable:** Read as 0, write operation has no effect. The RTL8139C(L)+ has no 66MHz capability.
4	NewCap	**New Capability:** Config3<PMEn>=0, Read as 0, write operation has no effect. Config3<PMEn>=1, Read as 1.
0-3	-	**Reserved**

RID: Revision ID Register: An 8-bit register that specifies the RTL8139C(L)+ controller revision number.

PIFR: Programming Interface Register. An 8-bit register that identifies the programming interface of the RTL8139C(L)+ controller. The PCI specifications, revision 2.1, do not define any other specific values for network devices. So PIFR = 00h.

SCR: Sub-Class Register. An 8-bit register that identifies the function of the RTL8139C(L)+. SCR = 00h indicates that the RTL8139C(L)+ is an Ethernet controller.

BCR: Base-Class Register. An 8-bit register that broadly classifies the function of the RTL8139C(L)+. BCR = 02h indicates that the RTL8139C(L)+ is a network controller.

CLS: Cache Line Size. Specifies, in units of 32-bit words (double-words), the system cache line size. The RTL8139C(L)+ supports cache line size of 8, and 16 longwords (DWORDs). The RTL8139C(L)+ uses Cache Line Size for PCI commands that are cache oriented, such as memory-read-line, memory-read-multiple, and memory-write-and-invalidate.

LTR: Latency Timer Register. Specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8139C(L)+. When the RTL8139C(L)+ asserts FRAMEB, it enables its latency timer to count. If the RTL8139C(L)+ deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8139C(L)+ initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write, and the default value is 00H.

HTR: Header Type Register. Reads will return a 0, writes are ignored.

BIST: Built-in Self Test. Reads will return a 0, writes are ignored.

IOAR: This register specifies the BASE IO address which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space.

Bit	Symbol	Description
31-8	IOAR31-8	**BASE IO Address:** This is set by software to the Base IO address for the operational register map.
7-2	IOSIZE	**Size Indication:** Read back as 0. This allows the PCI bridge to determine that the RTL8139C(L)+ requires 256 bytes of IO space.
1	-	**Reserved**
0	IOIN	**IO Space Indicator:** Read only. Set to 1 by the RTL8139C(L)+ to indicate that it is capable of being mapped into IO space.

MEMAR: This register specifies the base memory address for memory accesses to the RTL8139C(L)+ operational registers. This register must be initialized prior to accessing any of the RTL8139C(L)+'s registers with memory access.

Bit	Symbol	Description
31-8	MEM31-8	**Base Memory Address:** This is set by software to the base address for the operational register map.
7-4	MEMSIZE	**Memory Size:** These bits return 0, which indicates that the RTL8139C(L)+ requires 256 bytes of Memory Space.
3	MEMPF	**Memory Prefetchable:** Read only. Set to 0 by the RTL8139C(L)+.
2-1	MEMLOC	**Memory Location Select:** Read only. Set to 0 by the RTL8139C(L)+. This indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space.
0	MEMIN	**Memory Space Indicator:** Read only. Set to 0 by the RTL8139C(L)+ to indicate that it is capable of being mapped into memory space.

CISPtr: CardBus CIS Pointer. This field is valid only when CardB_En (bit3, Config3) = 1. The value of this register is auto-loaded from 93C46 or 93C56 (from offset 30h-31h).

- Bit 2-0: Address Space Indicator

Bit2-0	Meaning
0	Not supported. (CIS begins in device-dependent configuration space.)
1-6	The CIS begins in the memory address governed by one of the six Base Address Registers. Ex., if the value is 2, then the CIS begins in the memory address space governed by Base Address Register 2.
7	The CIS begins in the Expansion ROM space.

- Bit27-3: Address Space Offset
- Bit31-28: ROM Image number

Bit2-0	Space Type	Address Space Offset Values
0	Configuration space	Not supported.
X; 1≤X≤6	Memory space	0h≤value≤FFFF FFF8h. This is the offset into the memory address space governed by Base Address Register X. Adding this value to the value in the Base Address Register gives the location of the start of the CIS. For RTL8139C(L)+, the value is 100h.
7	Expansion ROM	0≤image number≤Fh, 0h≤value≤0FFF FFF8h. This is the offset into the expansion ROM address space governed by the Expansion ROM Base Register. The image number is in the uppermost nibble of the CISPtr register. The value consists of the remaining bytes. For RTL8139C(L)+, the image number is 0h.

This read-only register points to where the CIS begins, in one of the following spaces:

i. Memory space --- The CIS may be in any of the memory spaces from offset 100h and up after being auto-loaded from 93C56. The CIS is stored in 93C56 EEPROM physically from offset 80h-FFh.

ii. Expansion ROM space --- The CIS is stored in expansion ROM physically within the 128KB max.

SVID: Subsystem Vendor ID. This field will be set to a value corresponding to PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Subsystem Vendor ID.

SMID: Subsystem ID. This field will be set to value corresponding to PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

BMAR: This register specifies the base memory address for memory accesses to the RTL8139C(L)+ operational registers. This register must be initialized prior to accessing any RTL8139C(L)+'s register with memory access.

Bit	Symbol	Description
31-18	BMAR31-18	Boot ROM Base Address
17-11	ROMSIZE	These bits indicate how many Boot ROM spaces to be supported. The Relationship between Config 0 <BS2:0> and BMAR17-11 is as follows: **BS2 BS1 BS0 Description** 0 0 0 No Boot ROM, BROMEN=0 (R) 0 0 1 8K Boot ROM, BROMEN (R/W), BMAR12-11 = 0 (R), BMAR17-13 (R/W) 0 1 0 16K Boot ROM, BROMEN (R/W), BMAR13-11 = 0 (R), BMAR17-14 (R/W) 0 1 1 32K Boot ROM, BROMEN (R/W), BMAR14-11 = 0 (R), BMAR17-15 (R/W) 1 0 0 64K Boot ROM, BROMEN (R/W), BMAR15-11 = 0 (R), BMAR17-16 (R/W) 1 0 1 128K Boot ROM, BROMEN(R/W), BMAR16-11=0 (R), BMAR17 (R/W) 1 1 0 unused 1 1 1 unused
10-1	-	Reserved (read back 0)
0	BROMEN	Boot ROM Enable: This is used by the PCI BIOS to enable accesses to Boot ROM.

ILR: Interrupt Line Register. An 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the RTL8139C(L)+.

IPR: Interrupt Pin Register. An 8-bit register indicating the interrupt pin used by the RTL8139C(L)+. The RTL8139C(L)+ uses INTA interrupt pin. Read only. IPR = 01H.

MNGNT: Minimum Grant Timer: Read only. Specifies how long a burst period the RTL8139C(L)+ needs at 33 MHz clock rate in units of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

MXLAT: Maximum Latency Timer: Read only. Specifies how often the RTL8139C(L)+ needs to gain access to the PCI bus in unit of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

8.6 The Default Value After Power-on (RSTB asserted)

PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	1	1	1	0	1	1	0	0
01h		R	0	0	0	1	0	0	0	0
02h	DID	R	0	0	1	0	1	0	0	1
03h		R	1	0	0	0	0	0	0	1
04h	Command	R	0	0	0	0	0	0	0	0
		W	-	PERRSP	-	MWIEN	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	0	0	0	NewCap	0	0	0	0
07h		R	0	0	0	0	0	0	1	0
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	1	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R/W	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	1
11h		R/W	0	0	0	0	0	0	0	0
12h		R/W	0	0	0	0	0	0	0	0
13h		R/W	0	0	0	0	0	0	0	0
14h	MEMAR	R	0	0	0	0	0	0	0	0
15h		R/W	0	0	0	0	0	0	0	0
16h		R/W	0	0	0	0	0	0	0	0
17h		R/W	0	0	0	0	0	0	0	0
18h | 27h	-	RESERVED(ALL 0)								
28h	CISPtr	R	0	0	0	0	0	0	0	0
29h		R	0	0	0	0	0	0	0	0
2Ah		R	0	0	0	0	0	0	0	0
2Bh		R	0	0	0	0	0	0	0	0
2Ch	SVID	R	1	1	1	0	1	1	0	0
2Dh		R	0	0	0	1	0	0	0	0
2Eh	SMID	R	0	0	1	0	1	0	0	1
2Fh		R	1	0	0	0	0	0	0	1
30h	BMAR	R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	BROMEN
31h		R	0	0	0	0	0	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	0	0	0	0	0	0	0	0
33h		R/W	0	0	0	0	0	0	0	0

34h	Cap-Ptr	R	Ptr7	Ptr6	Ptr5	Ptr4	Ptr3	Ptr2	Ptr1	Ptr0
35h | 3Bh	-	RESERVED(ALL 0)								
3Ch	ILR	R/W	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h | FFh	-	RESERVED(ALL 0)								

8.7 PCI Power Management Functions

The RTL8139C(L)+ is compliant to ACPI (V1.0, V2.0), PCI Power Management (Rev 1.1), and Device Class Power Management Reference Specification (V1.0a), such as to support OS Directed Power Management (OSPM) environment. To support this, the RTL8139C(L)+ provides the following capabilities:

- The RTL8139C(L)+ can monitor the network for a Wakeup Frame, a Magic Packet, or a Link Change, and notify the system via PME# when such a packet or event arrives. Then, the whole system can restore to working state to process the incoming jobs.
- The RTL8139C(L)+ can be isolated from the PCI bus automatically with the auxiliary power circuit when the PCI bus is in B3 state, i.e. the power on the PCI bus is removed. When the motherboard includes a built-in RTL8139C(L)+ single-chip fast Ethernet controller, the RTL8139C(L)+ can be disabled when needed by pulling the isolate pin low to 0V.

When the RTL8139C(L)+ is in power down mode (D1 ~ D3),

- The Rx state machine is stopped, and the RTL8139C(L)+ keeps monitoring the network for wakeup events such Magic Packet, Wakeup Frame, and/or Link Change, in order to wake up the system. When in power down mode, the RTL8139C(L)+ will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO.
- The FIFO status and the packets which are already received into Rx FIFO before entering into power down mode, are kept by the RTL8139C(L)+ during power down mode
- The transmission is stopped. The action of PCI bus master mode is stopped, as well. The Tx FIFO is kept.
- After restoration to a D0 state, the PCI bus master mode continues to transfer the data, which is not yet moved into the Tx FIFO from the last break. The packet that was not transmitted completely last time is transmitted again.

D3cold_support_PME bit(bit15, PMC register) & Aux_I_b2:0 (bit8:6, PMC register) in PCI configuration space .
If EEPROM D3cold_support_PME bit(bit15, PMC) = 1, the above 4 bits depend on the existence of Aux power.
If EEPROM D3cold_support_PME bit(bit15, PMC) = 0, the above 4 bits are all 0's.

Examples:

1. If EEPROM D3c_support_PME = 1,
   - If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC, i.e. if EEPROM PMC = C2 F7, then PCI PMC = C2 F7.
   - If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's. I.e. if EEPROM PMC = C2 F7, the PCI PMC = 02 76.
     - In this case, if wakeup support is desired when the main power is off, it is suggested that the EEPROM PMC bet set to C2 F7 (RT EEPROM default value).

2. If EEPROM D3c_support_PME = 0,
   - If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC. I.e. if EEPROM PMC = C2 77, then PCI PMC = C2 77.
   - If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's. I.e. if EEPROM PMC = C2 77, the PCI PMC = 02 76.
     - In this case, if wakeup support is not desired when the main power is off, it is suggested that the EEPROM PMC be set to 02 76.

Link Wakeup occurs only when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the RTL8139C(L)+ is in an isolation state, or the PME# can be asserted in current power state.
- The Link status is re-established.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet matches.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the RTL8139C(L)+ is in isolation state, or the PME# can be asserted in current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC(can be none)+ 16 * DID(Destination ID) in any part of a valid (Fast) Ethernet packet.

Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame matches.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 8-bit CRC* (or 16-bit CRC) of the received Wakeup Frame matches with the 8-bit CRC* (or 16-bit CRC) of the sample Wakeup Frame pattern received from the local machine's OS.
- The last masked byte** of the received Wakeup Frame matches with the last masked byte** of the sample Wakeup Frame pattern provided by the local machine's OS. (In Long Wakeup Frame mode, the last masked byte field is replaced with the high byte of the 16-bit CRC.)

*** 8-bit CRC:**

This 8-bit CRC logic is used to generate an 8-bit CRC from the masked bytes of the received Wakeup Frame packet within offset 12 to 75. Software should calculate the 8-bit Power Management CRC for each specific sample wakeup frame and store the calculated CRC in the corresponding CRC register for the RTL8139C(L)+ to check if there is Wakeup Frame packet coming in.

*** 16-bit CRC: (Long Wakeup Frame mode, the mask bytes cover from offset 0 to 127)**

Long Wakeup Frame: The RTL8139C(L)+ also supports 3 long Wakeup Frames. If the range of mask bytes of the sample Wakeup Frame, passed down by the OS to the driver, exceeds the range from offset 12 to 75, the related registers of wakeup frame 2 and 3 can be merged to support one long wakeup frame by setting the LongWF (bit0, CONFIG4). Thus, the range of effective mask bytes extends from offset 0 to 127. The low byte and high byte of calculated 16-bit CRC should be stored into register CRC2 and LSBCRC2 respectively. The mask bytes (16 bytes) should be stored to register Wakeup2 and Wakeup3. The CRC3 and LSBCRC3 have no meaning in this case and should be reset to 0. So as the long Wakeup Frame pairs, wakeup frame 4 and 5, wakeup frame 6 and 7 each make up one wakeup frame. The CRC5, CRC7, LSBCRC5, and LSBCRC7 have no meaning in this case and should be reset to 0, if the RTL8139C(L)+ is set to support long Wakeup Frame. In this case, the RTL8139C(L)+ support 5 wakeup frames, that are 2 normal wakeup frames and 3 long wakeup frames.

**** Last masked byte:**

The last byte of the masked bytes of the received Wakeup Frame packet within offset 12 to 75 (in 8-bit CRC mode) should matches with the last byte of the masked bytes of the sample Wakeup Frame provided by the local machine's OS.

The PME# signal is asserted only when the following are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8139C(L)+ may assert PME# in current power state, or the RTL8139C(L)+ is in isolation[1] state. Refer to PME_Support(bit15-11) of the PMC register in PCI Configuration Space.
- Magic Packet, LinkUp, or Wakeup Frame has occurred.

Note: Writing a 1 to the PME_Status (bit15) of PMCSR register in the PCI Configuration Space will clear this bit and cause the RTL8139C(L)+ to stop asserting a PME# (if enabled).

When the RTL8139C(L)+ is in power down mode, ex. D1-D3, the IO, MEM, and Boot ROM space are all disabled. After RST# asserted, the power state must be changed to D0 if the original power state is $D3_{cold}$. There is no hardware enforced delays at RTL8139C(L)+'s power state. When in ACPI mode, the RTL8139C(L)+ does not support PME from D0, due to the setting of PMC register. This setting comes from EEPROM.

The RTL8139C(L)+ also supports LAN WAKE-UP function. The LWAKE pin is used to notify the motherboard to execute wake-up process whenever the RTL8139C(L)+ receives a wakeup event, such as Magic Packet.

The LWAKE signal is asserted according the following setting.

- LWPME bit (bit4, CONFIG4):
  0: The LWAKE is asserted whenever there is wakeup event occurs.
  1: The LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low.
- Bit1 of DELAY byte(offset 1Fh, EEPROM):
  0: LWAKE signal is disabled.
  1: LWAKE signal is enabled

8.8 Vital Product Data (VPD)

Bit 31 of the VPD is used to issue VPD read/write command and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56 is completed or not.

1. Write VPD register: (write data to 93C46/93C56) Write the flag bit to a one (at the same time the VPD address is written). When the flag bit is set to zero by the RTL8139C(L)+, the VPD data (all 4 bytes) has been transferred from the VPD data register to 93C46/93C56.
2. Read VPD register: (read data from 93C46/93C56) Write the flag bit to a zero at the same time the VPD address is written). When the flag bit is set to one by the RTL8139C(L)+, the VPD data (all 4 bytes) has been transferred from 93C46/93C56 to the VPD data register.

9. Functional Description

9.1 Transmit & Receive Operations in C mode

9.1.1 Transmit

The host CPU initiates a transmit by storing an entire packet of data in one of the descriptors in the main memory. Those descriptors should be aligned in double-word format. When the entire packet has been transferred to the Tx buffer, the RTL8139C(L)+ is instructed to move the data from the Tx buffer to the internal transmit FIFO in PCI bus master mode. When the transmit FIFO contains a complete packet or is filled to the programmed threshold level, the RTL8139C(L)+ begins packet transmission. Please refer to the Realtek RTL8139 series programming guide for detailed information.

9.1.2 Receive

The incoming packet is placed in the RTL8139C(L)+'s Rx FIFO. Concurrently, the RTL8139C(L)+ performs address filtering of multicast packets according to its hash algorithms. When the amount of data in the Rx FIFO reaches the level defined in the Receive Configuration Register (RCR), the RTL8139C(L)+ requests the PCI bus to begin transferring the data to the Rx buffer in PCI bus master mode. The Rx buffer should be pre-allocated and indicated in RCR before packet reception. All received packets stored in Rx buffer, including Rx header and 4-byte CRC, are double-word alignment. I.e., each received packet is placed at next available double-word alignment address after the last received packet in Rx buffer. Please refer to Realtek RTL8139 series programming guide for detailed information.

9.2 Transmit & Receive Operations in C+ mode

In C+ mode, the RTL8139C(L)+ supports a new descriptor-based buffer management that will significantly lower host CPU utilization and is more suitable for server applications. The new buffer management algorithm provides capabilities of Microsoft Large-Send offload, IP checksum offload, TCP checksum offload, UDP checksum offload, and IEEE802.1P, 802.1Q VLAN tagging. The RTL8139C(L)+ supports up to 64 consecutive descriptors in memory for transmit and receive separately, which means there can be 3 descriptor rings, one is a high priority transmit descriptor ring, another is a normal priority transmit descriptor ring, and the other is a receive descriptor ring. Each descriptor ring may consist of up to 64 4-double-word consecutive descriptors. Each descriptor consists of 4 consecutive double words. The start address of each descriptor group should be 256-byte alignment. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained to form a packet, in both Tx and Rx. Please refer to the Realtek RTL8139C(L)+ programming guide for detailed information. Any Tx buffer pointed to by one of Tx descriptors should be at least 4 bytes.

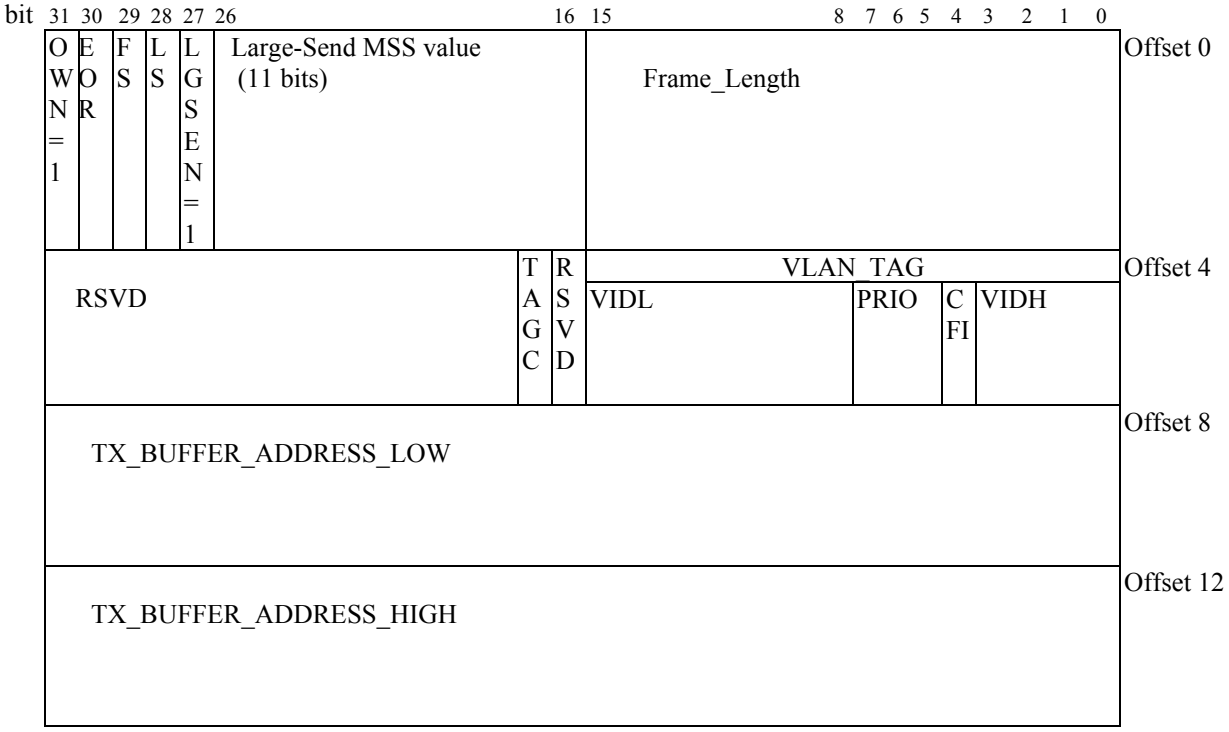
Padding: The RTL8139C+ will automatically pad any packet less than 64 bytes (including 4 bytes CRC) to 64-bytes in length (including 4-byte CRC) before transmitting that packet onto network medium, when the PAD bit is set to 1 in the C+CR (offset E0h) C+ command register.

If a packet consists of 2 or more descriptors, then the descriptors in command mode should have the same configuration, except EOR, FS, LS bits.

9.2.1 Transmit

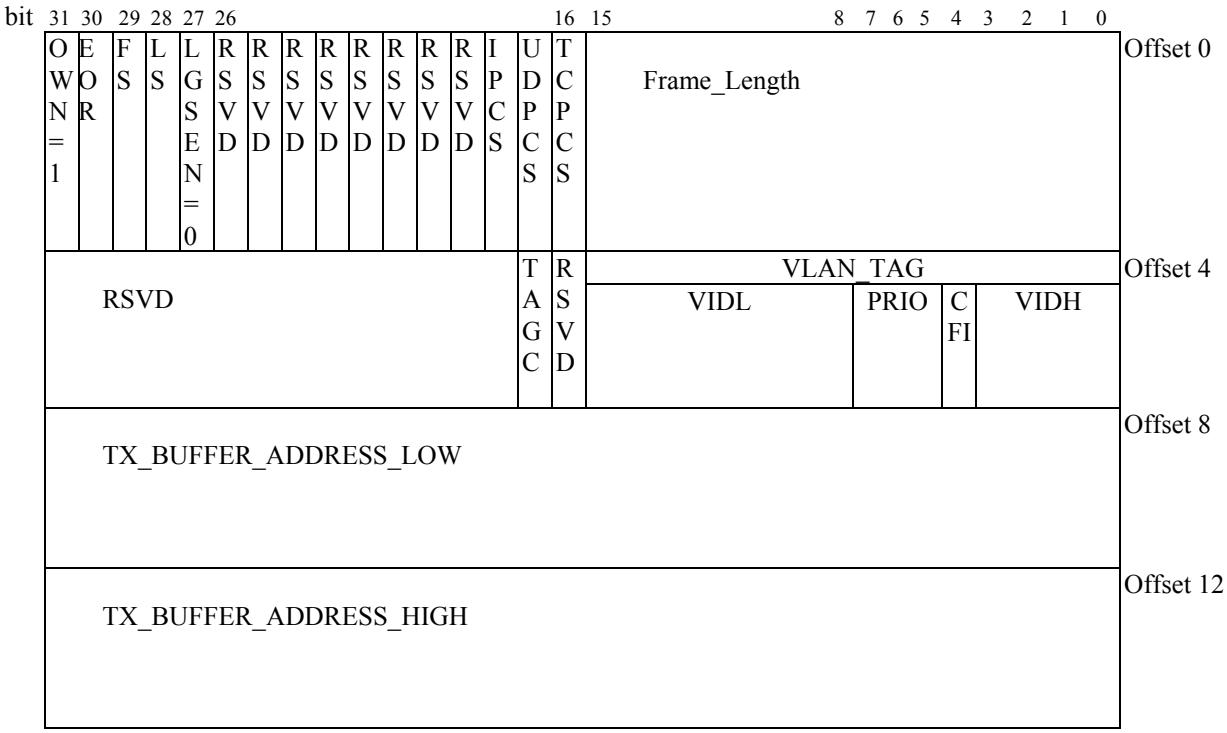
The following information describes what the Tx descriptor may look like, depending on different settings in each Tx descriptor.

Large-Send Task Offload Tx Descriptor Format (Before transmitting, OWN=1, LGSEN=1, Tx command mode 0)



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, indicates that the descriptor is owned by the NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.
0	30	EOR	**End of descriptor Ring:** When set, indicates that this is the last descriptor in the descriptor ring. When the internal transmit pointer of the NIC reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	**First Segment Descriptor:** When set, indicates that this is the first descriptor of a Tx packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last Segment Descriptor:** When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27	LGSEN	**TCP/IP Large Send Operation Enable:** A command bit. The driver sets this bit to ask the NIC to offload the Large send operation. In this case, LGSEN=1.
0	26-16	MSS	**Maximum Segmentation Size:** This is a command field, 11-bits long. The driver passes large send MSS to the NIC through this field.
0	15-0	Frame_Length	**Transmit Frame Length:** This field indicates the length in the Tx buffer, in bytes, to be transmitted.
4	31-18	RSVD	**Reserved**
4	17	TAGC	**VLAN Tag Control Bit:** 1: Enable. 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is a IEEE 802.1Q VLAN packet) is inserted after source address, and 2 bytes are inserted after tag protocol ID from VLAN_TAG field in transmit descriptor. 0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by upper layer.
4	16	RSVD	**Reserved**
4	15-0	VLAN_TAG	The 2-byte VLAN_TAG contains information, from upper layer, of user priority, canonical format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	TxBuffL	**Low 32-bit Address of Transmit Buffer**
12	31-0	TxBuffH	**High 32-bit Address of Transmit Buffer**

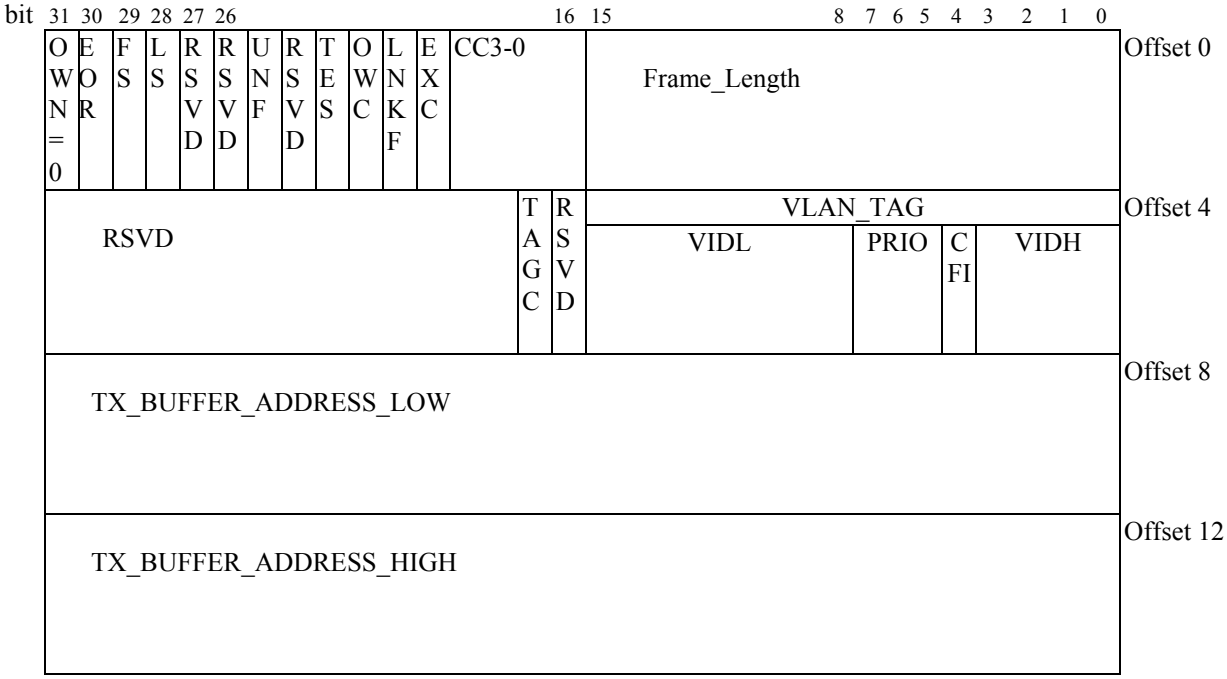
Normal (including IP, TCP, UDP Checksum Task Offloads) Tx Descriptor Format (before transmitting, OWN=1, LGSEN=0, Tx command mode 1)



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, indicates that the descriptor is owned by the NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.
0	30	EOR	**End of Descriptor Ring:** When set, indicates that this is the last descriptor in the descriptor ring. When the internal transmit pointer of the NIC reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	**First Segment Descriptor:** When set, indicates that this is the first descriptor of a Tx packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last segment descriptor:** When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27	LGSEN	**A Command Bit:** TCP/IP Large send operation enable. Driver sets this bit to ask NIC to offload Large send operation. In this case, LGSEN=0.
0	26-19	RSVD	**Reserved**
0	18	IPCS	**IP Checksum Offload:** A command bit. Driver sets this bit to ask NIC to offload IP checksum.
0	17	UDPCS	**UDP Checksum Offload:** A command bit. Driver sets this bit to ask NIC to offload UDP checksum.
0	16	TCPCS	**TCP checksum offload enable:** A command bit. The driver sets this bit to ask the NIC to offload the TCP checksum.
0	15-0	Frame_Length	**Transmit Frame Length:** This field indicates the length in the Tx buffer, in bytes, to be transmitted
4	31-18	RSEV	**Reserved**
4	17	TAGC	**VLAN Tag Control Bit:** 1: Enable. 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is a IEEE 802.1Q VLAN packet) is inserted after source address, and 2 bytes are inserted after tag protocol ID from VLAN_TAG field in transmit descriptor. 0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by upper layer.
4	16	RSEV	**Reserved**
4	15-0	VLAN_TAG	The 2-byte VLAN_TAG contains information, from upper layer, of user priority, canonical format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	TxBuffL	**Low 32-bit Address of Transmit Buffer**
12	31-0	TxBuffH	**High 32-bit Address of Transmit Buffer**

Tx Status Descriptor (After transmitting, OWN=0, Tx status mode)

After having transmitted, the Tx descriptor turns into a Tx status descriptor.



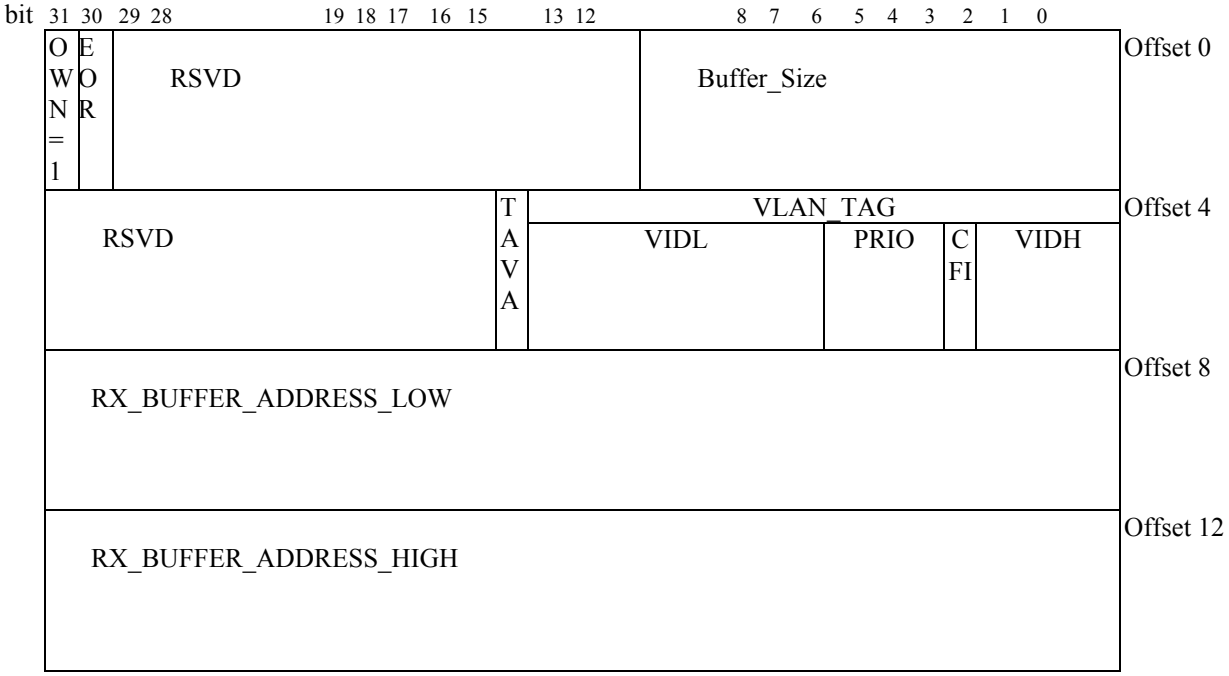
Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, indicates that the descriptor is owned by the NIC. When cleared, indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is already transmitted. In this case, OWN=0.
0	30	EOR	**End of Descriptor Ring:** When set, indicates that this is the last descriptor in the descriptor ring. When the internal transmit pointer of the NIC reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	**First Segment Descriptor:** When set, indicates that this is the first descriptor of a Tx packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last Segment Descriptor:** When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27-26	RSVD	**Reserved**
0	25	UNF	**FIFO Underrun:** A status bit. NIC sets this bit to inform driver that FIFO underrun had ever occurred before this packet transmitted.
0	24	RSVD	**Reserved**
0	23	TES	**Transmit Error Summary:** When set, indicates that at least one of the following errors has occurred: OWC, EXC, LNKF. This bit is valid only when the LS (Last segment) bit is set.
0	22	OWC	**Out of Window Collision:** A status bit. When set, it means an "out-of-window" collision is encountered during transmission of a packet.
0	21	LNKF	**Link Failure:** A status bit. The NIC sets this bit to inform the driver of a link failure.
0	20	EXC	**Excessive Collision:** When set, indicates that the transmission was aborted due to 16 consecutive collisions.
0	19-16	CC3-0	**Collision Counter:** When Own bit =0, this is a status field. A 4-bit collision counter, showing the total collision times before the packet was transmitted.
0	15-0	Frame_Length	**Transmit Frame Length:** This field indicates the length of the Tx buffer, in bytes, to be transmitted
4	31-18	RSEV	**Reserved**
4	17	TAGC	**VLAN Tag Control Bit:** 1: Enable. 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is a IEEE 802.1Q VLAN packet) is inserted after source address, and 2 bytes are inserted after tag protocol ID from VLAN_TAG field in transmit descriptor. 0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was passed down by upper layer.
4	16	RSEV	**Reserved**
4	15-0	VLAN_TAG	The 2-byte VLAN_TAG contains information, from upper layer, of user priority, canonical format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	TxBuffL	**Low 32-bit Address of Transmit Buffer**
12	31-0	TxBuffH	**High 32-bit Address of Transmit Buffer**

9.2.2 Receive

The following information describes what the Rx descriptor may look like, depending on different states in each Rx descriptor. Any Rx buffer, which is pointed to by one of the Rx descriptors, should be at least 4 bytes.

Rx Command Descriptor (OWN=1)

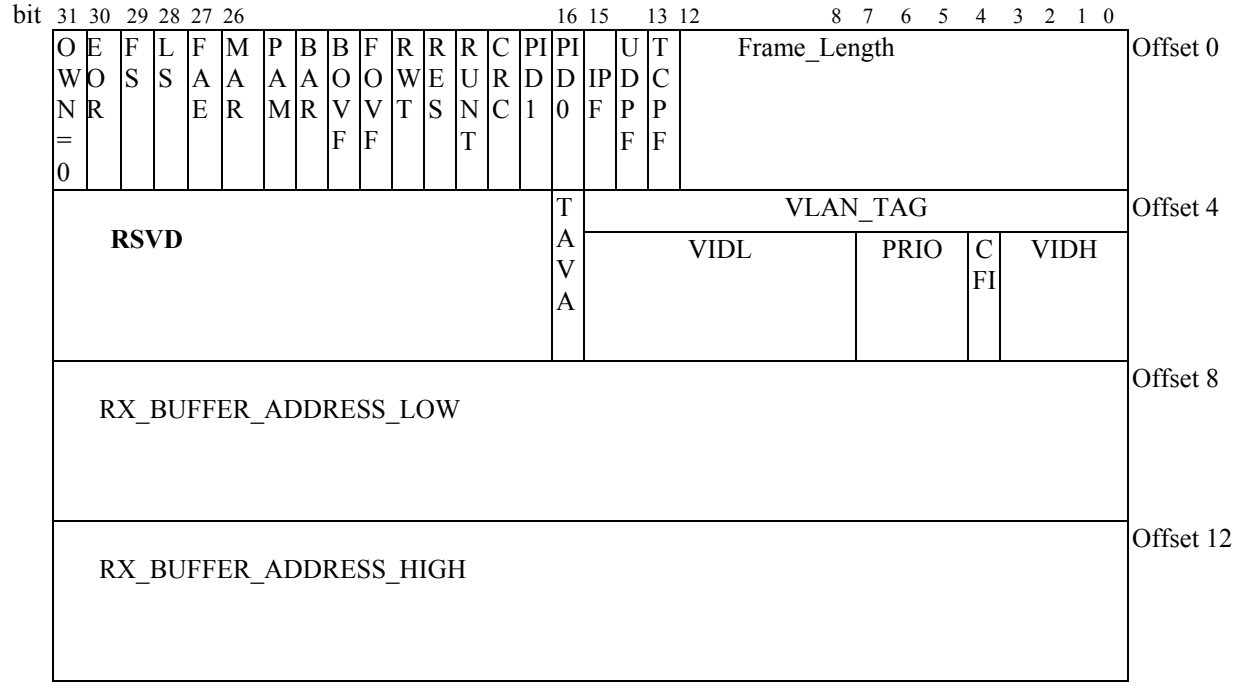
The driver should pre-allocate Rx buffers and configure Rx descriptors before packet reception. The following describes what a Rx descriptor may look like before packet reception.



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, indicates that the descriptor is owned by the NIC, and is ready to receive a packet. The OWN bit is set by the driver after having pre-allocated a buffer at initialization, or the host has released the buffer to the driver. In this case, OWN=1.
0	30	EOR	**End of Rx descriptor Ring:** Set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the internal receive descriptor pointer of the NIC reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29-13	RSVD	**Reserved**
0	12-0	Buffer_Size	**Buffer Size:** This field indicates the receive buffer size in bytes. Although the maximum buffer size is 8K bytes/buffer, the RTL8139C(L)+ purges all data after 4K bytes if the packet is larger than 4K-bytes long.
4	31-17	RSEV	**Reserved**
4	16	TAVA	**Tag Available:** When set, the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.
4	15-0	VLAN_TAG	If the TAG of the packet is 0x8100, The MAC of the RTL8139C(L)+ extracts four bytes from the after source ID, sets the TAVA bit to1, and moves the TAG value to this field in the Rx descriptor. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	RxBuffL	**Low 32-bit Address of Receive Buffer**
12	31-0	RxBuffH	High 32-bit address of receive buffer.

Rx Status Descriptor (OWN=0)

When a packet is received, the Rx command descriptor turns into a Rx status descriptor.



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, indicates that the descriptor is owned by the NIC. When cleared, indicates that the descriptor is owned by the host system. The NIC clears this bit when it has filled up this Rx buffer with a packet or part of a packet. In this case, OWN=0.
0	30	EOR	**End of Rx Descriptor Ring:** Set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. When the internal receive descriptor pointer of the NIC reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29	FS	**First Segment Descriptor:** When set, indicates that this is the first descriptor of a received packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last Segment Descriptor:** When set, indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.
0	27	FAE	**Frame Alignment Error:** When set, indicates a frame alignment error has occurred on the received packet. FAE packets can be received only when RCR_AER is set.
0	26	MAR	**Multicast Address Packet Received:** When set, indicates that a multicast packet has been received.
0	25	PAM	**Physical Address Matched:** When set, indicates that the destination address of this Rx packet matches the value in the ID registers of the RTL8139C(L)+.
0	24	BAR	**Broadcast Address Received:** When set, indicates that a broadcast packet has been received. BAR and MAR will not be set simultaneously.
0	23	BOVF	**Buffer Overflow:** When set, indicates that receive buffer has been exhausted before this packet was received.
0	22	FOVF	**FIFO Overflow:** When set, indicates that a FIFO overflow has occurred before this packet was received.
0	21	RWT	**Receive Watchdog Timer Expired:** When set, indicates that the received packet length exceeds 4096 bytes. The receive watchdog timer will expire and stop the receiving engine. (Same as the Long Bit definition in 8139a)
0	20	RES	**Receive Error Summary:** When set, indicates that at least one of the following errors has occurred: CRC, RUNT, RWT, FAE. This bit is valid only when the LS (Last Segment) bit is set.

<table>
<tr><td>0</td><td>19</td><td>RUNT</td><td>Runt Packet: When set, indicates that the received packet length is smaller than 64 bytes. RUNT packets can be received only when RCR_AR is set.</td></tr>
<tr><td>0</td><td>18</td><td>CRC</td><td>CRC Error: When set, indicates that a CRC error has occurred on the received packet. CRC packets can be received only when RCR_AER is set.</td></tr>
<tr><td>0</td><td>17, 16</td><td>PID1, PID0</td><td>Protocol ID1, Protocol ID0: These 2 bits indicate the protocol type of the packet received.
<table>
<tr><td></td><td>PID1</td><td>PID0</td></tr>
<tr><td>Non-IP</td><td>0</td><td>0</td></tr>
<tr><td>TCP/IP</td><td>0</td><td>1</td></tr>
<tr><td>UDP/IP</td><td>1</td><td>0</td></tr>
<tr><td>IP</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>0</td><td>15</td><td>IPF</td><td>When set, indicates IP checksum failure.</td></tr>
<tr><td>0</td><td>14</td><td>UDPF</td><td>When set, indicates UDP checksum failure.</td></tr>
<tr><td>0</td><td>13</td><td>TCPF</td><td>When set, indicates TCP checksum failure.</td></tr>
<tr><td>0</td><td>12-0</td><td>Frame_Length</td><td>When OWN=0 and LS =1, it indicates the received packet length including CRC, in bytes.</td></tr>
<tr><td>4</td><td>31-17</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>4</td><td>16</td><td>TAVA</td><td>Tag Available: When set, the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.</td></tr>
<tr><td>4</td><td>15-0</td><td>VLAN_TAG</td><td>If the packet ‘s TAG is 0x8100, The RTL8139C(L)+’s MAC extracts four bytes from after source ID, sets TAVA bit to1, and moves the TAG value to this field in Rx descriptor.
VIDH: The high 4 bits of a 12-bit VLAN ID.
VIDL: The low 8 bits of a 12-bit VLAN ID.
PRIO: 3-bit 8-level priority.
CFI: Canonical Format Indicator.</td></tr>
<tr><td>8</td><td>31-0</td><td>RxBuffL</td><td>Low 32-bit Address of Receive Buffer</td></tr>
<tr><td>12</td><td>31-0</td><td>RxBuffH</td><td>High 32-bit Address of Receive Buffer</td></tr>
</table>

9.3 Line Quality Monitor

The line quality monitor function is available in 100Base-TX mode. It is possible to determine the amount of Equalization being used by accessing certain test registers. This provides a crude indication of connected cable length. This function allows for a quick and simple verification of the line quality in that any significant deviation from an expected register value (based on a known cable length) would indicate that the signal quality has deviated from the expected nominal case.

9.4 Clock Recovery Module

The Clock Recovery Module (CRM) is supported in both 10Base-T and 100Base-TX mode. The CRM accepts 125Mb/s MLT3 data from the equalizer. The DPLL locks onto the 125Mb/s data stream and extracts a 125MHz recovered clock. The extracted and synchronized clock and data are used as required by the synchronous receive operations.

9.5 Loopback Operation

Loopback mode is normally used to verify that the logic operations up to the Ethernet cable function correctly. In loopback mode for 100Mbps, the RTL8139C(L)+ takes frames from the transmit descriptor and transmits them up to internal Twister logic. The loopback function does not apply to external PHYceiver.

9.6 Tx Encapsulation with the Internal PHYceiver

While operating in 100Base-Tx mode, the RTL8139C(L)+ encapsulates the frames that it transmits according to the 4B/5B code-groups table. The changes of the original packet data are listed as follows:

1. The first byte of the preamble in the MAC frame is replaced with the JK symbol pair.
2. After the CRC, the TR symbol pair is inserted.

9.7 Collision

If the RTL8139C(L)+ is not in the full-duplex mode, a collision event occurs when the receive input is not idle while the RTL8139C(L)+ transmits. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble (including the JK symbol pair).

9.8 Rx Decapsulation with the Internal PHYceiver

The RTL8139C(L)+ continuously monitors the network when reception is enabled. When activity is recognized it starts to process the incoming data.

After detecting receive activity on the line, the RTL8139C(L)+ starts to process the preamble bytes based on the mode of operation.

While operating in 100Base-Tx mode, the RTL8139C(L)+ expects the frame to start with the symbol pair JK in the first bye of the 8-byte preamble.

The RTL8139C(L)+ checks the CRC bytes and checks if the packet data ends with the TR symbol pair, if not, the RTL8139C(L)+ reports an CRC error RSR.

The RTL8139C(L)+ reports a RSR<CRC> error in the following case:

In 100Base-Tx mode, one of the following occurs:

a. An invalid symbol (4B/5B Table) is received in the middle of the frame.
The RSR<ISE> bit also sets.

b. The frame does not end with the TR symbol pair.

9.9 Flow Control

The RTL8139C(L)+ supports IEEE802.3X flow control to improve performance in full-duplex mode. It detects PAUSE packets to achieve flow control tasks.

9.9.1. Control Frame Transmission

When the RTL8139C(L)+, configured in C mode, detects that its free receive buffer less than 3K bytes, it sends a PAUSE packet with pause_time(=FFFFh) to inform the source station to stop transmission for the specified period of time. After the driver has processed the packets in the receive buffer and updated the boundary pointer, the RTL8139C(L)+ sends the another PAUSE packet with pause_time(=0000h) to wake up the source station to restart transmission.

When the RTL8139C(L)+ is configured in C+ mode with Tx Flow Control enabled, it sends out a PAUSE packet with pause time = FFFFh, whenever there are no free Rx descriptors available.

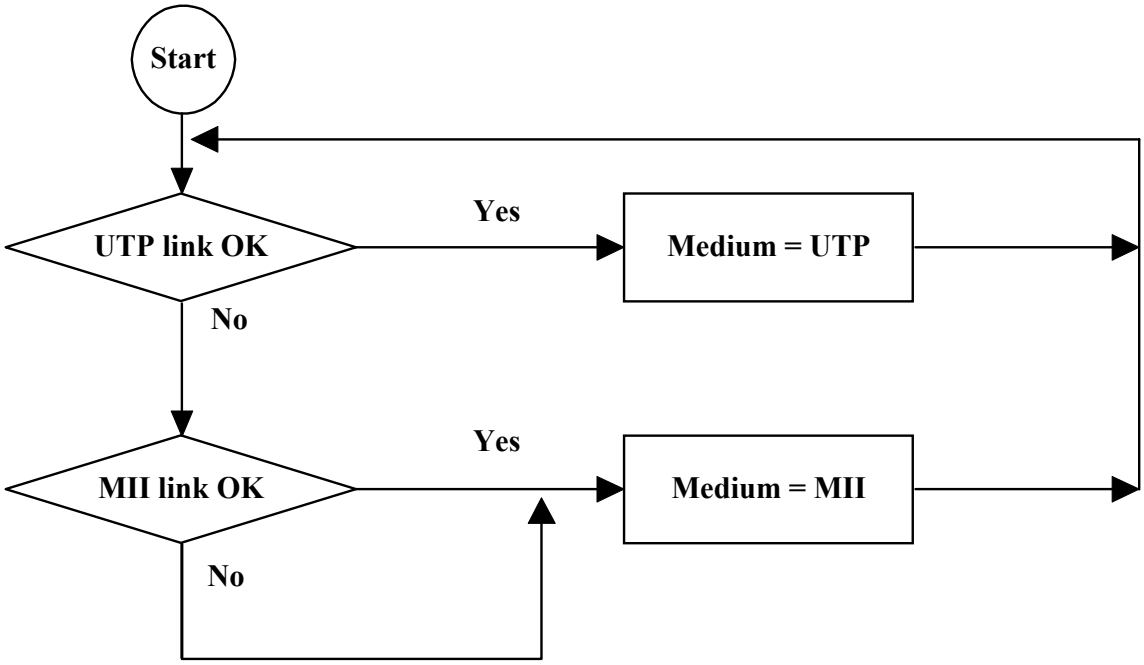
9.9.2. Control Frame Reception

The RTL8139C(L)+ enters a backoff state for a specified period of time when it receives a valid PAUSE packet with pause_time (=n). If the PAUSE packet is received while the RTL8139C(L)+ is transmitting, the RTL8139C(L)+ starts to backoff after the current transmission completes. The RTL8139C(L)+ is free to transmit the next packet when it receives a valid PAUSE packet with pause_time(=0000h) or the backoff timer(=n*512 bit time) elapses.

Note: The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. a PAUSE packet). The N-way flow control capability can be disabled, please refer to Section 7, “EEPROM (93C46 or 93C56) Contents” for a detailed description.

9.10 Medium Auto-Detect
(UTP or MII, no Boot ROM interface)

The following diagram describes the process the RTL8139C(L)+ uses to detect the medium used.



9.11 Cable Connection Status

- For medium status from an external PHYceiver (MII application enabled, no Boot ROM) to be reported correctly, the MLINK (pin 102) and MFDUP (pin 103) pins should be connected to relative pins of the external PHYceiver.
- The status of Link Speed and Duplex mode are reflected to the relative registers when the current medium is either UTP or MII (MII application enabled).
- Link change from current LinkOk medium generates an interrupt (LinkChg, bit5, ISR) to notify the drivers of link change event.
- Force Link Speed function is effective only to RTL8139C(L)+'s internal PHYceiver. The RTL8139C(L)+ does not support hardware access to external PHYceiver's MII registers in MII application. The only way to force link speed of external PHYceiver, is to use software generated MII timing through MII register (Offset FCh, when medium select is set to Auto-Detect or MII mode).

1. UTP: Same as the RTL8139 series.
2. MII:

   The information reflects the medium status from external PHYceiver, provided that the MLINK and MFDUP are both connected to the relative pins of the external PHYceiver.

   Link: by MLINK pin 102

   If MLinkP (bit3, BMCR, offset 63h) = 1, then MLink=high means MII link OK

   If MLinkP (bit3, BMCR, offset 63h) = 0, then MLink=low means MII link OK

   MLinkP can be auto-loaded from EEPROM.

   Duplex: by MFDUP pin 101

   If MDupP (bit2, BMCR, offset 63h) = 1, then MFDup=high means MII Duplex=Full

   If MDupP (bit2, BMCR, offset 63h) = 0, then MFDup=low means MII Duplex=Full

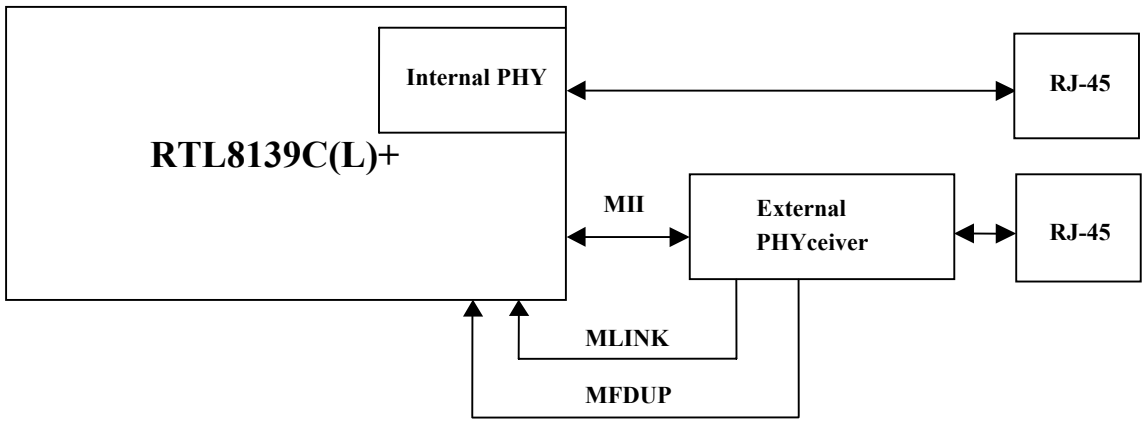
   MDupP can be auto-loaded from EEPROM.

   Speed: by MTXC

   If MTXC = 2.5MHz, then Speed=10Mbps. If MTXC = 25MHz, Speed=100Mbps.

9.12 MII Redundant Link

The following diagram shows the process used by the RTL8139C(L)+ to implement the MII redundant link feature. This feature is valid only in MII applications only.



9.13 Memory Functions

9.13.1 Memory Read Line (MRL)

The Memory Read Line command reads information from a longword (DWORD) up to cache line boundary in size into a prefetchable address space. The Memory Read Line command is semantically identical to the Memory Read command except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by reading up to a cache line boundary in response to the request, rather than a single memory cycle. As with the Memory Read command, pre-fetched buffers must be invalidated before any synchronization events are passed through this access path.

The RTL8139C(L)+ performs the MRL process according to the following rules:

i. Read accesses that reach the cache line boundary use the Memory Read Line (MRL) command, instead of Memory Read command.
ii. Read accesses that do not reach the cache line boundary use the Memory Read (MR) command.
iii. The Memory Read Line (MRL) command operates in conjunction with the Memory Read Multiple (MRM) command.
iv. The RTL8139C(L)+ will terminate the read transaction on to the cache line boundary when it is out of resources on the transmit DMA. For example, when the transmit FIFO is almost full.

9.13.2 Memory Read Multiple (MRM)

The Memory Read Multiple command is semantically identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The memory controller should continue pipelining memory requests as long as FRAMEB is asserted. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by sequentially reading ahead one or more additional cache line(s) when a software transparent buffer is available for temporary storage.

The RTL8139C(L)+ performs the MRM process according to the following rules:

i. When the RTL8139C(L)+ reads full cache lines, it will use the Memory Read Multiple command.
ii. If the memory buffer is not cache-aligned, the RTL8139C(L)+ will use Memory Read Line command to reach the cache line boundary first.

Example:

Assume the packet length = 1514 byte, cache line size = 16 longwords (DWORDs), and Tx buffer start address = 64m+4 (m > 0).

;Step1: Memory Read Line (MRL)
;Data: (0-3) => (4-7) => (8-11) =>……... => (56-59) (byte offset of the Tx packet)
;From Address: <64m+4>, <64m+8>, ……., <64m+60> (reach cache line boundary)
;Step2. Memory Read Multiple (MRM)
;Data: (60-63) => (64-67) => (68-71) => ……... => (1454-1467)
;From Address: <64m+64>, <64m+68>, ……., <64m+64+(16*4)*21+(16-1)*4>
;Step3. Memory Read(MR)
;Data: (1468-1471) => (1472-1475) => ……, => (1510-1513)
;From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>
Step1: Memory Read Multiple (MRM)
Data: (0-3) => (4-7) => (8-11) =>…….. => (1454-1467)
From Address: <64m+4>, <64m+8>, ……., <64m+64+(16*4)*21+(16-1)*4>
Step2. Memory Read(MRL)
Data: (1468-1471) => (1472-1475) => ……, => (1510-1513)
From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>

9.13.3 Memory Write and Invalidate (MWI)

The Memory Write and Invalidate command is semantically identical to the Memory Write command except that it additionally guarantees a minimum transfer of one complete cache line. For example, the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. Note that all byte enables must be asserted during each data phase for this command.

The master may allow the transaction to cross a cache line boundary only if it intends to transfer the entire next line as well. This command requires implementation of a configuration register in the master indicating the cache line size and may only be used with Linear Burst Ordering. It allows a memory performance optimization by invalidating a "dirty" line in a write-back cache without requiring the actual write-back cycle, thus shortening access time. The RTL8139C(L)+ uses the MWI command while writing full cache lines, and the Memory Write command while writing partial cache lines.

When the following requirements are met, the RTL8139C(L)+ issues the MWI command instead of the MW command on Rx DMA:

i. The Cache Line Size written in the offset 0Ch of the PCI configuration space is 8 or 16 longwords (DWORDs).
ii. The accessed address is cache line aligned.
iii. The RTL8139C(L)+ has at least 8/16 longwords (DWORDs) of data in its RX FIFO.
iv. The MWI (bit 4) in the PCI configuration command register should be set to 1.

The RTL8139C(L)+ uses the Memory Write (MW) command instead of MWI whenever any one of the above listed requirements fails. The RTL8139C(L)+ terminates the WMI cycle at the end of the cache line when a WMI cycle has started and at least one of the requirements are no longer valid.

Example:

Assume Rx packet length = 1514 byte, cache line size = 16 DWORDs (longwords), and Rx buffer start address = 64m+4 (m > 0).

Step1: Memory Write (MW)
Data: (0-3) => (4-7) => (8-11) => ……... => (56-59) (byte offset of the Rx packet)
To Address: <64m+4>, <64m+8>, ……., <64m+60> (reach cache line boundary)
Step2. Memory Write and Invalidate (MWI)
Data: (60-63) => (64-67) => (68-71) => ……..…..... => (1454-1457)
To Address: <64m+64>, <64m+68>, ……..…..., <64m+64+(16*4)*21+(16-1)*4>
Step3. Memory Write(MW)
Data: (1458-1461) => (1462-1465) => ……..…….... => (1512-1513)
To Address: <64m+64+(16*4)*22>, <64m+64+(16*4)*22+4>, , <64m+64+(16*4)*22+42>

9.13.4 Dual Address Cycle (DAC)

The Dual Address Cycle (DAC) command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is not in the low 4 GB address space. The RTL8139C(L)+ is capable of performing DAC, such that it is very competent as a network server card in a heavy-duty server with the possibility of allocating a memory buffer above the 4GB memory address space.

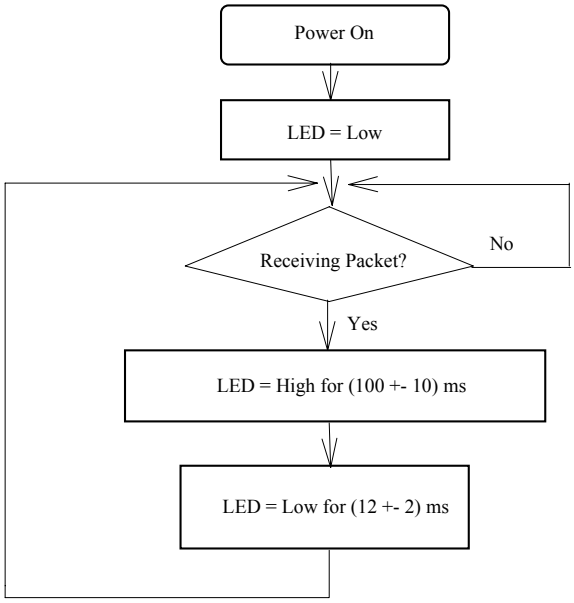
9.14 LED Functions

9.14.1 10/100 Mbps Link Monitor

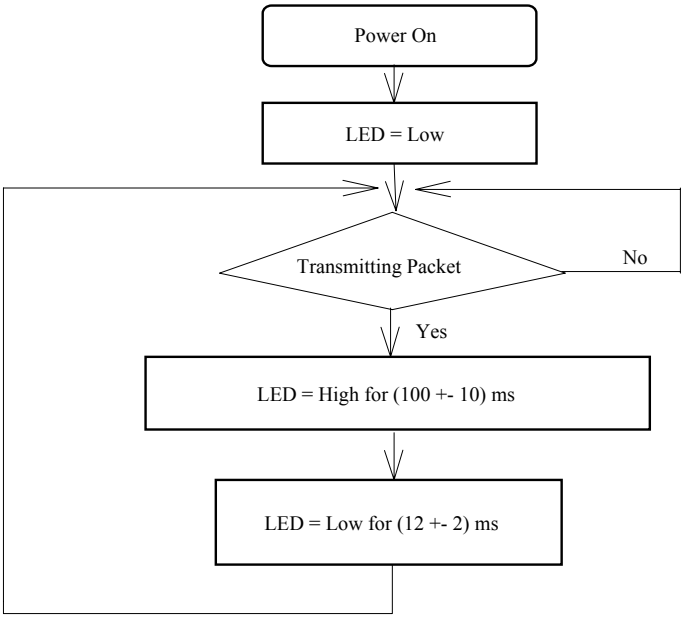
The Link Monitor senses the link integrity or if a station is down.

9.14.2 LED_RX

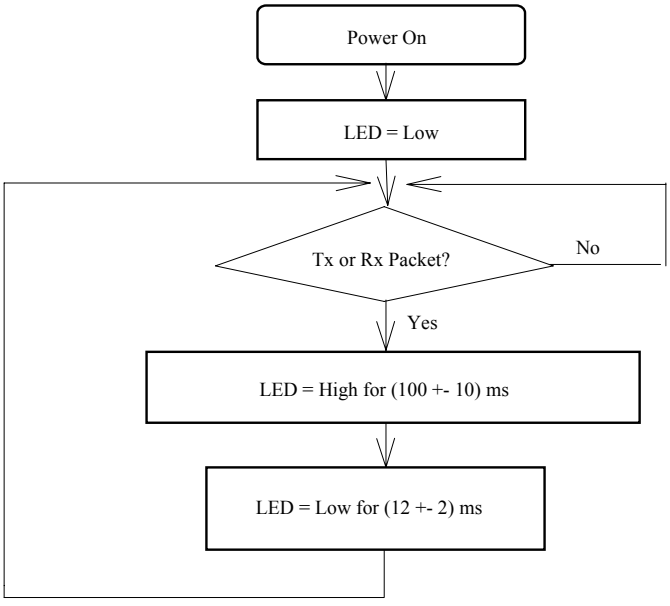
In 10/100 Mbps mode, the LED function is like that of the RTL8129.



9.14.3 LED_TX



9.14.4 LED_TX+LED_RX



9.15 Physical Layer Interfaces

The RTL8139C(L)+ supports standard media independent MII for 10Mbps and 100Mbps applications. In addition, a management interface is defined for MII.

9.15.1 Media Independent Interface (MII)

The RTL8139C(L)+ supports 10Mbps and 100Mbps physical layer devices through the MII as defined in the IEEE 802.3 (clause 22) specifications. The MII consists of a transmit data interface (TxEN, TxER, TXD[3:0], and TxCLK), a receive data interface (RxDV, RxER, RXD[3:0], and RxCLK), 2 status signals (CRS and COL) and a management interface (MDC and MDIO). In this mode of operation, both Transmit and Receive clocks are supplied by the PHY.

9.15.2 MII Management Interface

The MII management interface utilizes a communication protocol similar to a serial EEPROM. Signaling occurs on two signals: clock (MDC) and data (MDIO). This protocol provides capability for addressing up to 32 individual Physical Media Dependent (PMD) devices which share the same serial interface, and for addressing up to 32 16-bit read/write registers within each PMD. The MII management protocol utilizes the following frame format: start bits (SB), opcode (OP), PMD address (PA), register address (RA), line turnaround (LT) and data, as shown below.

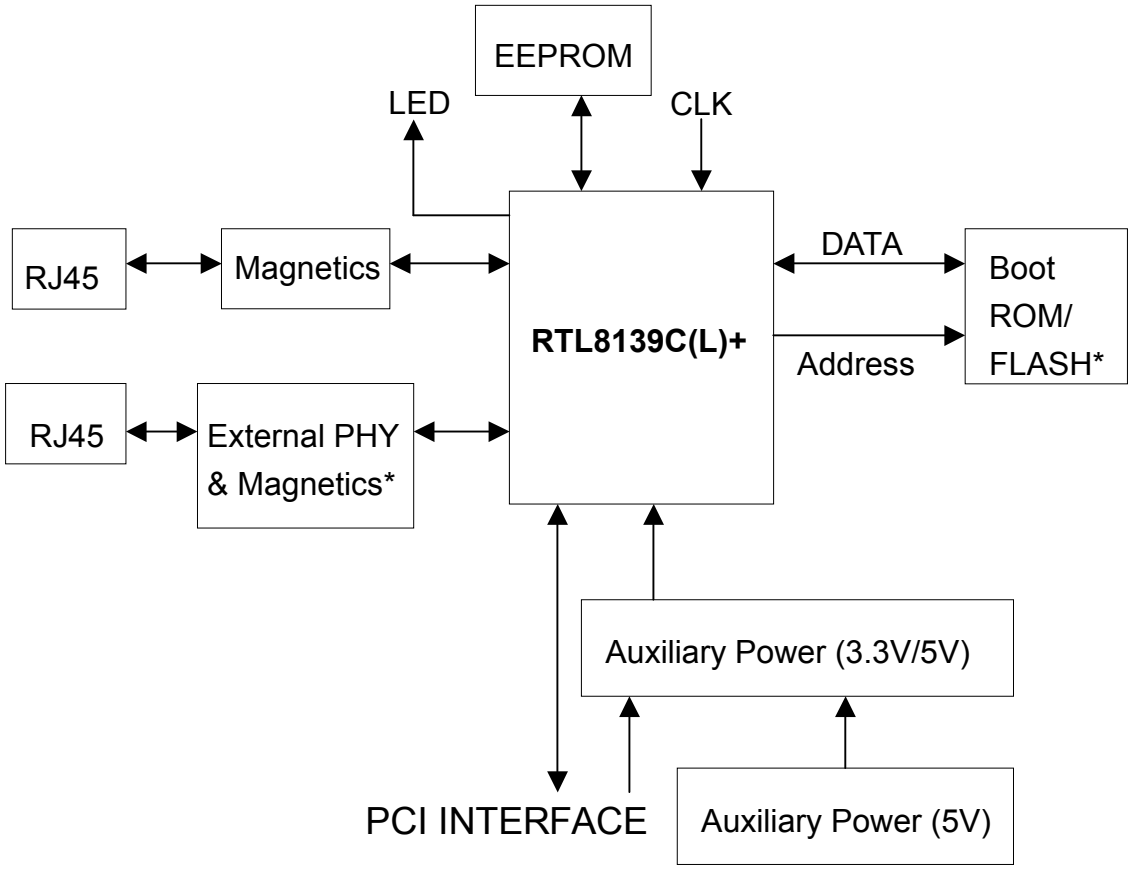
SB	OP	PA	RA	LT	Data
2 bits	2 bits	5 bits	5 bits	2 bits	16 bits

MII Management Frame Format

i. Start bits are defined as <01>.
ii. Opcode bits are defined as <01> for a Write access and <10> for a Read access.
iii. PMD address is the device address.
iv. Register address is address of the register within that device.
v. Line turnaround bits will be <10> for Write accesses and will be <xx> for Read accesses. This allows time for the MII lines to "turn around".
vi. Data is the 16 bits of data that will be written to or read from the PMD device.

A reset frame, defined as 32 consecutive 1s (FFFF FFFFh), is also provided. After power up, all MII PMD devices must wait for a reset frame to be received prior to participating in MII management communication. Additionally, a reset frame may be issued at any time to allow all connected PMDs to re-synchronize to the data traffic.

10. Application Diagram



* Boot ROM/FLASH and External PHY can not be implemented at the same time.

11. Electrical Characteristics

11.1 Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	°C
Operating temperature	0	70	°C

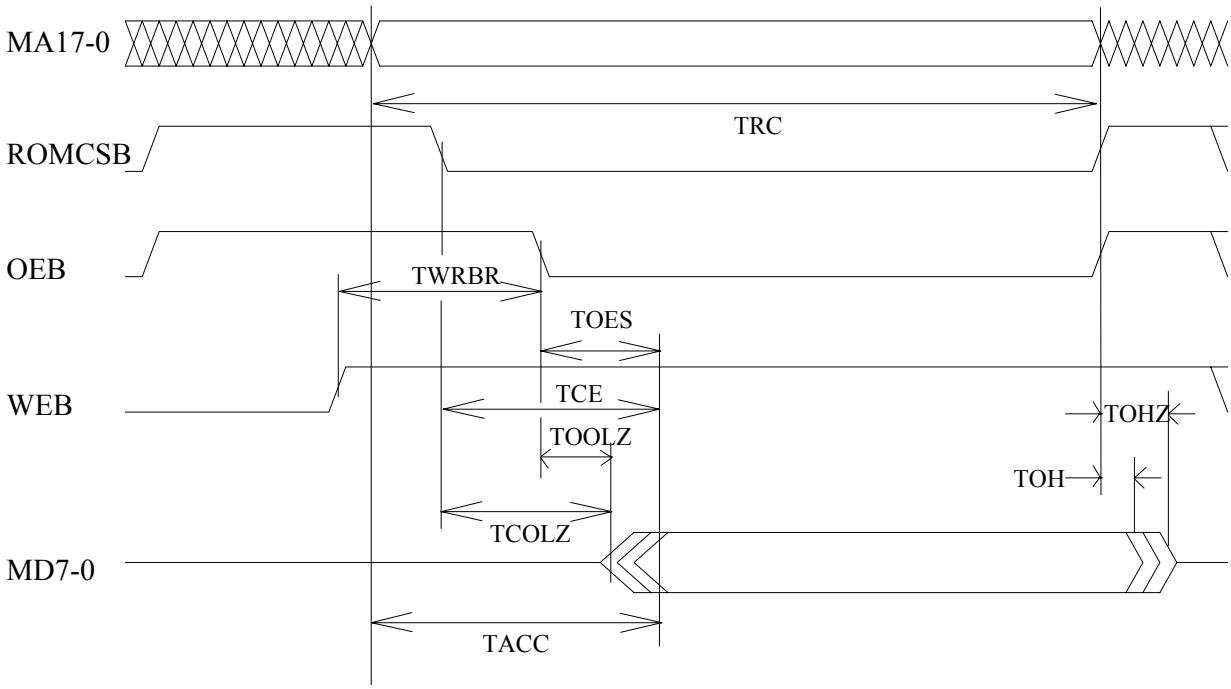
11.2 DC Characteristics

11.2.1 Supply Voltage
Vcc = 3.0V min. to 3.6V max.

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH}= -8mA	0.9 * Vcc	Vcc	V
V_{OL}	Maximum Low Level Output Voltage	I_{OL}= 8mA		0.1 * Vcc	V
V_{IH}	Minimum High Level Input Voltage		0.5 * Vcc	Vcc+0.5	V
V_{IL}	Maximum Low Level Input Voltage		-0.5	0.3 * Vcc	V
I_{IN}	Input Current	V_{IN}=V_{CC} or GND	-1.0	1.0	uA
I_{OZ}	Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND	-10	10	uA
I_{CC}	Average Operating Supply Current	I_{OUT}=0mA,		330	mA

11.3 AC Characteristics

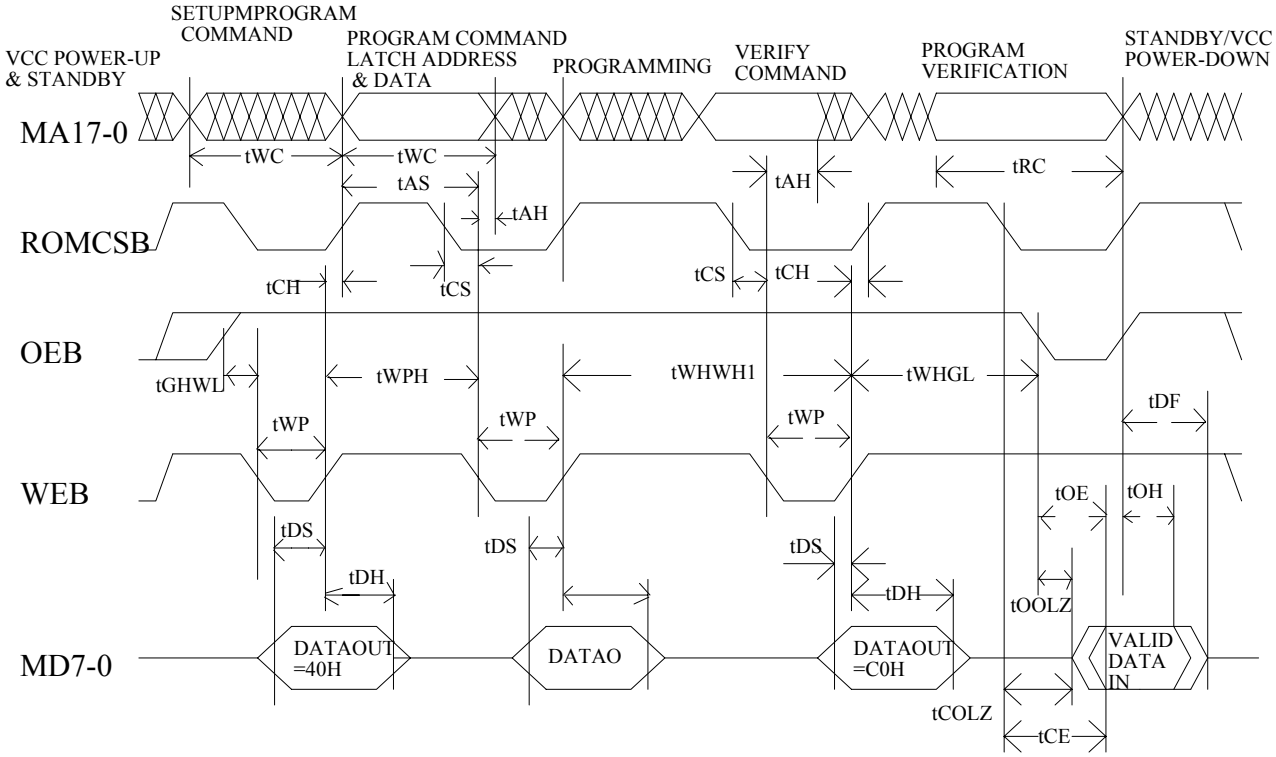
11.3.1 FLASH/BOOT ROM Timing



FLASH/BOOT ROM - Read

Symbol	Description	Minimum	Typical	Maximum	Units
TRC	Read Cycle	135	-	-	ns
TCE	Chip Enable Access Time	-	-	200	ns
TACC	Address Access Time	-	-	200	ns
TOES	Output Enable Access Time	-	-	60	ns
TCOLZ	Chip Enable to Output in Low Z	0	-	-	ns
TOOLZ	Output Enable to Output in Low Z	0	-	-	ns
TOHZ	Output Disable to Output in High Z	-	-	40	ns
TOH	Output Hold from Address, ROMCSB, or OEB	0	-	0	ns
TWRBR	Write Recovery time Before Read	6	-	-	us

FLASH/BOOT ROM – Read Table

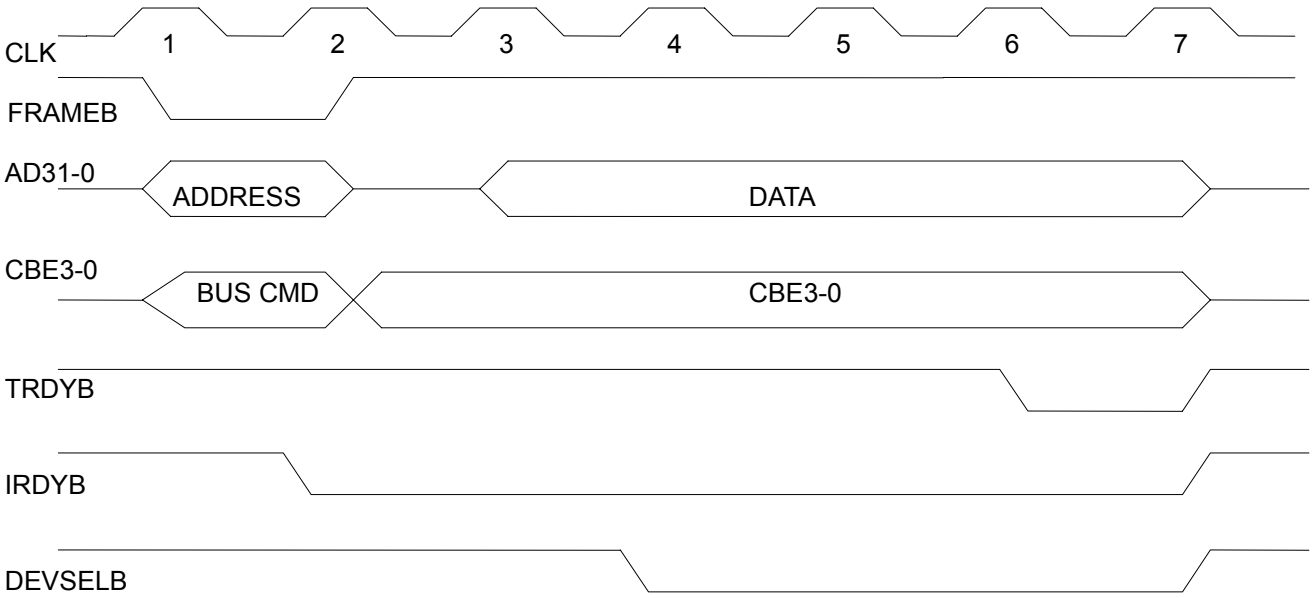


FLASH MEMORY – Write

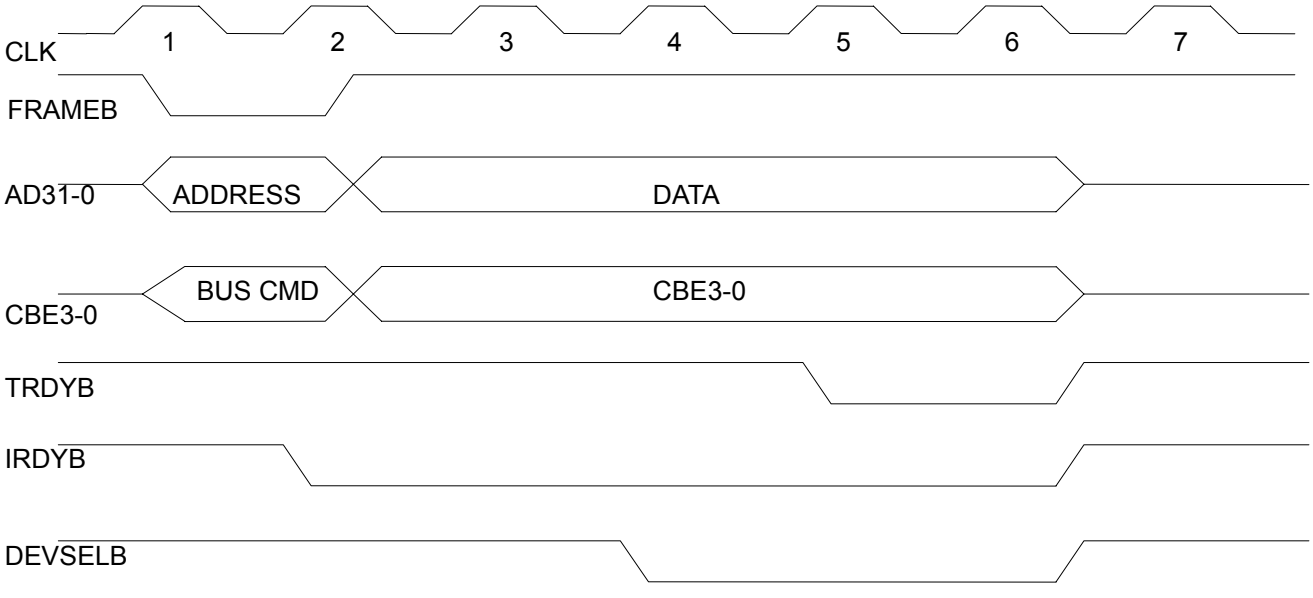
Symbol	Description	Minimum	Typical	Maximum	Units
TWC	Write Cycle Time	135	-	-	ns
TAS	Address Set-up Time	0	-	-	ns
TAH	Address Hold Time	60	-	-	ns
TDS	Data Set-up Time	50	-	-	ns
TDH	Data Hold Time	10	-	-	ns
TWHGL	Write Recovery Time before Read	6	-	-	us
TGHWL	Read Recovery Time before Write	0	-	-	us
TCS	Chip Enable Set-up Time before Write	20	-	-	ns
TCH	Chip Enable Hold Time	0	-	-	us
TWP	Write Pulse Width	50	-	-	ns
TWPH	Write Pulse Width High	20	-	-	ns
TWHWH1	Duration of Programming Operation	10	-	25	us

FLASH MEMORY – Write Table

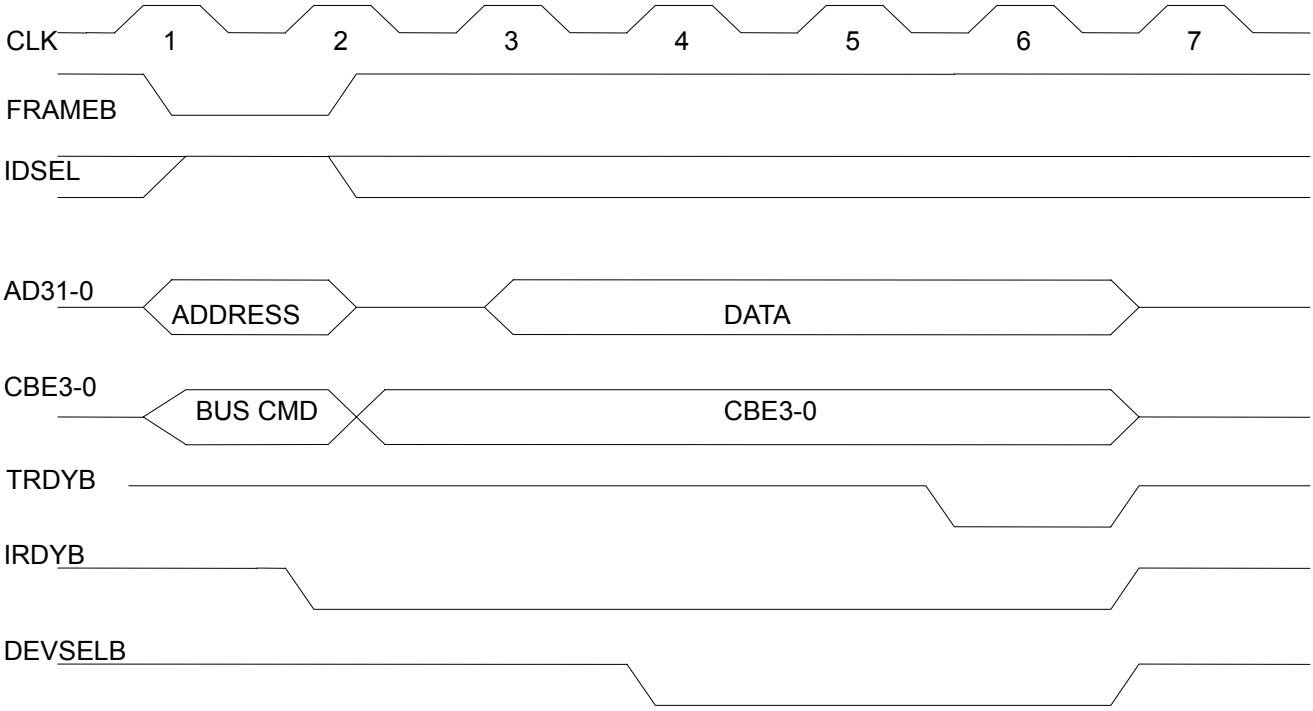
11.3.2 PCI Bus Operation Timing



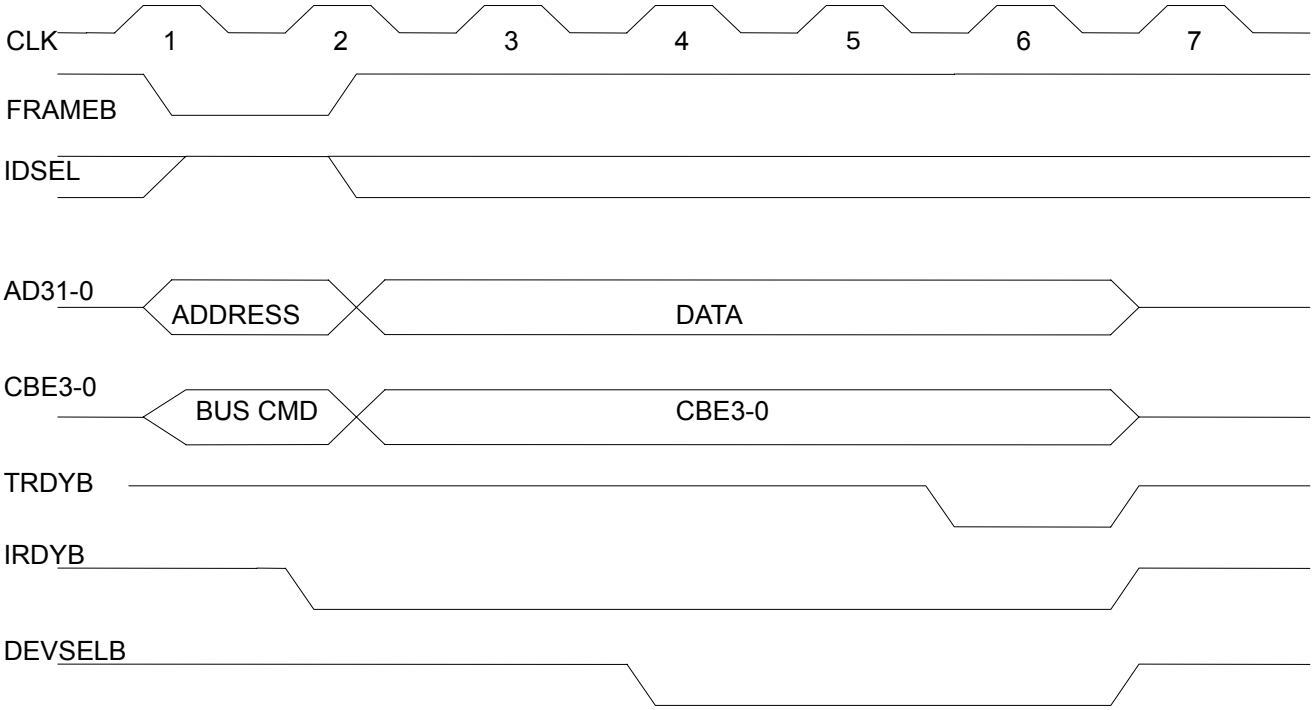
Target Read



Target Write

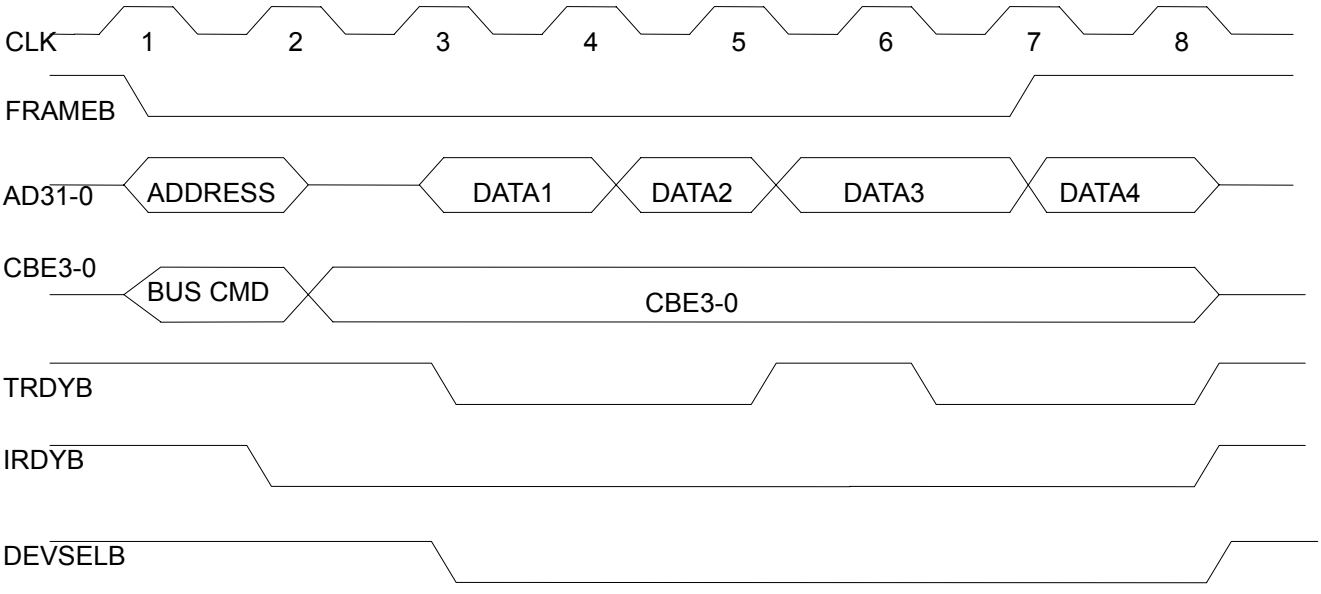


Configuration Read

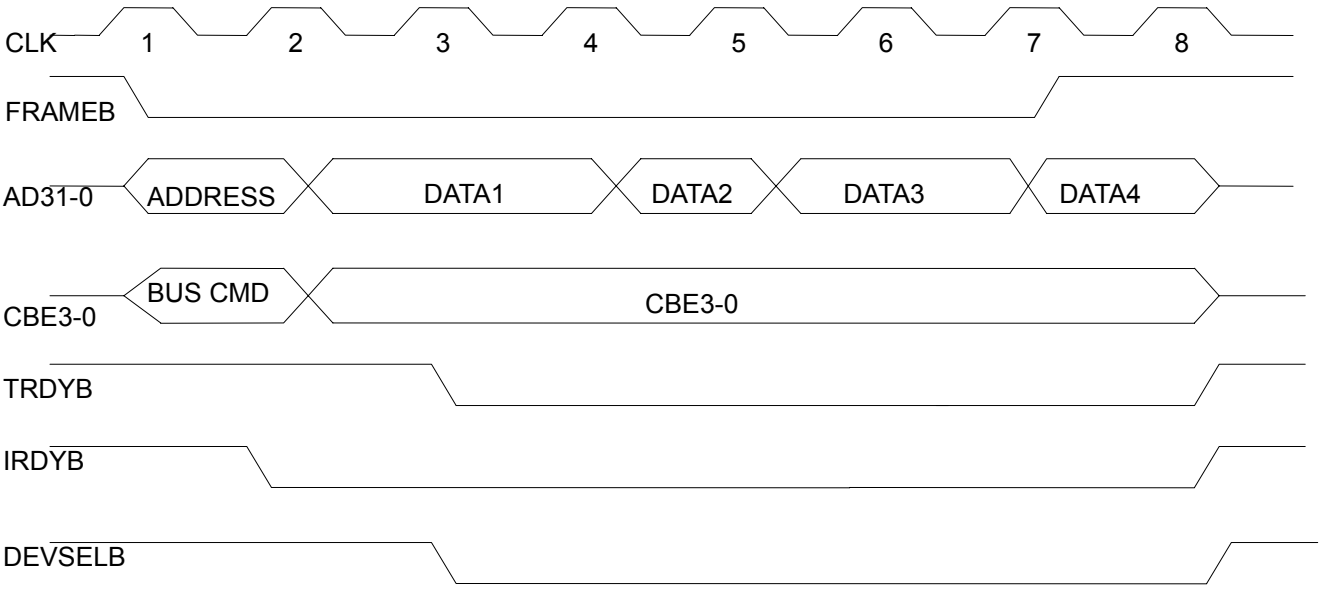


Configuration Write

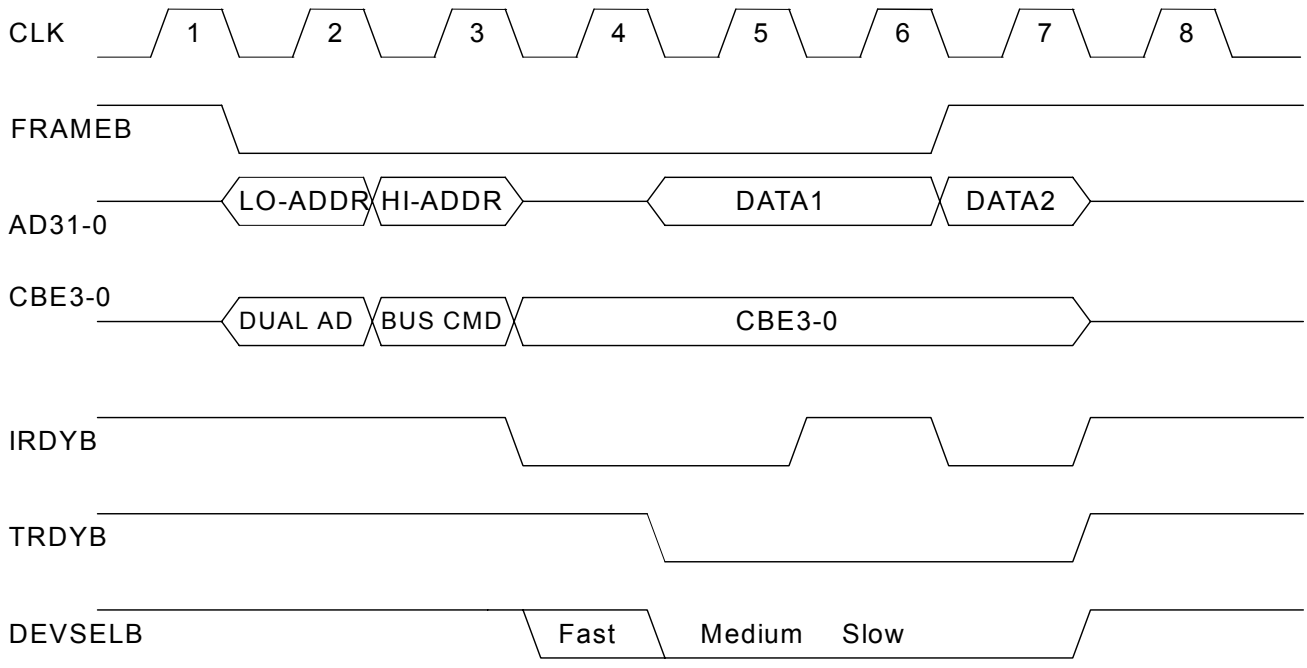
BUS Arbitration



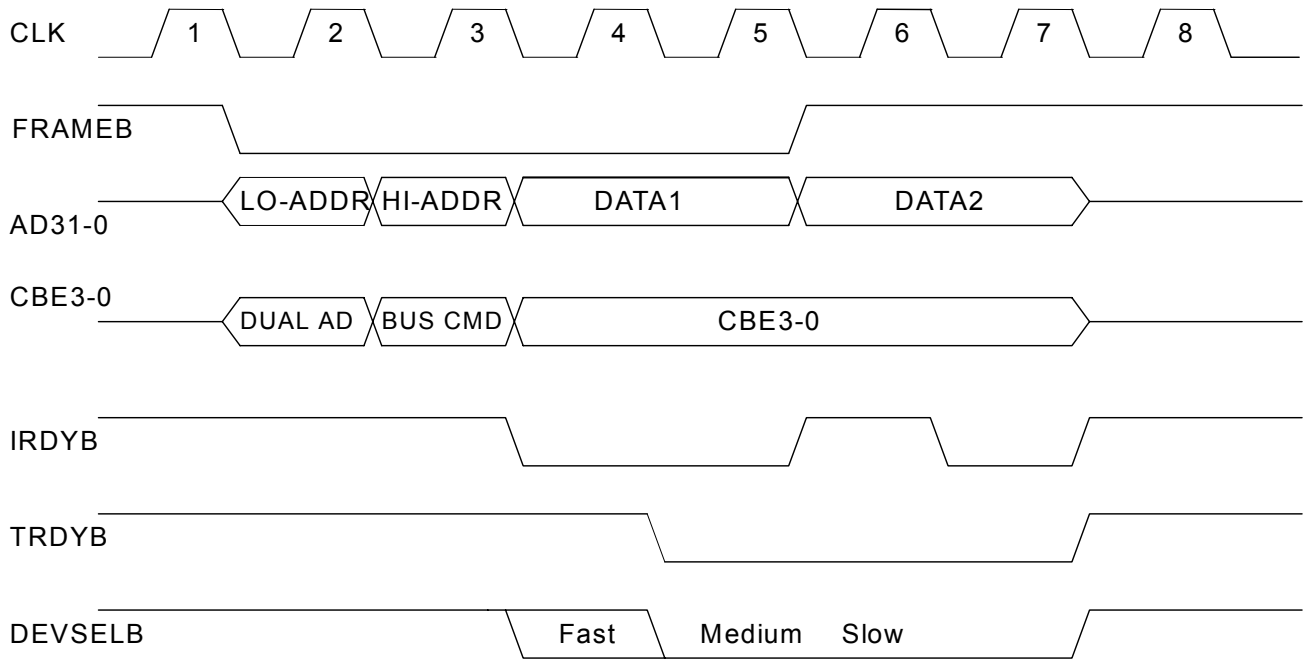
Memory Read



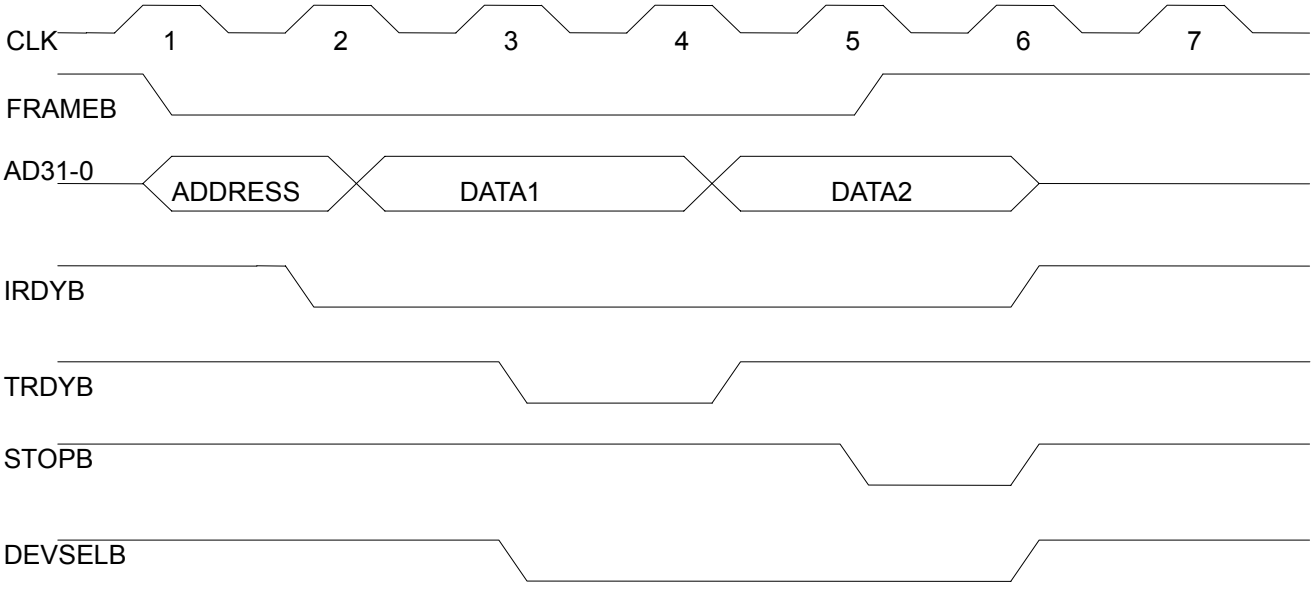
Memory Write



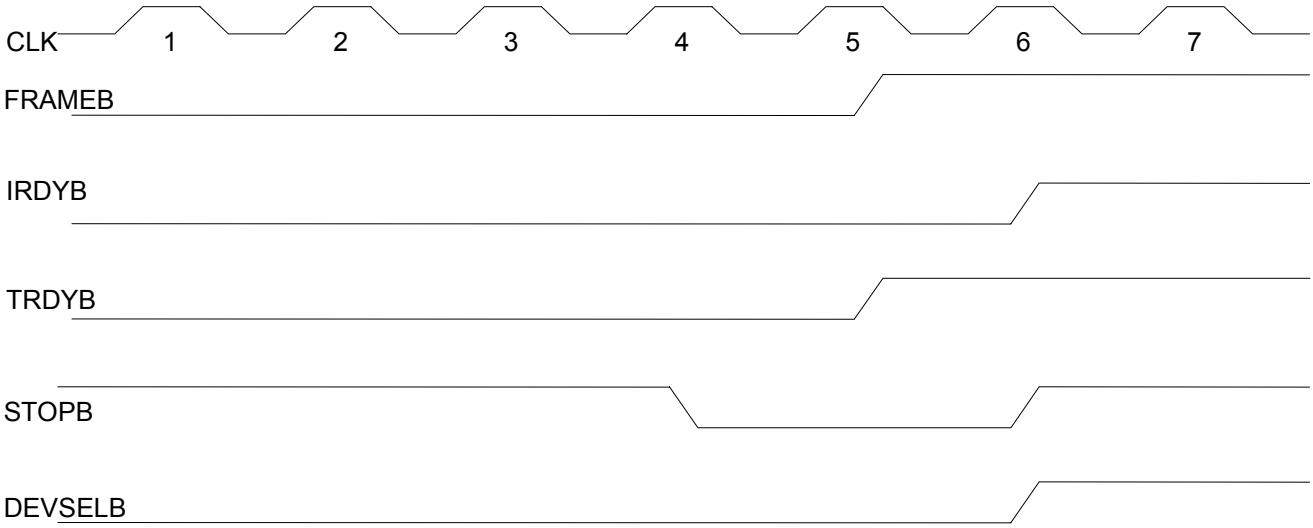
DAC Memory Read



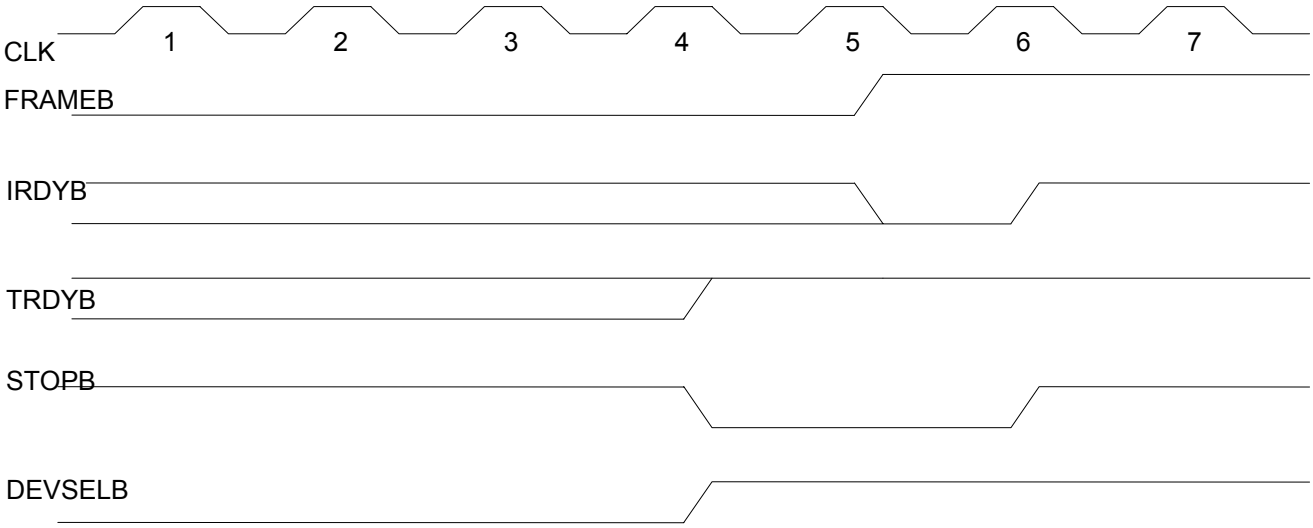
DAC Memory Write



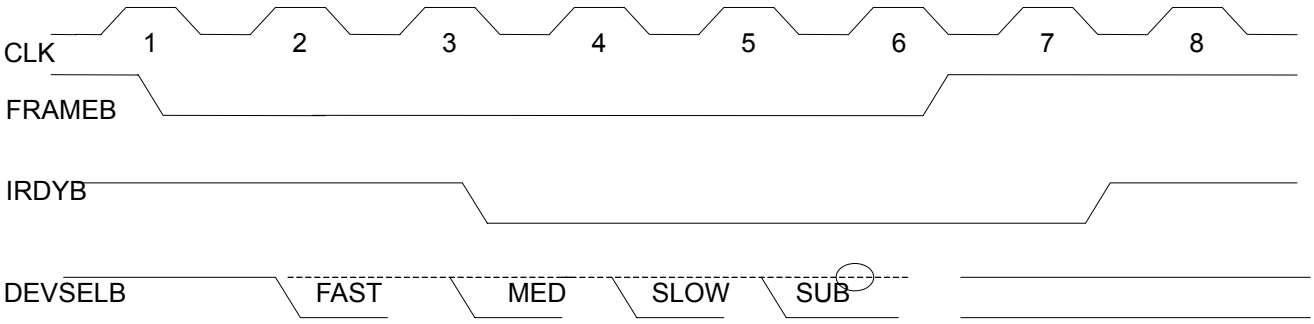
Target Initiated Termination - Retry



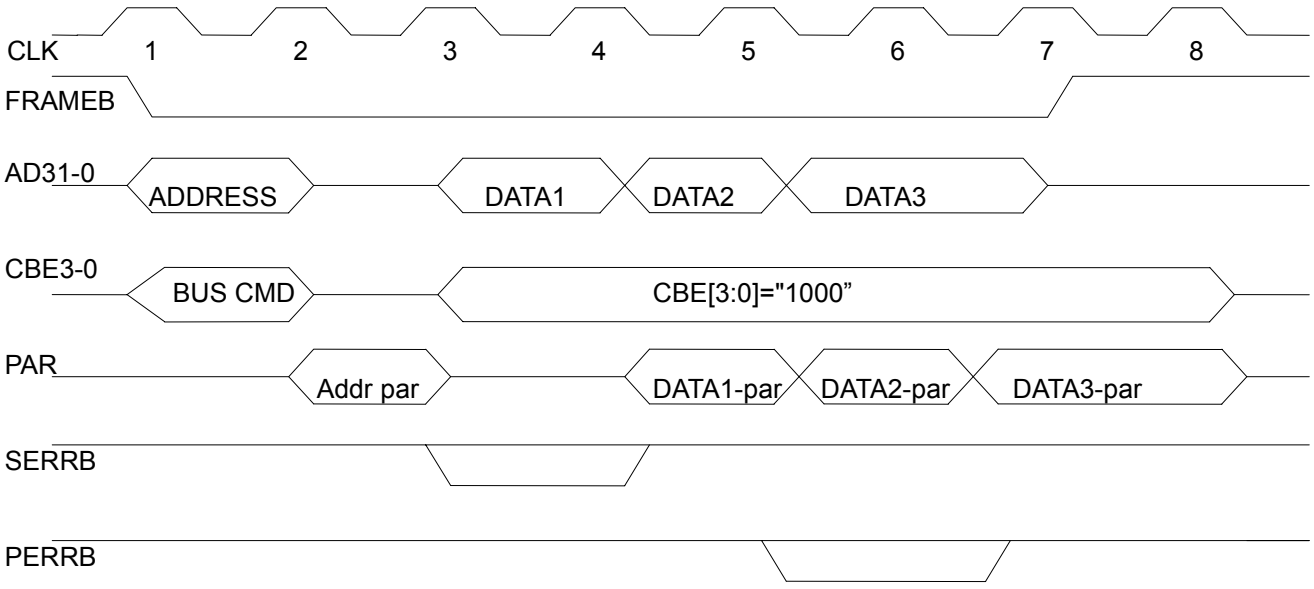
Target Initiated Termination - Disconnect



Target Initiated Termination - Abort

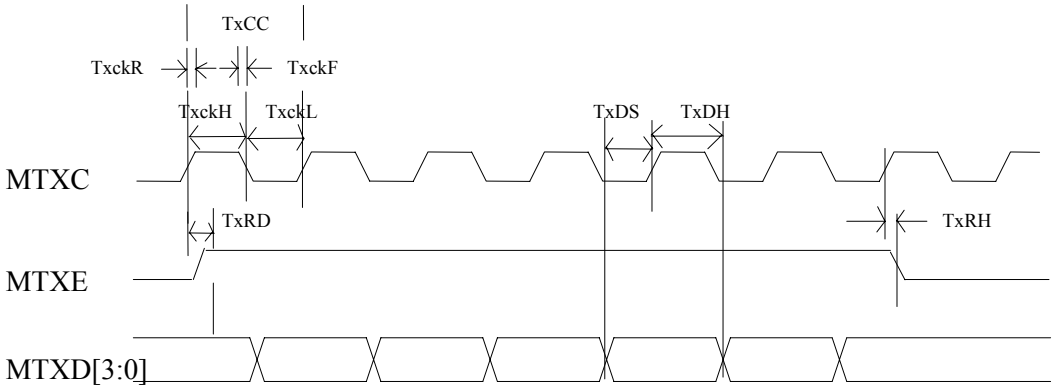


Master Initiated Termination - Abort



Parity Operation - One Example

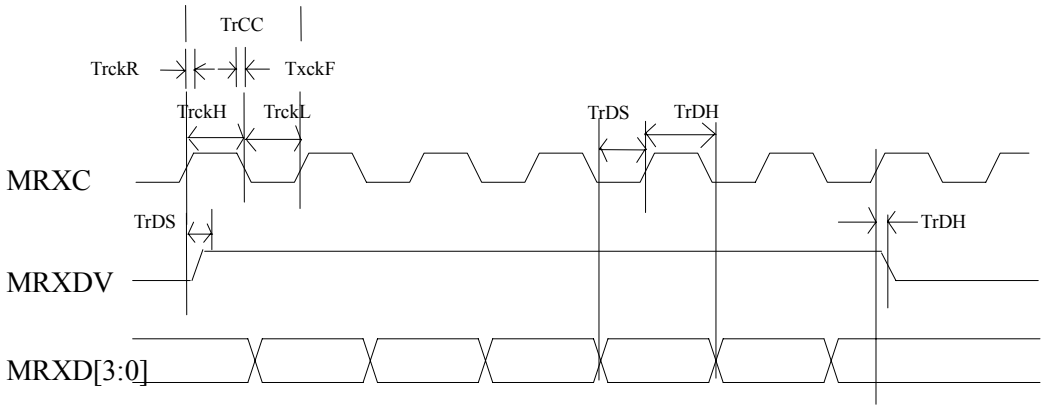
11.3.3 MII Timing



MII Port – Transmit

Symbol	Description	Minimum	Typical	Maximum	Units
TxCC	MTXC cycle	-	40	-	ns
TxckR	MTXC rise time	-	8	-	Ns
TxckF	MTXC fall time	-	8	-	Ns
TxckH	MTXC high time	14	-	26	Ns
TxckL	MTXC low time	14	-	26	Ns
TxDS	MTXD setup	-	-	10	Ns
TxDH	MTXD hold	10			Ns
TxRD	MTXC rise to MTXE valid time or MTXC rise to MTXD[3:0] valid time	-	-	12	Ns
TxRH	MTXD hold	5	-	-	Ns

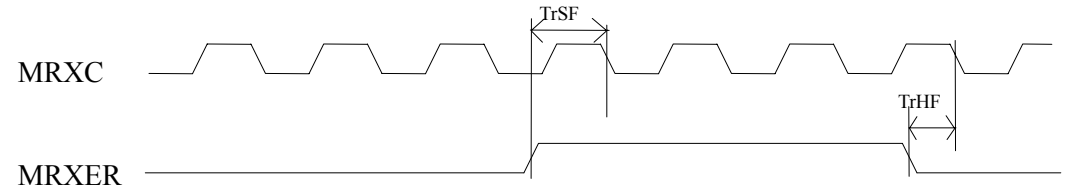
MII Port – Transmit Table



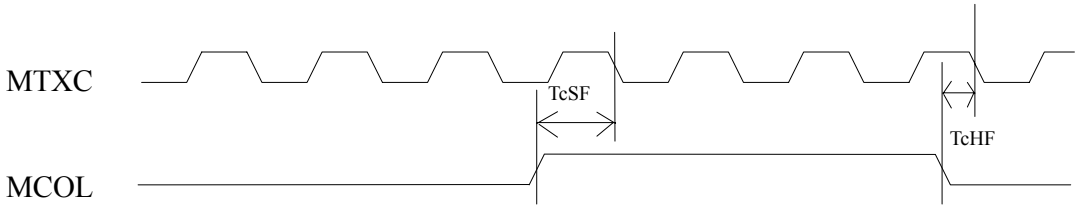
MII Port – Receive

Symbol	Description	Minimum	Typical	Maximum	Units
TrCC	MRXC cycle	-	40		ns
TrckR	MRXC rise time	-	8		ns
TrckF	MRXC fall time	-	8		ns
TrckH	MRXC high time	14	-	26	ns
TrckL	MRXC low time	14	-	26	ns
TrDS	MRXD[3:0] setup to MRXC rise time or MRXDV setup to MRXC rise time	10		-	ns
TrDH	MRXDV hold to after MRXC rise time or MRXD[3:0] hold to after MRXC rise time	10			ns

MII Port – Transmit Table



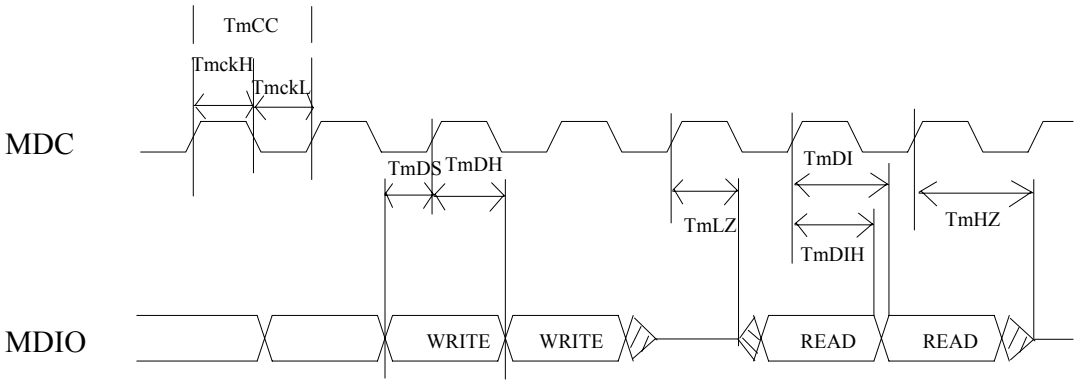
MII PORT - Receive Error



MII PORT - Carrier Sense and Collision

Symbol	Description	Minimum	Typical	Maximum	Units
TrSF/TcSF	MRXER (MCOL) setup to MRXC (MTXC) fall time	10	-	20	ns
TrHF/TcHF	MRXER (MCOL) hold to MRXC (MTXC) fall time	10	-	18	ns

MII PORT - Carrier Sense and Collision Table

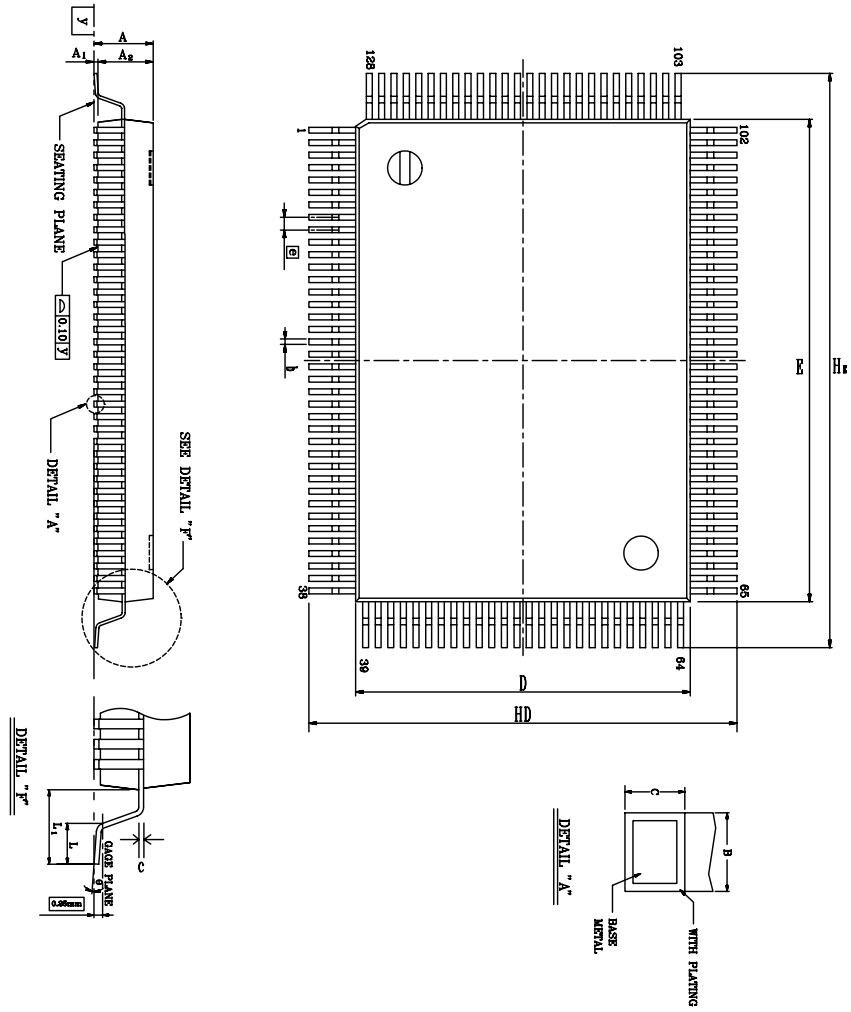


MII Management Port

Symbol	Description	Minimum	Typical	Maximum	Units
TmCC	MDC cycle time	50	-	-	ns
TmckH	MDC high time	25	-	-	ns
TmckL	MDC low time	25	-	-	ns
TmDS	MDIO set up (as output pin)	10	-	-	ns
TmDH	MDIO hold (as output pin)	5			ns
TmLZ	MDC rising clock to MDIO (as input pin) Low Impedance	-	-	40	ns
TmHZ	MDC rising clock to MDIO (as input pin) High Impedance	-	-	20	ns
TmDI	MDIO (as input pin) Valid from MDC rising edge	-	-	40	ns
TmDIH	MDIO (as input pin) hold from MDC rising edge	5			ns

MII Management Port Table

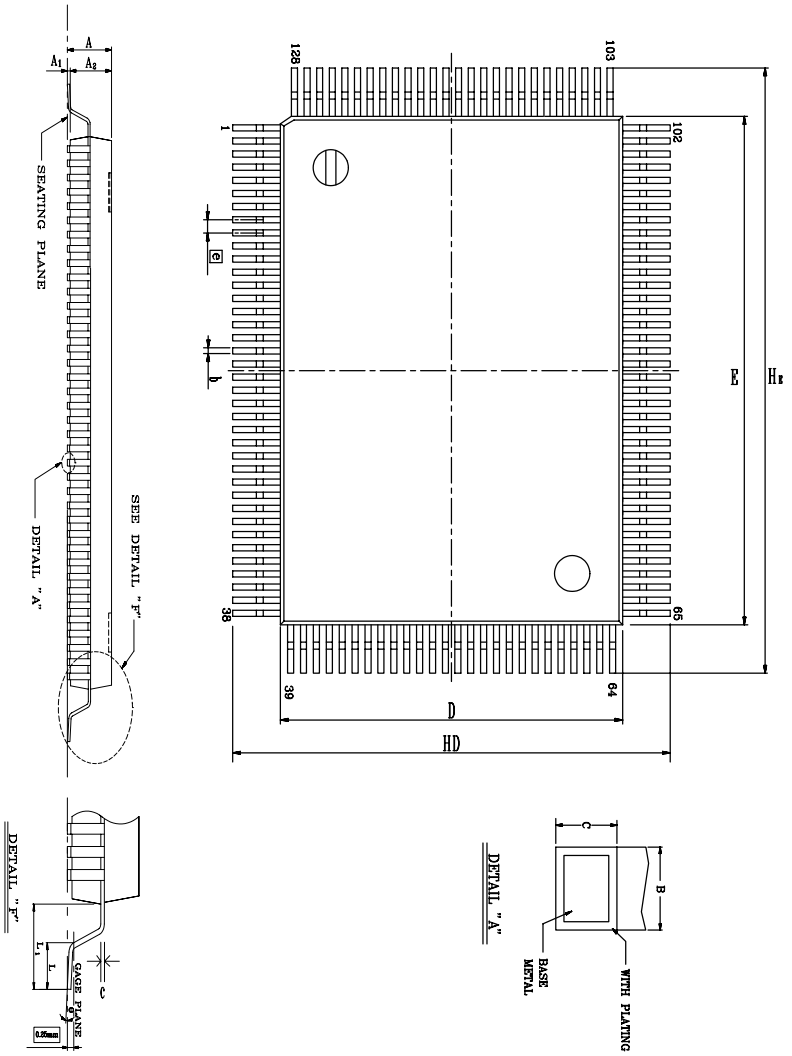
12. Mechanical Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE: **128 QFP** (14x20 mm) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	Nov. 4 1999
REALTEK SEMI-CONDUCTOR CO., LTD			



Symbol	Dimension in inch			Dimension in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	-	0.25
A2	0.051	0.055	0.059	1.30	**1.40**	1.50
b	0.006	0.009	0.011	0.15	**0.22**	0.29
c	0.004	-	0.006	0.09	-	0.20
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e		0.020	BSC		0.50	BSC
HD	0.620	0.630	0.640	15.90	**16.00**	16.30
HE	0.855	0.866	0.877	21.70	**22.00**	23.30
L	0.016	0.024	0.031	0.45	**0.60**	0.75
L1		0.039	REF		1.00	REF
θ	0°	3.5°	9°	0°	3.5°	9°

Notes:

1.Dimension b does not include dambar protrusion/intrusion.
2.Controlling dimension: Millimeter
3.General appearance spec. should be based on final visual inspection spec.

TITLE: 128LD **LQFP** (14x20x1.4 mm*2) PACKAGE OUTLINE -CU L/F, FOOTPRINT 2.0 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	LQ128 - 1
		DATE	Nov. 4.1999
REALTEK SEMI-CONDUCTOR CO., LTD			

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