Real Time Clock Module — RTC 58321

by SaRonix

Technical Data

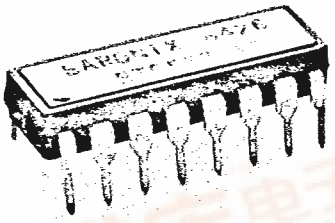
Ref. No. RTC
Date May 1985

Description

A Real Time Clock incorporating an on board quartz crystal in a single 16-pin DIP package, eliminating the need for external crystal, resistors and capacitors.

Features

- Built in 32.768kHz quartz crystal.
- Low power standby operation.
- Addressable counter start, stop, and reset function.
- 12-hour or 24-hour format.
- Automatic leap year selection.
- Microprocessor compatible 4-bit data bus.
- Standard 16-pin DIP package.
- Pin to pin compatible with MS58321RS.



Function Table

Internal Counter	Address	Address Input D_3 (A_3)	D_2 (A_2)	D_1 (A_1)	D_0 (A_0)	Address Output D_3	D_2	D_1	D_0	Count Value	Remarks
S_1	0	L	L	L	L	*	*	*	*	0~9	
S_{10}	1	L	L	L	H		*	*	*	0~5	
MI_1	2	L	L	H	L	*	*	*	*	0~9	
MI_{10}	3	L	L	H	H		*	*	*	0~5	
H_1	4	L	H	L	L	*	*	*	*	0~9	
H_{10}	5	L	H	L	H	*1	*	*	*	0~1 0~2	D_2H for p.m., L for a.m., D_3=H for 24-hour clock, L for 12-hour clock. When D_3=H is written, the D_2 bit is reset inside the IC and remains constantly at L.
W	6	L	H	H	L		*	*	*	0~6	D_2 and D_3 in the D_{10} line are for leap year selection.
D_1	7	L	H	H	H	*	*	*	*	0~9	
D_{10}	8	H	L	L	L	*2	*2	*	*	0~3	
MO_1	9	H	L	L	H	*	*	*	*	0~9	
MO_{10}	A	H	L	H	L				*	0~1	
Y_1	B	H	L	H	H	*	*	*	*	0~9	
Y_{10}	C	H	H	L	L	*	*	*	*	0~9	
	D	H	H	L	H						These selections are for resetting the 5-stage and the BUSY circuit after the $1/2^{15}$ frequency stage. Resetting is activated by latching this code on to the address latch and setting the WRITE input to H.
	E ~ F	H	H	H	L/H						These selections are for obtaining standard signals. By latching this code on to the address latch and setting READ to H, the standard signals will be output at D_0~D_3.

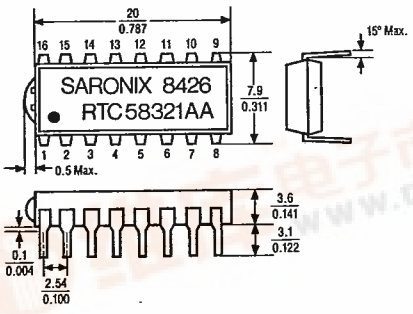
Calendar	D_3	D_2	Remainder when divided years by 4
Western	L	L	0
Japanese	L	H	3
	H	L	2
	H	H	1

Note 1. The blank spaces in the data input/output columns indicate that there are no bits. When READ is performed the L level is output. When WRITE is performed nothing will be stored in the memory because there are no bits.

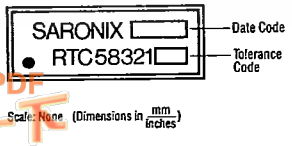
Note 2. The bit indicated by the symbol *1 is for selecting the 12hr/24hr clock and those indicated by *2 are for leap year selection. READ and WRITE are possible with all three bits.

Note 3. For address input, send a signal to the D_0~D_3 bus line, then input ADDRESS WRITE. The ADDRESS data will be latched on to the address latch.

Package



Standard Marking Format



Scale: None (Dimensions in mm / inches)

Part Numbering Guide

RTC 58321 AA

Type
Model

Stability Tolerance:
AA = ±10 ppm (0.001%)
A = ±25ppm (0.0025%)
B = ±50ppm (0.005%)

NYMPH®

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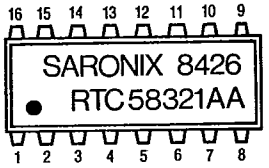
Pin Connections

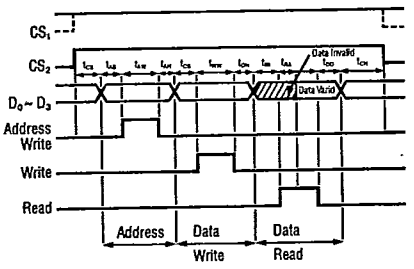


16	15	14	13	12	11	10	9
V_{DD}	NC	NC	CS_1	TEST	STOP	$\overline{BUSY}$	ADRSS WRITE

1	2	3	4	5	6	7	8
CS_2	WRITE	READ	D_0	D_1	D_2	D_3	V_{SS}

NC: Do not connect externally.

Write and Read Timing



(V_{DD} = 5V ±5% Ta = 25°C)

Item	Symbol	Min	Max	Units
CS set-up time	t_{CS}	0	—	μs
Address set-up time	t_{AS}	0	—	μs
Address write pulse range	t_{AW}	0.5	—	μs
Address hold time	t_{AH}	0.1	—	μs
Data set-up time	t_{DS}	0	—	μs
Write pulse range	t_{WW}	2	—	μs
Data hold time	t_{DH}	0	—	μs
Read inhibit time	t_{RI}	0	—	μs
Read access time	t_{RA}	—	*	μs
Read delay time	t_{DD}	—	1	μs
CS hold time	t_{CH}	0	—	μs

*$t_{RA} = 1\mu S + CR\ln\left(\frac{V_{DD}}{V_{DD}-VH}\right)$

C: Data line wiring capacity
R: Pull-up resistance value
V_H: "H" input voltage of the IC connected to the data line
In: Natural logarithms

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Conditions	Rated Value	Unit
Power voltage	V_{DD}	Ta = 25°C	−0.3~7	V
Input voltage	V_I	Ta = 25°C	GND −0.3~V_{DD} +0.3	V
Output voltage	V_O	Ta = 25°C	GND −0.3~V_{DD} +0.3	V
Storage temperature	Tstg	—	−30~+80	°C

Working Range

Item	Symbol	Conditions	Range	Units
Power voltage	V_{DD}	—	4.5~5.5	V
Data-holding voltage	V_{DH}	—	2.2~5.5	V
Quartz frequency	f_O	—	32.768	kHz
Working temperature	T_{OP}	—	−10~+60	°C

Note Data-holding voltage: Data outside the IC is not guaranteed. This voltage guarantees clock operation.

Electrical Properties V_{DD} = 5V ±5% Ta = −10~+60°C

Item	Symbol	Conditions	Min	Typ	Max	Unit
H. Input voltage	V_{IH1} Note 1	—	3.6	—	—	V
	V_{IH2} Note 2	—	V_{DD}−0.5	—	—	V
L. Input voltage	V_{IL}	—	—	—	0.8	V
L. Output voltage	V_{OL}	I_O = 1.6mA	—	—	0.4	V
L. Output current	I_{OL}	V_O = 0.4V	1.6	—	—	mA
H. Input current	I_{IH} Note 3	V_I = 5V	10	30	80	μA
L. Input current	I_{IL} Note 3	V_I = 0V	—	—	−1	μA
D_0~D_3 terminals input off-leak current	I_{LIH}/I_{LIL}	V_I = 5V/V_I = 0V	—	—	I/−1	μA
Input capacity	C_I	f = 1MHz	—	5	—	pF
Consumption current	I_{OP}	Ta = 25°C V_{DD} = 5V/V_{DD} = 3V	—	16.5/6.2	30.0/10.0	μA
Tolerances	$\Delta f/f_o$	Ta = 25°C V_{DD} = 5V	—	—	±10 ±25 ±50	ppm ppm ppm

Note 1. CS2 WRITE, READ, ADDRESS-WRITE, STOP, TEST, D_0~D_3 terminals.
Note 2. CS1 terminals.
Note 3. CS1, CS2, WRITE, READ, ADDRESS-WRITE, STOP, TEST terminals.

Circuit Diagram